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USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

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CONTENTS

HARDWARE

THE M5100 COMPUTER COMPLEX. OPERATING PRINCIPLES

Moscow VYCHISLITEL'NYY KOMPLEKS M5100. PRINTSIPY RABOTY (The M5100 Computer Complex. Operating Principles) in Russian 1979 signed to press 17 May 1979 pp 2, 3-4

[Annotation, table of contents and foreword from book by Bronislovas Bronislavovich Belyauskas, Regina Ionovna Valatkayte and Antanas Mikolovich Nemeykshis, Statistika, 17,500 copies, 144 pages]

[Text] Annotation

A new computer complex, the M5100, its structure and main principles of organization and also the technical means of reorganization of two-machine complexes are examined in the book.

The book is intended for users of the complex and can be useful to persons studying questions about the architecture and structure of electronic computers.

Contents

Foreword

Computers of the M5000 type, specialized for the conducting of mass economic calculations, have found wide application in the national economy of the country. Those computers are small electronic computers, well-suited for the processing of large masses of alphanumeric data and successfully used in computing and data processing centers and stations of the USSR Central Statistical Administration system, and also in the computer centers of small industrial and non-industrial enterprises. For the M5000 and M5010 computers both general software representing the basis of successful and effective use but also practical software in the spheres of statistics, trade, agriculture, industrial and transport enterprises, etc.

The computer complex M5100 is a new model in the family of the model M5000 computers. This computer represents a further development of the hardware and architecture constituting the base of the preceding models of the M5000 machines. Together with that, in the M5100 computer complex a number of new technological solutions have been introduced that assure some additional possibilities and greater capacity than preceding models. The differences in those solutions do not exclude, however, continuity in the family of computers of that type, that is, the new model is compatible with preceding models with respect to software. All the practical software developed for the M5000 and M5010 complexes can be used in solving problems with the use of apparatus of the M5100 computer complex. The software compatibility of the M5000 and M5010 models with the M5100 computer complex facilitates its introduction, in particular, in organizations that already have experience in the use of computers of the M5000 type.

The high capacity of the M5100 computer complex is its main difference from preceding models. The increase in capacity was achieved thanks to increase of the internal speed of the processor, rearrangement of input-output control, increase of the volume of the working storage and the external immediate-access storage, organization of the multi-program regime, etc. All this contributes to expansion of the range of problems solved with computers of type M5000.

The functional possibilities of the complex have also been expanded in another direction. The hardware and software of the complex allow the possibility of organizing two-machine complexes based on the M5100 computer complex and the M5010. In addition, interaction with other computers or terminals through outlets on the communications line is assured.

The architecture of the M5100 computer complex takes into consideration the clearly noted tendency toward replacement of punched data carriers by magnetic carriers. Actually, punched cards and tapes have great shortcomings in the quality of the means of storage of primary or intermediate data. More promising in that respect are magnetic carriers, that is, magnetic tapes and disks. At the present time there already exists the R810 data preparation system (see section 1.4), intended for the registration of data from a primary document directly on a magnetic disk. One should expect in the future the appearance of devices for the preparation of data on magnetic carriers of other types, and also the possibilities of preparing data by means of the computers themselves. These trends have been reflected in the organization of the connection of peripherals to the M5100 computer complex in general and, in particular, in the expansion of types and the number of magnetic disk and tape stores. This assures convenience of data storage and immediate access to those data.

The authors examine the logical structure and operating principles of the complex as a whole and its separate devices, and also present some comparative data. In the presentation of the material the authors started from the fact that the readers are already acquainted with the M5000 computer from the book "Perforatsionnyy vychislitel'nyy kompleks M5000" (The M5000 Perforation Computer Complex), Moscow, Statistika, 1970). And so attention is given here to aspects of the architecture of the M5100 complex and the devices that are new and distinguish that comples from preceding models. The software is an independent subject and is examined only to the extent necessary to explain the main material of the book.

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GENERAL CHARACTERISTICS OF THE M5100 COMPUTER COMPLEX

Moscow VYCHISLITEL'NYY KOMPLEKS M5100. PRINTSIP RABOTY (The M5100 Computer Complex. Operating Principles) in Russian 1979 signed to press 17 May 1979 pp 5-28

[Chapter 1 from book by Bronislovas Bronislavovich Belyauskas, Regina Ionovna Valatkayte and Antanas Mikolovich Nemeykshis, Statistika, 17,500 copies, 144 pages]

[Text] 1.1. Structure of the Complex

The M5100 computer complex is a set of logically completed devices with various functional purposes that allow their being combined into a system that constitutes its own specific variant of execution of the complex, that is, a specific electronic computer. A certain portion of the devices of the complex is necessary in each execution, and some devices of the complex can be connected selectively to create necessary configuations in accordance with the group of problems to be solved and the needs of the user. The block diagram (Fig 1.1) illustrates the composition of the complex and the logical principles of its construction and expansion.

The immediate-access storage is realized in the form of an independent R140 device and is intended for the storage of programs and data directly participating in computations. The immediate-access storage is loaded with data from external carriers through an input-output device.

The R122 processor is intended for the performance of all operations on data in accordance with the instructions list. In spite of the fact that the R122 processor is made as a separate structural unit of the complex, in considering the operating principles it is convenient to consider that it includes two independent functional parts: the central processor and the input-output processor. The functions of the central processor include the readout of program instructions from the immediate-access storage, the interpretation of instructions and the performance of operations on data, including the disposition of a result, the modification of addresses and other actions. However, if the program instruction requires any sort of actions connected with the functioning of the equipment and external in relation to the R122 processor and the immediate-access storage, then the central processor actuates the input-output processor, communicating the necessary control data to it. The functions of the input-output processor include organization of data exchange between the immediate-access storage and the external carriers, including all actions in the control of the equipment. In executing its functions the input-output processor acts independently of the central processor up to completion of exchange operations.

The input-output processor is equipped with standardized outputs in the direction of the peripheral part of the complex--toward the input-output devices, the external stores and other equipment. By standardized outputs should be understood a system of busses and signals determined by the M5100 computer complex input-output interface. The general principle of connection of the devices determined the following path of data exchange between the input-output processor and the devices: the interface lines, the equipment control unit or group of devices and the device. In that case the outputs of all control units in the direction of the input-output processor are determined by a standard set of signals and procedures in accordance with the input-output interface of the M5100 computer complex, and the outputs in the direction of the devices are different and are determined by the specifics of the devices themselves. The main purpose of the control units is coordination of the logical and electrical parameters of the devices with the parameters of the central part of the complex. The volume of the apparatus of the control units and their specific functions are determined by the type of connected devices.

The input-output devices have an R212 control panel, an R512 input-output tape perforator, an R630 card puncher, an R610 punched-card input and printers.

The R212 control panel is the main means of control of the work of the complex. The panel includes a control unit, a printer and the operator's panel of the system.

The printer is the means by which the operator has a dialog with the machine. In the process of executing programs it prints information on the course of the work of the complex, gives instructions to the operator on the performance of any previously envisaged actions, or informs him of the need to make a decision when there are alternative possibilities of continuing the work. The operator's instructions are introduced from the keyboard of the control panel printer and are simultaneously printed, and that assures documentation of the entire operator-machine dialog.

The operator's panel of the system contains necessary luminous signals that indicate to the operator normal or emergency situations in the functioning of the system. By means of that panel the regimes for execution of tasks of the complex are started, stopped or changed.

The R512 tape unit is intended for the input and output of data, the external carrier of which is punched paper tape. The device consists of

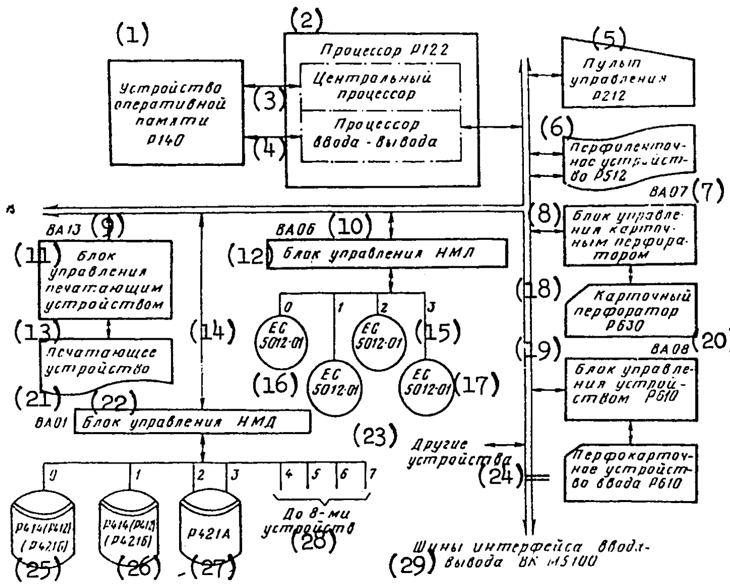

Fig 1.1. Structure of the M5100 computer complex.

1 -- R140 immediate-access storage
2 -- R122 processor
3 -- Central processor
4 -- Input-output processor
5 -- R212 control panel
6 -- R512 tape unit
7 -- VA07
8 -- Card puncher control unit
9 -- VA13
10 -- VA06
11 -- Printer control unit
12 -- Magnetic tape storage control
13 -- Printer
14 to 17 -- YeS-5012-01 computers
18 -- R630 card puncher
19 -- R610 control unit
20 -- VA08
21 -- VA01
22 -- Magnetic disk store control
23 -- Device address
24 -- R610 card puncher
25 and 26 -- R414 (R412) (R421B)
27 -- R421A
28 -- To 8th device
29 -- Interface buses of M5100 computer complex interface

a control unit, a device for readout of data from punched tape (FS-1501) and a PL-150 perforator.

The R630 card punch serves for the output of data, the external carrier of which is a standard 80-column punched card. The R630 punch is connected to the machine through a VA07 control unit. Besides its main function of signal matching the control unit recodes data from the internal code of the M5100 computer complex into the punched card code. In that unit provision is made for a memory for the brief storage of data in the volume of two punched cards in order to free the input-output processor from tracking the position of the perforator mechanism and to assure the monitoring of perforation.

The R610 input punch is used for the input of data, the carrier of which is a standard 80-column punched card. The device is connected through a VA08 control unit which accomplished the logical and electrical matching of signals, and also transformation of the data code from the punched card code into the internal code of the M5100 computer complex.

The printer is used in the complex for the output of informational reports of the operating system and the output of the results of calculations in the form of printed documents--forms, lists, tables, etc. The device is connected through a VA13control unit. A wide-format printing device of the ATsPU-128-3M or DV-313 type can be connected to that unit.

In the M5100 complex use is made of two external stores: magnetic tape stores and magnetic disk stores. Each type, with its control units, forms an external memory of the complex on magnetic tapes and magnetic disks.

The external magnetic tape store is intended mainly for the long-term storage of large masses of data in cases where operative access to data is not required, for example, during the storage of copies, archive data, etc. Magnetic tape stores can be used for the brief storage of data during transcriptions from some carriers to others and, finally, magnetic tape stores can be used as systems equipment intended for control of the process of fulfilment of tasks. Used in the M5100 computer complex are YeS-5012-01 magnetic tape stores, which are connected to the complex through a VA06 general control unit in a quantity not exceeding 4.

The external magnetic disk store occupies an intermediate position between the immediate-access memory and such external carriers as magnetic tape stores, in view of their relatively high speed, the possibility of direct access to data and fairly great capacity. On magnetic disk stores is the main load in the solution of most problems with the application of the complex. This applies to such operations in putting masses of data in order as sorting, the formation of new masses through merging, etc. It should be emphasized that the performance of such procedures with the use of magnetic disks gives the main effect from the application of the complex in the area of the processing of economic and statistical data.

In the complex, magnetic disk stores are used in three main directions:
--for the storage of programs of the operational system;
--for the operational storage of intermediate data during the execution of tasks;
--for the long-term storage of data requiring immediate access.

Since a magnetic disk store is the place of storage of programs of the operational system, it continuously participates in the control of work of the complex. The portion of the total volume of magnetic disk storage intended for the storage of programs of the operational system must be constantly preserved and renewed for the purpose of assuring the normal functioning of the complex. The remaining portion of the magnetic disk storage can be used arbitrarily with respect to the performed work and needs of the user. For example, the most frequently run programs of the user can be stored in the magnetic disk store.

Devices of types R412, R414, R421A and R421B can be used as magnetic disk stores in the complex; they are connected through the general control disk by VA01 disk stores, and their total number does not exceed 8.

All the devices have a modular structure, both in a functional respect and in respect to design execution. A device or group of devices, together with the entire control unit, can be removed from the makeup of the complex without any sort of changes in the remaining part of it. Any new device can be connected to the complex if it is equipped with a control unit with an output corresponding to the interface of the M5100 computer complex.

From the point of view of the dynamics the work of the M5100 computer complex is based on the use of the following principles:
--independence of the work of individual devices from one another;
--maximum coincidence in the time of performance of internal operations and operations of exchange with input-output devices.

The independence of the work of individual devices should be understood as the possibility of independent functioning of all outputs from the control units to the input-output processor and in the reverse direction. The action of devices connected to a single control unit should generally have limitations. Thus, operations of the exchange of data simultaneously by two magnetic disk store or two magnetic tape store devices are not permitted. At the same time, in a group of devices of the same kind it is possible to combine the performance of one exchange operation with the performance of one or more control operations, for example, readout of a tape in one device and rewinding of the tape in another magnetic tape device. If the control unit has several outputs in the direction of the interface, the work of devices connected to it can be combined. For example, the control unit in the R512 device permits readout of data from punched tape and simultaneous perforation.

The independence of the control of devices and the high throughput capacity of an input-output processor assure the possibility of combining in time the operations of exchange of all groups of devices with consideration of the above enumerated limitations. In general the sequence of the work of devices and the degree of coincidence are determined by the programs. The operations of peripheral units are controlled by the input-output processor in accordance with the established order of priority of servicing of the devices. Thus magnetic disk stores, as the most rapid peripheral unit, have the highest priority in the combination of the work of peripherals. However, devices of the same type in a group have identical priority and the device is serviced toward which the program refers.

Envisaged to a considerable degree in the architecture of the complex is independent action of the central processor and the input-output processor during the time of data exchange with the immediate-access storage and the input-output devices. It was pointed out earlier that from the moment an instruction is obtained until the operation of exchange is completed the input-output processor acts independently of the central processor, refers independently to the immediate-access storage for the disposition or reception of data relating to external carriers. The central processor is equipped with its own means of reference to the immediate-access store. The R140 immediate-access store device services two processors in proportion to the arrival of requests for servicing. When requests arrive simultaneously the priority is presented to the input-output processor, which assures the rapid disposition of data from external carriers. It is natural that in such an organization both processors must have minimum means of buffering data for the necessary waiting time. In that case the state of the devices is monitored by the software of the complex and instructions are issued to peripherals for the purpose of organizing a continuous processing of the flow of data.

1.2. Basic Composition and Alternatives of Execution

Fig 1.1 presents the functional devices and units entering the basic composition of the complex: the immediate-access store, processor, control panel, punched tape and card input-output devices, printers, magnetic disk stores and magnetic tape stores. To power those devices, the basic composition also includes an R001 unit (not shown on the diagram). Installed in that device is all the apparatus for manual switching of network voltage on and off, both for the complex as a whole and for its separate devices, apparatus for the automatic switching off of the power network in emergency situations and network filters for its protection against noises arising during operation of devices of the complex.

Still another component of the basic composition of the complex is software delivered to the user in the form of a set of carriers with recordings and corresponding operational documentation. The composition of the software is examined in section 1.6.

A specific electronic computer, constructed on the basis of devices of the M5100 computer complex, does not obligatorily contain all components of the basic composition of the complex. Obligatory components in any form of a complex are the R140 immediate-access storage, an R122 processor, an R212 control panel, an R001 power unit and software. Other devices of the basic composition can be switched on in different combination; this makes it possible to form electronic computers with different capacity in accordance with the needs of the user.

The manufacturers have proposed issuing the M5100 computer complex of the basic composition in five alternative types (Appendix 1) differing mainly in the type of magnetic disk and tape stores included.

The inclusion in the complex of special-purpose devices, that is, adapters, apparatus for output to communication lines and video terminals (see 1.7) must be agreed upon with the manufacturers of the complex.

The formation of alternative units (specific electronic computers) is based on the modular principle of construction of separate component parts of the complex in both functional and design respects. The combination of devices of the complex into a single electronic computer is accomplished on the basis of a rigid previous plan for arrangement of the apparatus. A specific set of devices together with a specific set of installation complexes that include connective cables, standard couplings intended for the electrical connection to the standard outputs of an input-output processor, and other necessary parts, also constitute a specific variant of execution of the complex.

All the apparatus (Fig 1.2) is installed around a rigid metal loop 1--of boxes intended for the laying of connecting cables between equipment with the requirements of reliability and noise resistance of the connections taken into consideration. The obligatory parts of any form of the complex are arranged in columns designated on Fig 1.2 by the positions 2, 3 and 4. In column 2 is the R001 power equipment, in column 3 the R140 immediate-access store, and in column 4 the R122 processor. An obligatory component part also is the R212 control panel (5) with the operator's panel for the system 6 and the printer 7.

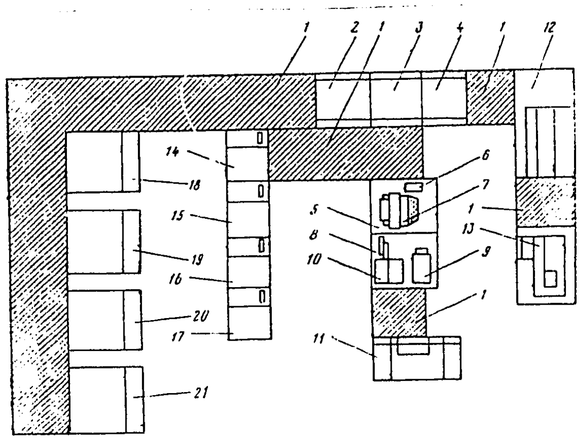

Fig 1.2. Arrangement of apparatus of the M5100 computer complex

The R512 input-output tape unit (8) is made in the form of a single structural unit that includes an FS-1501 device for readout from punched tape, a PL-150 tape perforator (10) and their control unit. An ATsPU-128-3M or DB-313 printer is designated by position 11. The control unit of the VA13 printer is set in the rack of the R512 console. That unit is an interchangeable independent structural and functional unit and when the type of printer is changed can be replaced by another unit that matches the device used.

The R630 card puncher (12) and the R610 punched card input (13) are installed in a single design type with its own VA07 and VA08 control units respectively.

The magnetic disk stores (14-17) can be of any types in a combination provided for by the alternative types of system. Their control unit VA01 is in rack 3 instead of the immediate-access store and represents an independent interchangeable structural unit.

The magnetic tape stores (18-21) are installed in a quantity of not more than 8. The VA06 tape control unit is put in rack 3.

The physical outputs of the input-output processor, corresponding to the M5100 computer complex input-output interface, are arranged in rack 4. The outputs are occupied by standardized TS coupling elements if the device is connected through them. From the coupling elements to the control units of the devices run connecting cables through which radial connections of the physical outputs of the input-output processor and the devices are accomplished.

If a device of any type is absent in a specific electronic computer, then the corresponding coupling element also will be absent, as will the control unit and the set of connecting cables, and the loop 1 will be reduced to dimensions corresponding to the specific execution.

The connection to the complex of any new device above the basic composition requires the presence of outputs corresponding to the M5100 computer complex input-output interface and the making of the control unit with observance of the construction standards of M5100 computer complex apparatus.

1.3. Technical Characteristics of the Equipment

Before examining the technical characteristics of the equipment, we will dwell on some indicators characterizing the M5100 computer complex as a computer on the whole.

1. The M5100 computer complex is compatible as regards programming with M5000 models of the machines produced earlier as regards programs of the user and information carriers.

Compatibility on the level of user programs means the possibility of running on the M5100 computer complex programs developed for the M5000 and M5010 computer complexes. However, in view of the fact that new orders and programs created with their use have been included in the order set of the M5100 computer complex, they will be run only on the M5100 computer complex.

Used in the M5100 complex as information carriers are punched cards and tapes and magnetic disks and tapes, that is, the same information carriers as in preceding models of machines of the M5000 type. Compatibility on the carrier level can be regarded as physical compatibility and compatibility with respect to information coding. The direct use of carriers of preceding models of the M5000 type of machine allows magnetic disks and tapes on which information is stored in the internal code of the machine. The data format on the magnetic tape corresponds to ISO recommendations Nos 1862 and 1863.

The data on punched cards are presented in the code of All-Union State Standard 19769-74, and the data on punched tape in the code of either All-Union State Standard 13052-74 or of MTK-2M. The presentation of data on punched cards and tapes in other codes also is allowed, but in data input and output in that case programmed precoding by means of programs of the operational system is required.

2. The M5100 computer complex permits connection to 128 input-output devices.

The devices are connected through 16 physical outputs of the input-output processor. Each physical output allows the connection of up to 8 devices of the same kind, controlled by a single control unit.

3. Reference to M5100 computer complex equipment occurs by means of physical addresses established during the development of the control units. Priority of servicing of devices by the input-output processor when they are simultaneously put in operation is determined by the place of connection of those equipment to the standard outputs of the input-output processor (the output number).

For equipment of the basic composition of the M5100 computer complex the following physical addresses have been established (the addresses are presented in sexadecimal representation):

magnetic disk stores	00, 01, 02, 03, 04, 05, 06, 07
magnetic tape stores	08, 09, 0A, 0B
printers	10, 18
card punch	20
R512 device (input from punched tape)	28
card punch of R610 input	30
R512 device (output on punched tape)	38
control panel	40

The R122 processor performs operations on binary, decimal and symbolic data arranged in the immediate-access storage and controls data exchange between the immediate-access and external storage in accordance with the program orders.

Technical Characteristics

Capacity	at least 30,000 orders/s in the solution of tasks in economic planning
Number system	binary-decimal
Representation of alphanumeric characters	8 informational bits, 1 control
Decimal data length	variable, from 1st to 31st decimal place
Alphanumeric data length	variable, from 1 to 256 characters
Form of number representation	with fixed point
Order length	variable, 2, 4 or 6 bites
Number of addresses in an order	0, 1 or 2
Number of basic orders	61
Processor cycle	0.625 microsecond
Average time required for completion of operations on two 4-digit decimal numbers:	
comparison	25 microseconds
addition	30 "
multiplication	150 "
division	250 "
Possibility of multiprogram work	execution of up to three working programs
Storage protection	program-circuit
Interruption system	" "
Input-output regime	multiplex
Input-output rate	up to 500 Kbites/s

The immediate-access storage is made in the form a separate device containing a VA03 control unit and a ferrite storage consisting of four type MSK-18 modules. Data is exchanged through the VA03 control unit, equipped with two sets of input lines, for reception of the controlling word and data from the central processor and the input-ootput processor, and one set of output lines, for the transmission of information to the R122 processor. The modules of the storage device were connected in parallel and put into operation by the general controlling word. That unit sets the cycle of reference to the immediate-access storage on the basis of requests from the central processor of the input-output processor and establishes the priority of the input-output processor during simultaneous access.

Technical Characteristics

Main memory capacity	61 Kbites
Main memory access cycle time	2.5 microseconds
Main memory word length	72 binary digits (18 binary digits per module)
Word structure	8 bites with check digits
Memory operation	reading (readout of 8-bite word); recording (recording of 8-bite word or part of word with regeneration of the initial content of the remainder of the word)

The R212 control panel is intended for the operative control of the work of the M5100 computer complex and consists of a control unit, a "Konsul-260" printer, an operator's panel and power units.

Technical Characteristics

Information carrier	roll paper 200-250 mm wide
Printing rate	10 characters/s
Line length	106 charactees
Set of characters	92

The R512 tape unit performs the readout of information, given in the form of perforations on a 5-, 7- or 8-track punched tape, and refers the read information to the R122 processor, and also punches the data obtained from that processor. The unit consists of a control unit, an FS-1501 photo-reader (CSSR), a PL-150 perforator and a power unit.

Technical Characteristics

Input rate	1500 lines/s
Output rate	80 to 150 lines/s

The R630 card punch punches data obtained from the R122 processor on 80-column punched cards. The punched cards advance in a channel and are punched by position. The R630 punch contains a reception unit for control readout of punched information from a punched card. The control is performed by the VA07 control unit.

Technical Characteristics

Punching and readout rates	100±10 punched cards/minute
Feed magazine capacity	at least 700 punched cards
Receiving magazine capacity	at least 500 punched cards
Number of receiving magazines	2

Henceforth the replacement of the R630 card punch by the PKPA80-3 (see 1.7) universal data preparation device is assumed.

The R610 punched card input device is intended for the input of data presented in the form of punched holes on 80-column punched cards. Punched cards move in the channel of the device by the narrow side, and the data are read by columns.

Technical Characteristics

Readout rate	250, 500 punched cards/minute
Feed magazine capacity	1000 punched cards
Receiving magazine capacity	1000 punched cards

Printers. Provision is made for use of the ATsPU-128-3M alphanumeric printer or the DV-313 alphanumeric printer (Poland). Both devices print data from the R122 processor on perforated paper 420 mm wide. The number of different characters used in the printers is 96.

The printing rate of the ATsPU-128-3M is 360-440 lines/minute. The largest number of characters in a line is 128.

The printing rate of the DV-313 depends on the number of characters to be printed in a line. When short lines with not more than 32 characters are being printed, the rate remains 1520 lines/minute, and when full lines of 128 characteris are being printed, the rate diminishes to 190 lines/minute.

Magnetic disk stores. All types of stores use as the carrier a detachable monodisk with a magnetic coating. The R412 store was used in preceding models of M5000 computers and is widely known by the users, and so its main characteristics are presented here only for comparison with the R414, R421A and R421B stores. In the R414 store, as in the R412 store, only one working surface of a disk is used at one time, that is, the disk must be halted for access to data on the other surface. The R414 store has a larger storage capacity than the R412. In each of those devices only one cassette with a disk can be installed, that is, those stores have a single electromechanical unit apiece. The R412 and R414 also contain electronic units that assure the performance by the devices of the required functions, and also power units.

Technical Characteristics

	R412	R414
Number of disks in a cassette	1	1
Number of magnetic heads in a unit	1	1
Number of tracks on one disk surface	128	128
Number of recordings in a presentation	$0.8\cdot10^6$ bites/s	$1.6\cdot10^6$ bites/s
Number of sectors in a track	20	40
Sector capacity	256 bites	256 bites
Useful capacity of the working surface of a monodisk	$0.65\cdot10^6$ bites	$1.30\cdot10^6$ bites
Disk rotation rate	960 rpm	960 rpm
Average time of track access	200 millisec	150 millisec

The R421A and R421B stores differ substantially from the R412 and R414 stores both in the main indicators and in a design respect. A single device in the R421A execution has two storage units with corresponding electronic apparatus and a power source. In the R421B execution the device contains one storage unit. Both surfaces of the disk installed in the device are working surfaces, which in combination with the great capacity and the good time characteristics makes the R421 convenient and effective in the processing of large masses of data.

Technical Characteristics of a Separate Storage Unit

Number of disks in a cassette	1
Number of working surfaces on a monodisk	2
Number of magnetic heads	2
Track density	5 tracks/mm
Number of tracks on a single disk surface	256
Useful capacity of the working surface of a monodisk	$5.2 \cdot 10^6$ bites
Rate of disk rotation	1500 rpm
Number of sectors in a track	not over 40
Recording and reproduction frequency	$2.5 \cdot 10^6$ bits/s

During work in the M5100 computer complex each electromechanical unit of the R421A store functions as a separate device in accordance with the assigned physical address.

The YeS-5012-01 magnetic tape store (Bulgaria) is intended for the recording, storage and reproduction of data on magnetic tape. The device consists of a tape drive, electronic apparatus that provides the recording and reproduction of data and operations of mechanism control and a power unit.

Technical Characteristics

Information exchange rate	up to 64 Kbites/s
Longitudinal density of information recording	8 or 32 bits/mm
Number of tracks	9
Tape width	12.7 mm
Cassette capacity	$2 \cdot 10^8$ bits
Tape velocity	2 ± 0.1 m/s
Power consumption	not over 2.5 kV·A

1.4. Data Preparation System

Two important aspects in the technology of processing accounting and statistical information are connected with the data carriers: the first is data storage and the second is the preparation of primary data and its input into the computer.

In the area of application of type M5000 computer complexes punched cards have long been the dominant data carrier both for the storage and for the input of primary data. The volume of work done by standard computer and data processing centers can be determined from the quantity of punched cards processed monthly--$(400\text{-}500)\cdot 10^3$. About 50 percent of them require fairly long storage--6 months or more. Punched card storage involves great inconveniences. Finally, large volumes of data on punched cards lead to a considerable expenditure of a material in short supply--paper for their manufacture. For these reasons the further application of punched cards as data carriers is not promising.

In all models of the type M5000 computer complex, including the M5100, the magnetic disk is the main data carrier in the sense of data processing and storage. The R412, R414 and R421 magnetic disk stores with replaceable cassettes assure fairly reliable and convenient storage of large masses of data and at the same time provide immediate access to the data. Besides the devices and cassettes delivered with the basic set of equipment of the complex, the user can acquire cassettes containing disks separately in a quantity assuring data storage in the necessary volume. Along with that, in the M5010 and M5100 complexes there is the possibility of storing data on magnetic tapes. Thus, with the application of computer complexes of the M5000 type the work with punched cards is reduced to just the preparation of primary data or can be eliminated completely.

In the M5100 complex the question of preparation of primary data without using punched cards can be solved by using the R810 data preparation system.

The R810 data preparation system is being produced by industry at the present time and can be acquired by a user. The system is intended for the keyboard input of data from primary documents on replaceable magnetic disk stores used in the M5000, M5010 and M5100 complexes. The application of the R810 system for the preparation of primary data instead of punched card equipment can increase labor productivity on data preparation by 25-30 percent through a greater degree of automation of data transfer from keyboard to carrier, a higher rate of execution of duplication, skipping and recording of nonsignificant zeroes, simplicity of error correction and great reliability of the apparatus. The input of data stored on magnetic disks in the autonomous R810 system also gives a considerable saving of machine time, as it is done several times more rapidly than the input of the same volume of data from punched cards.

The R810 system (Fig 1.3) is an autonomous system that assures data input from several keyboards working simultaneously and data storage on a replaceable magnetic disk. The system can have from 1 to 8 keyboards, each of which together with the control apparatus and the indication system represents an R911 operator panel. That panel has a desk-top design. The R821 control unit of that system is intended for intermediate storage, primary processing and the monitoring of data input from keyboards, coordination of the work of the panels and control of the store. An R412 or R414 can be used as the store.

Each of the operators of an R810 system is presented the possibility of the input by character of recordings with a length of 1 to 224 alphanumeric characters, constituting the lines of the primary document. The recordings are disposed on a magnetic disk in the zone allocated for the operator. Each sector of the disk in the zone allocated to the operator can contain from 1 to 15 recordings with a total length of not more than 256 bites. The total capacity of one disk surface is distributed as a function of the number of operator panels. Recordings are made on a disk in the internal code of the M5100 computer complex and can be used directly for processing after they have been stored.

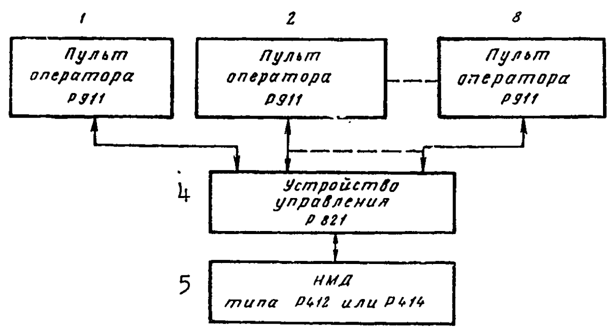

Fig 1.3. Structure of the R810 data preparation system.
1, 2 and 3 -- R911 operator panel
4 -- R821 control unit
5 -- R412 or R474 magnetic disk store

The work of the operators is automated by means of format programs consisting of a sequence of 8-bit code combinations, each of which characterizes a separate character in the recording. The format programs are stored in the process of the work in the storage of the R821 control unit and can be input from the R911 operator panel or from the store itself. The storage in the magnetic disk store of up to 200 format programs is provided for in the system. The functions of format programs include the monitoring and primary processing of input recordings, including:

--the monitoring of recordings by means of control sums within the limits of a single recording;
--the monitoring of the length of fields by means of separative information;
--monitoring the type of introduced character (figure, letter of the Russian or Roman alphabet, or special sign);
--automatic filling of all positions of the field by the code "space";
--automatic duplication of fields;
--automatic recording of nonsignificant zeroes of the indicator.

The R911 operator panel contains an alphanumeric keyboard corresponding to type 2 according to All-Union State Standard 14289-69, with a total number of 94 different characters. Besides the alphanumeric keyboard there is a separate keyboard for the input of only digital information by the "blind" method, corresponding to All-Union State Standard 15816-70.

Visual monitoring of the work of the operator and of the system as a whole can be accomplished by means of an indication table on which provision is made for the indication of an input character, orders of the format program, addresses of recordings in the magnetic disk store, the state of apparatus of the system, etc. Failure in the work of the system or apparatus through the fault of the operator is signalized by means of a sound signal.

The above examined brief technical characterization of the R810 data preparation system makes it possible for the user to become acquainted with one of the most promising methods of data preparation. The introduction of this system will lead in the end to gradual displacement of punched cards as information carriers, and consequently of punched card equipment.

In the M5100 computer complex provision is made for the use of traditional data carriers--punched cards, in view of the fact that punched card equipment is still widespread at the present time, the technology of punched card processing is well organized, but the replacement of punched card equipment and the equipping of computer centers with equipment for the preparation of data on magnetic carriers can be done gradually, in proportion to the production of a sufficient quantity of the equipment. Therefore in the set of spare parts the user receives equipment for the preparation of data on punched cards of the PKPA80-1 type, which accomplishes the punching and primary monitoring of data given by the operator by means of a keyboard.

In the M5100 computer complex provision is made for the use of punched tape equipment, but equipment for the preparation of data on punched tape is not delivered with the set, but can be acquired by the user separately. When it is necessary to store and frequently use data on perforated tape the data can be prepared by means of punched card equipment. In that case the data must be re-registered from punched cards to punched tape by means of programs of the operational system.

1.5. Technical Servicing of the Complex

Technical servicing of the complex includes the conducting of regular prophylactic and maintenance work, and also periodic verification of the working capacity of the complex. All types of work connected with technical servicing are done by means of hardware and software intended for that purpose.

The periodicity and volume of regular prophylactic work is provided for by the technical dommumentation of the equipment in the complex and assured, where that is possible, by special instruments constituting the set of of service apparatus. The service apparatus is also intended for maintenance work. The single structural and elementary base of logical devices and units of the complex permits using a small set of instruments to seek out and eliminate malfunctions in the logical units. Any standard replacement element can be inspected by means of instruments in the set of service apparatus: the SA01 stand or the SA02 stand. The SA01 stand is used for the inspection of some special standard replacement elements, and the SA02 stand for the inspection of standard replacement elements containing logical apparatus.

Very important in technical servicing are inspection of the working capacity and in the case of appearance of a failure, seeking out the place of the malfunction. Software and hardware also are provided for that work in the complex.

Operative monitoring of the working capacity of separate devices in the complex as a whole is done by means of special test and control programs. A system of test programs is delivered along with the software of the complex and embraces all the devices in the specific configuration of the complex. The main task of the test programs is verification of working capacity with maximum embrace of the functional possibilities of the component parts of the complex. However, the test programs represent the first stage in the diagnosis of failures, as they permit distinguishing the separate failed parts of the complex on the basis of data printed in the reports of test programs on the printer of the R212 control panel.

Another type of operative monitoring is the solution of check problems, which consist in programs working in regimes very similar to the regimes of fulfilment of real problems. Verification by means of check problems requires considerably more time and is recommended upon the startup of a complex after large amounts of repair or maintenance work. Check problem programs are also delivered with the software of the complex.

The methods and means of seeking out malfunctions of separate parts of a complex also are indicated in the technical documentation of the equipment. The apparatus base for seeking out the places of failures consists of built-in panels that assure autonomous working regimes of the devices and units. In most cases a faulty device can be effectively disconnected from the system in order to do repair work without halting the remaining part of the complex.

Very complex logical devices, such as the R122 processor, the magnetic disk store control unit, etc, have a fairly developed manual control apparatus, intended for the diagnosis of defects. In particular, the R122 processor assures all the working regimes necessary for the inspection and regulation of the R140 immediate-access storage in a complex without special testing apparatus.

A partially automated system for finding defects has also been developed for the M5100 computer complex, one that compiles special programs with

with fixed data and a procedure for their use. The system can use punched cards or tapes or magnetic disks as information carriers. The main task of an automated system for finding defects is effective determination of the character and place of a defect in a very complex logical device, the R122 processor, but it is also useful in finding defects in other devices of a complex.

1.6. Brief Characterization of the Software

The software of the M5100 computer complex, delivered with the equipment, consists of a disk operating system, test programs and check problem programs.

The M5100 disk operating system (DOS) is the basic software component intended for the effective use of the hardware of the complex in all its applications. The DOS consists of a group of programs that give the user the means to compile working programs and run them on the machine, and that also accomplish control of the equipment during the running of those programs. The DOS programs participate in the work of the complex both during the preparation and running of programs of the user and during the running of check problem programs and some test programs.

Test programs and check problem programs have a narrower application and are used only to verify the working capacity of hardware of the complex (see 1.5).

The software is delivered to the user in the form of magnetic disk recordings and corresponding technical documentation.

The M5100 disk operating system is a single one for all alternatives of execution of the complex and includes the programs needed for control of devices the complex in any composition. The DOS in the form in which it is delivered to the user along with the equipment of the complex can be used by him without the introduction of any sort of changes. However, in the general case the DOS in that form is not adapted in the best manner to the specific configuration of the equipment and to the class of problems solved by it. Therefore the user is presented means of generation that permit forming DOS alternatives, that is, so-called DOS generations that are most suitable in solving problems of a definite class with the use of a specific composition of devices. In proportion to the inclusion in the complex of devices of other types not in the main composition: adapters for communication with other electronic computers, video terminals, etc, in the DOS delivered to the user programs assuring the use of the new devices will be included. DOS programs are characterized by a modular structure, which also assure the possibility of forming the required DOS alternatives.

The external carrier of disk operating system programs is the magnetic disk. Magnetic disk stores of any type from the number of devices available in a specific variant of execution of the complex can be used as the DOS carrier in the process of the work.

The main tasks of disk operating systems are curtailment of the time from the moment the problem is formulated to the obtaining of the results of its solution and increase of the effectiveness of use of equipment of the complex.

Curtailment of the time from the formulation of the problem until the obtaining of the result is achieved because the M5100 DOS presents means of programming in symbolic source languages of a different level: Kobol, RPG, PL/1, Assembler and, in addition, contains a number of programs intended for service work in the adjustment and documentation of programs of the user.

Increase of the effectiveness of use of equipment of the complex is achieved by organizing, by means of the disk operating system, packet processing as the principal method of running programs of the user, and a multiprogram working regime of the complex, in which up to three programs of the user are run independently and simultaneously.

Packet processing consists in this, that all the work done, consisting of one or several programs, is formulated in the form of tasks containing controlling information for an operating system, and also programs and data relating to programs if they are required. Such tasks are grouped in packets and form an input flow of tasks for the system. The transition from fulfilment of one task to another occurs by means of the disk operating system automatically upon completion of the next task. The application of packet processing improves the use of machine time, reduces downtime of the equipment in the intervals between the running of separate programs and thus reduces the volume of work done by the operator manually.

Packet processing does not, however, exclude the possibilities of starting and running single programs.

Multiprogram work. In the M5100 computer complex, in contrast with the M5000 computer complex, a multiprogram regime of work has been realized. That regime is organized by the formation of a fixed number of sections of the immediate-access memory allocated for programs of the user. The number of sections (from 1 to 3) is established during DOS generation for the specific configuration of the equipment. The multiprogram regime of work adopted in the M5100 DOS is characterized by the fact that for each section of the immediate-access memory a certain set of input-output equipment is allocated, that is, all the means of the complex are fictitiously divided into parts constituting as it were independent simultaneously working computers.

In a multiprogram work regime in each section its own flow of tasks is run independently of the flows of tasks of other sections. Within the limits of each flow of tasks all the tasks are run successively, one after the other. Between the sections of the immediate-access memory and, therefore, the programs in the sections, a rigid order of priority is established which also determines the distribution of time of the central processor in the multiprogram regime of performance of tasks.

The volume of immediate-access memory allocated to a section is not fixed and can be established with consideration of the class of the problems to be solved, starting from some minimum volume set by the operating system to assure the functioning in the section of part of the disk operating system controlling programs.

From the point of view of the user, each section with the input-output devices allocated for it can be regarded as a separate computer, working in a regime of packet processing. Any user program can be run in any section if the volume of the immediate-access memory and the composition of the equipment allocated for that section satisfy its requirements.

Disk operating systems programs are divided according to functional designation into two groups: controlling and processing (Fig 1.4).

Controlling programs accomplish the distribution of resources of the system, organization of the uninterrupted running of programs, control of the work of equipment and monitoring of its functioning, and also assure the parallel work of the processor and input-output devices. A portion of the controlling programs is constantly in the immediate-access memory and participates in the running of any disk operating system processing program or user program.

The initial loading program acts at the moment of initiation of work of the system and is intended for readout from the resident disk and disposition in the immediate-access memory of that part of the controlling program which must constantly be in the memory in the process of running other programs.

The supervisor is a part of a controlling program and is intended for monitoring the execution of the working program and the control and monitoring of the functioning of equipment of the complex.

The main function of the supervisor is to distribute the time of the central processor in a multiprogram work regime by starting from the activity and priority of the section in which the program is run.

A section is considered active for which the immediate-access memory has been distinguished and which contains a program ready for execution. The supervisor plans the time of the central processor by surveying the sections in the order of decreasing priority. Control is transferred to the program that is in the first active section, discovered during their successive survey. That program can be run until a section with a higher priority becomes active, or in the program itself a situation develops in which its continuation is possible only after the end of some event: completion of the input-output operation, expiration of a given time interval, etc. In that case the control is transferred to the program contained in an active section with a lower priority. In the absence of active sections the supervisor transfers the computer system into a waiting mode of operation.

Other functions of the supervisor include the planning of input-output operations, the loading of programs in the immediate-access memory, the execution of procedures in the completion of programs, the organization of communications with the operator of the system, the creation of check points in working programs, the correction of equipment malfunctions, etc. All these functions can make use of programs run in each section.

The functioning of the supervisor starts directly after performance of the procedure of initial loading. In that stage of the work of the operating system the supervisor loads in the immediate-access memory and triggers the program of control of disk operating system tasks for the purpose of organizing the start of the execution of tasks. Later, during the running of other disk operating system programs or user programs, the supervisor obtains control through the interrupt system. The interruption of a program being run and transfer of control to the supervisor in some cases occur asynchronously in relation to the program being run, as, for example, during malfunctions of equipment during the running of a program. The transfer of control to the supervisor for the purpose of execution of prescribed functions can also occur upon requests of the program being run at points specified in the program. For that purpose macroorders of the supervisor that define the required functions are included in the starting program. After translation into the machine language the working program at the points of arrangement of the macroorders contains orders to refer to the supervisor that cause program interruptions, that is, transfer of the supervisor's control of the programs.

The program of task control is intended for the organization of packet processing. The task of this part of the controlling program consists in the organization of the reception of tasks and their subsequent execution, and in the organization of the preparation and start of separate recording programs. In that case the program of task control establishes the working regime of the disk operating system, designates the physical input-output devices in accordance with the logical numbers of the devices in the programs, etc. In the execution of its functions the program of task control uses information contained in special operators of task control. The necessary operators of task control are selected by the programmer during compilation of the packet of tasks. The operator servicing the complex can also act on the course of execution of the flow of tasks by introducing through the control panel printer directives of task control, similar to the operators controlling tasks included in a packet.

The task control program is stored in the system library of absolute modules on a resident disk and is called into the immediate-access memory by the supervisor after the initial loading, completion of the task or part of it, after abnormal completion of the task or according to the requirement of the operator servicing the complex. This program is run in each section in the

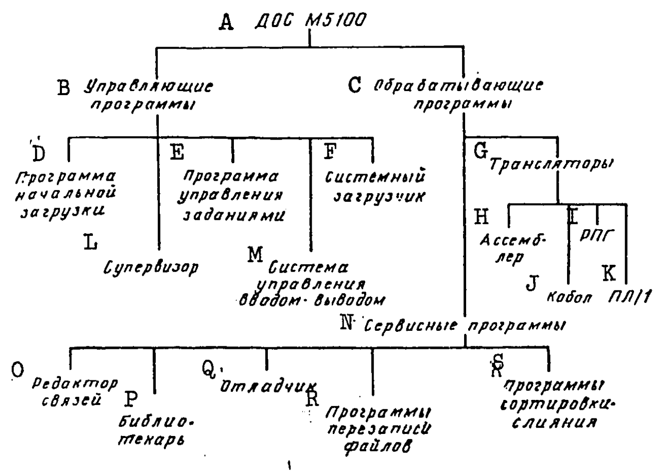

Fig 1.4. Composition of the M5100 disk operating system.

A -- M5100 DOS
B -- Controlling programs
C -- Processing programs
D -- Initial loading program
E -- Task control program
F -- Systems loader
G -- Translators
H -- Assembler
I -- RPG
J -- Kobol
K -- PL/1
L -- Supervisor
M -- Input-output control system
N -- Service programs
O -- Communication editor
P -- Librarian
Q -- Adjuster
R -- File re-recording programs
S -- Sorting and merger programs

same regions of the immediate-access memory as the problem programs. The work of the task control program is concluded by transfer of control to the supervisor with the requirement of loading of the next problem program of the packet. Thus in processing the flow of tasks in each section the work of the task control program is alternated with the next program of the packet.

The input-output control system is intended for the organization of the procedure of reference files on external carriers. Modules of the input-output control system are stored in the system library on a resident disk and are switched into the working program in the stage of preparation and execution if the initial problem program contains operators requesting the performance of definite functions of the input-output control system.

The system loading consists of a program that performs the loading of working programs in the immediate-access memory of the libraries of absolute modules by the moment of their execution. The system loader uses both the task control program, which in that case performs the loading and start of the first program module, and also the same working programs in which provision is made for loading of program phases by means of macroorders of the supervisor.

The processing programs are intended for the preparation of programs for execution, organization of program storage and the execution of procedures often used by problem programs.

Each problem program, recorded in the source language most suitable for it, is transformed into a machine language by the disk operating system translators (see Fig 1.4). Translation, as a rule, does not mean that a program has already been prepared for execution. A result of translation is the program module, constructed in relation to a certain address, determined during translation, and containing all the information permitting placement of the program in the immediate-access memory during preparation and execution. The final processing of a program is performed by means of one of the disk operating system service programs--the COMMUNICATION EDITOR.

The COMMUNICATION EDITOR does the editing, that is, the connection of program modules obtained as a result of translation. In that case a determination is made of the order of inclusion of separate models in the working program, the loading addresses are determined, standard functions are included, etc. A result of the editing is a working program in an absolute format, prepared for loading in the immediate-access memory and for direct execution.

The LIBRARIAN is a complex of programs intended for the organization and servicing of libraries in which programs of the operating system and user programs can be stored.

The disk operating system (DOS) makes provision for the management of system libraries arranged on a resident disk, and simultaneously makes it possible to organize personal libraries for the user program. A system library is intended for the storage of programs of an operating system. DOS programs are stored, as a rule, in an absolute format and called into the immediate-access memory for execution in the process of functioning of the system.

For the storage of user programs by means of DOS a library of initial modules can be organized, that is, a library of programs in the source language, and a library of absolute modules, that is, of programs ready for execution. The presence of the libraries makes it possible to exclude separate stages in the process of program preparation. For example, the user programs run most often can be stored in the library of absolute modules and called for execution as needed, which makes it possible to exclude the stages of translation and editing during each run of programs.

The ADJUSTER permits obtaining information about the work of given working sections of programs, information necessary for the adjustment of new programs.

Programs of FILE RE-RECORDING organize the recording of files of data from one carrier to another such as, for example, the re-recording from a magnetic disk to a magnetic tape, the printing of the content of a magnetic disk, the copying of a magnetic disk, etc. The programs are stored in the system library of absolute modules and can be included in tasks or executed as independent working programs.

SORTING-MERGER programs are means for the generation of specific programs for putting the data files in order or forming new files through merger. Those programs are included in the composition of the disk operating system in view of the fact that the operations of putting files in order are often used in solving a broad range of tasks. The formation of working programs meeting the needs of the user is accomplished by assigning the required parameters of programs in the editing stage.

1.7. Prospects of Development of the Complex

It is proposed to develop the M5100 computer complex in the following main directions:

--expansion of the functional possibilities of the complex by attachment of devices of other types, not provided for in the basic composition of the complex;

--gradual replacement of individual devicesof the basic composition of the complex by new and more improved devices for similar purposes as they are produced by industry.

Connected with the first direction of development of the complex is the development of devices intended for the organization of multimachine complexes, that is, devices for output to communication channels, video terminals and cassette magnetic tape stores. A brief technical characterization of devices to be included first is presented below.

Channel adapters are intended for the organization of direct communications between M5100-M5000 or M5010 and M5100-M5100 computer complexes. The inclusion of channel adapters in the composition of the M5100 computer complex makes it possible to organize multimachine complexes on the basis of M5000 computers. The principles of organization of multimachine complexes are examined in greater detail in Chapter 6.

A device for coupling the M5100 computer complex with communication channels serves for the bilateral exchange of data over commutated communication channels between the M5100 computer complex and computers of the Unified Electronic Computer System (YeS EVM). The presence of that device with the corresponding software makes it possible to connect the M5100 computer complex into the network of computer centers.

The outputs of equipment for coupling to the central part of the complex assures its functioning in accordance with the M5100 and M5000 input-output interfaces. Consequently, the coupling equipment can be used for the connection of both the M5100 computer complex and preceding models to channels of communication. The output of the coupling unit on communication channels is accomplished through modems of the YeS-8001 or YeS-8005 types. The working regimes and rates of data transmission through communication channels are determined by the modem type.

The data transmission rates are: 200 bits/s with use of the YeS-8001 modem and 1200 bits/s with use of the YeS-8005 modem.

Video terminals. A display module of the DM-2000 type can be used as a video terminal in the M5100 computer complex. Display modules are connected to the central part of the complex by an R380 coupling device. That device permits the connection of up to 8 display modules situated at a distance of not more than 1 km from the M5100 computer complex. The connection, addressing of display models and exchange of data between the central part of the complex and the display modules are accomplished in accordance with the general principles suitable for the M5100 computer complex.

The dimensions of the DM-2000 screen assure the placement of 24 lines with 80 characters per line. The display module is equipped with an internal memory, an alphanumeric keyboard with special keyboard control that permits conducting various operations of data correction: displacement, substitution, etc.

The cassette magnetic tape store is connected through a separate control unit. Replaceable magnetic tape mini cassettes are used to store data. The store is a table model with two magnetic tape cassettes.

Technical Characteristics

Type of minicassette	MK-60
Tape width	3.81 mm
Number of tracks	2 (one informational and one synchronizing)
Recording density	up to 10 imp/mm
Tape velocity	up to 0.2 m/s
Tape rewind time in any direction	not over 50 s
Acceleration time	not over 30 milliseconds
Deceleration time	not over 40 milliseconds

Data are recorded on tape successively on one track in the internal code of the M5100 computer complex. The useful capacity of the cassette is about 7 Kbites in that case.

The cassette magnetic tape store can be used as an input-output device to replace, for example, punched card or punched tape devices. An advantage of this device is the relatively cost of the device itself and the data carrier, simplicity in servicing, the possibility of efficient replacement of cassettes and convenience of their storage. The main reason for the use of the cassette store as an input-output device is the issuance of a device for the preparation of primary data on magnetic tape minicassettes, which has been planned for the near future.

The second direction of development of the complex results from the need to replace devices without prospects.

In connection with reduction of the total volume of work with punched cards in the near future it is proposed to make a change in the composition of punched card devices. A universal device, the PKPA80-3 perforator control keyboard printer, can be introduced to replace the R630 card punch and the PKPA80-1 data preparation device in the composition of the complex at the user's request.

The PKPA80-3 device is connected to the complex according to the general principles of organization of input-output through a control unit arranged in the device itself. In an autonomous working regime the PKPA80-3 device can perform all the operations of primary data preparation on punched cards done at the present time by the PKPA80-1 device. In a regime of joint work with the complex the PKPA80-3 device can be used as an input-output card punch with the following speeds: 30 punched cards per minute during input and 20 punched cards per minute during output.

This replacement represents an intermediate stage in the transition to complete rejection of punched cards as data carriers.

The further development of the complex is intended for longer periods. A characteristic feature of that stage of development of the complex is the gradual replacement of separate devices by new, more promising devices with preservation of the architecture of the complex in order to assure complete continuity of models. The replacement can take place only in the peripheral part of the complex. Also proposed is the total replacement by new of such devices as the immediate-access memory and the central processor in connection with the use of large integrated circuits.

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PRINCIPLES OF ORGANIZATION OF MULTIMACHINE COMPLEXES

Moscow VYCHISLITEL'NYY KOMPLEKS M5100. PRINTSIPY RABOTY (The M5100 Computer Complex. Operating Principles) in Russian 1979 signed to press 17 May 1979 pp 130-132]

[Section 6.1 from book by Bronislovas Bronislavovich Belyauskas, Regina Ionovna Valaktayte and Antanas Mikolovich Nemeykshis, Statistika, 17,500 copies, 144 pages]

[Text] The apparatus included in the M5100 computer complex and its organization permit in principle the creation on the basis of the M5100 computer complex and preceding models of computer systems consisting of two or more computers. The use of a computer system consisting of more than two machines requires the individual planning of software both for control of the computer system itself and for the effective practical solution of problems in that system. The simplest case of a multimachine computer system is a two-machine complex. The possibility of its use is assured by the presence of hardware and software for control of data exchange between the two computers.

The hardware and software of the M5100 computer complex envisage the organization of two-machine complexes of two types:

--combination of two computers of the M5100 computer complex through a common magnetic disk store;
--combination of the M5100 computer with an M5000 or M5010 through a channel adapter*.

A specific two-machine computer system is determined by the set of hardware and the disk operating system variant that provides for the functioning of that system. A computer system of the first type is constructed on the

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*In the future the connection of two M5100 computer complexes through a channel adapter is assumed.

basis of devices of the basic composition of the M5100 computer complex and requires only special disk operating system generation. When two-machine systems of the second type are organized, additional apparatus must be installed.

It is characteristic of two-machine computer systems with a common magnetic disk store that it consists of computers with identical capacity and communication between the machines is accomplished through an external carrier, a magnetic disk. In essence, those are two separate computers that have potentially greater effectivenesseven when used traditionally in view of the possibility of immediate access to data if the problems being solved on those machines partially overlap. Such use requires only insignificant changes in the programs existing for the separate machines, in connection with the need for redundancy of magnetic disk stores for programs. When the tasks for such a computer system are especially planned its effectiveness can be greatly increased.

The hardware and software aspects of use of a common magnetic disk store were examined in Chapter 5.

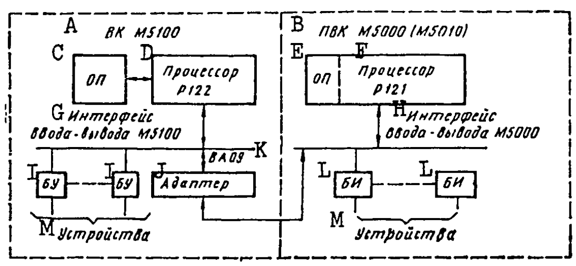


Fig 6.1. Logical structure of the two-machine complex M5100-M5000.

A -- M5100 computer complex
B -- M5000 (M5010) computer complex
C -- Processing program
D -- R122 processor
E -- Processing program
F -- R121 processor
G -- M5100 input-output interface
H -- M5000 input-output interface
I -- BU [not further identified]
J -- Adapter
K -- VA09
L -- BI [not further identified]
M -- Devices

The structure of a computer system (of the second type) is presented on Fig 6.1. In that system the exchange of data between computers takes place through input-output channels directly from the immediate-access memory of one to that of another computer under the control of program orders. In that sense one computer is a peripheral in relation to the other.

The intermediate VA09 device called an adapter enters the M5100 computer complex as an auxiliary device and is intended for the organization of commujications between channels. The functions of the adapter include electrical and logical matching of signals transmitted from channel to channel, as the function of the M5100 and M5000 computer complex channels is based on input-output interfaces different in their characteristics.

The exchange of data between computers takes place in a multiplex mode, that is, during the exchange the work of other input-output devices is allowed, and the performance of external operations in processors within the limits of the possibilities of each computer. The maximum exchange rate is determined by the less rapid channel of the M5000 computer complex input-output and cannot be more than 50 Kbites/s.

The adapter apparatus permits establishment of communications for the purpose of data exchange upon the initiative of any of the two computers. However, in specific applications one of the machines will be the initiator of communications, using the second computer as a multifunctional input-output device. This follows from the fact that in such a system one of the machines (specifically the M5100 computer complex) has higher indicators with respect to the principal technical characteristics. Thus the internal rate of calculations in the M5100 computer complex can be 2.5 to 4 times that in the M5000, depending on the character of the programs and the data. The volume of the M5100 computer complex immediate-access memory is twice as large, and the rate of exchange with the input-output devices is 2 to 4 times that in the M5000. Consequently, it can be assumed that in specific applications the main calculations and control of the system will be entrusted to the M5100 computer complex.

The organization of exchange between the M5100 and M5000 machines through an adapter will be examined in greater detail in the following section. From the point of view of functioning the M5000 and M5010 are identical, and so henceforth no difference will be distinguished between them.

[2174/315]

2174
CSO: 1863

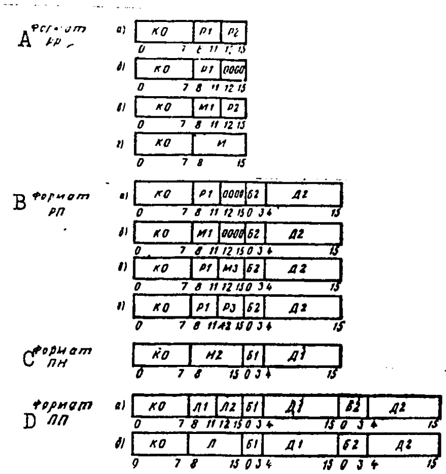
APPROVED FOR RELEASE: 2007/02/08: CIA-RDP82-00850R000200100037-8

THE M5100 COMPUTER COMPLEX INSTRUCTION FORMAT

Moscow VYCHISLITEL'NYY KOMPLEKS M5100. PRINTSIPY RABOTY (The M5100 Computer Complex. Operating Principles) in Russian 1979 signed to press 17 May 1979 p 137

[Appendix 2 from the book by Bronislovas Bronislavovich Belyauskas, Regina Ionovna Valaktayte and Antanas Mikolovich Nemeykshis, Statistika, 17,500 copies, 144 pages]

[Text]



Key: A -- Format RR
B -- Format RP
C -- Format PN
D -- Format PP

KO -- operation code
P -- register number
M -- mask
I -- direct operand
B -- base address register number
D -- displacement
L -- field length

The numeration of bits of order fields is given within the limits of a single half-word.

[2174/315]

2174
CSO: 1863

UDC 621.382:621.3.049.77

MICROELECTRONICS AND SEMICONDUCTING INSTRUMENTS

Moscow MIKROELEKTRONIKA I POLUPROVODNIKOVYYE PRIBORY in Russian No 4 1979 pp 2, 14-17, 29-33, 37-38, 45-48, 48-50, 53-56, 56-57, 62, 62-70, 95-96, 103, 108, 139-149, 155-156, 292-293, 296, 296-297, 298-302

[Annotation, table of contents, articles, excerpts from articles, and article abstracts from the collection of works "Mikroelektronika i Poluprovodnikovyye Pribory" edited by Aleksandr Anatol'yevich Vasenkov and Yakov Andreyevich Fedotov, Izdatel'stvo Sovetskoye Radio, signed to press 17 April 1979, 12,000 copies, 302 pages]

[Text] ANNOTATION

This collection of works contains articles by Soviet authors on the following subjects: general problems in and the physical principles of microelectronics, microprocessors, integrated hybrid and thin-film microcircuits, principles of integrated circuit technology, monitoring methods and measuring equipment, the designing of microelectronic equipment and the technology for manufacturing it, opticoelectronics, and new directions in microelectronics.

The basic part of this collection is devoted to questions having to do with the development and utilization of microprocessor integrated circuits and microprocessors and microcomputers based on them, engineering design methods and large-scale integrated microcircuit engineering, and the results of an investigation of the properties of discrete semiconducting instruments and opticoelectronic devices.

This book is intended for specialists engaged in the development, production and utilization of microcircuits and microelectronic equipment.

TABLE OF CONTENTS

MICROPROCESSOR INTEGRATED CIRCUITS -- THE BASIS OF FOURTH-GENERATION COMPUTERS [Excerpt -- pp 14-17]

[Text] The only alternative to the uncontrollable growth of the number of microprocessor circuits may be the systems approach to the development, production and utilization of microprocessor circuits and computer equipment based on them. The essence of this, on the one hand, is that the architecture of a series of compatible computer equipment be developed on the basis of a thorough analysis of the execution algorithms for the most diversified applied problems in a single cycle and that this equipment be the basis for all level of software and hardware, including the element base (MP [multiprocessor] BIS's [large-scale integrated circuit]). In connection with this, all the newest achievements in the theory and practice of the designing of computer architecture and microelectronics must be used. On the other hand, a series of complexes of general-purposes MP BIS's that have common structural design principles and are capable of satsifying the needs of a broad circle of users are being developed. Universality and extensive applicability are achieved because this series of complexes is being constructed on different technological bases, which makes it possible to obtain computer equipment based on them that has different productivity indicators.

Such an approach to the designing of multiprocessor BIS's does not eliminate the appearance of individual, narrowly specified

Table 3.

Серия (1)	Номер схемы (2)	Функциональное назначение схемы (3)	Технология (4)	Технические характеристики (5)						Тип корпуса (12)
				разрядность, бит (емкость лог. произведений) (6)	быстродействие, мкс (7)	потребл. мощность, Вт (8)	число команд (микрокоманд) (9)	напряжение питания, В (10)	число регистров арифм./инд./РОН) (11)	
K580	K580ИК80 (13)	Микропроцессор (14)	n-МДП (15)	8	2,0	0,8	78	±5; 12	1/0/6	244.48-1
K584	K584ИК1 (13)	Микропроцессор (14)	И²Л (16)	4n	1,5	0,13	(512)	1, 20	0/1/10	241.48-8
K587	K587ИК2 (13)	АЛУ (18)	КМДП (19)	4n	2,0	0,05	168	9	1/1/8	429.42-1
	K587РП1 (17)	Управляющая память (20)		(64) n	1,5	0,05	—	9	—	429.42-1
	K587ИК1 (13)	Обмен информацией (21)		8n	1,5	0,05	60	9	—	429.42-1
	K587ИК3 (13)	Арифметический расширитель (22)		8n	2,0	0,05	64	9	—	429.42-1
K588	K588ИК2 (13)	АЛУ (18)	КМДП (19)	16n	2,0	0,005	96	5	1/0/16	429.42-1
	K588ИК1 (13)	Управляющая память (20)		(100)	2,0	0,005	—	5	—	429.42-1
K589	K589ИК01 (13)	Микропрограммное управление (23)	ТТЛШ (25)	—	0,02	0,4	—	5	—	230.40-1
	K589ИК02 (13)	Процессорный элемент (24)		2n	0,15	0,85	—	5	1/0/11	247.28-2
	K589ИК03 (13)	Ускоренный перенос (26)		8	0,02	0,4	—	5	—	247.28-2
K589	K589ИР12 (27)	Буферный регистр (28)		8	0,08	0,45	—	5	—	239.24-2
	K589ИК14 (13)	Приоритетное прерывание (29)	—	—	0,08	0,45	—	5	—	239.24-2
	K589АП16 (30)	Шинный формирователь (31)	—	4	0,02	0,45	—	5	—	238.16-2
	K589АП26 (30)	Шинный формирователь с инверсией (32)		4	0,02	0,45	—	5	—	238.16-2
K536	14БИС (33)	Различное назначение (34)	p-МДР (35)	8	10,0	1,0	140	−24; +1,5	—	413.48-1 460.24-1
K582	K582ИК1 (13)	Процессорный элемент (24)	И²Л (16)	4	1,5	0,2		1,2	0/1/10	244.48-8
K581	K581ИК1 (13)	Регистровое АЛУ (36)	n-МДП (15)	16	1,6	0,9	—	±5; 12	0/0/26	244.48-8
	K581ИК2 (13)	Управление (37)		—	—	—	—	—	—	244.48-8
	K581РУ1 (38)	Микропрограммное ЗУ (39)	—	12	—	0,16	512	±5; 12	—	244.48-8
	K581РУ2									244.48-1

Key:
1. Series
2. Circuit number
3. Functional purpose of circuit
4. Technology
5. Specifications
19. Complementary MDP
20. Control memory
21. Information exchange
22. Arithmetic expander
23. Microprogram control
24. Processor element

[key continued on next page]

Key to Table 3 [continued]:

6. Digital configuration, bits (size of logical products)
7. Operating speed, μs
8. Power consumption, W
9. Number of commands (microcommands)
10. Power, V
11. Number of registers (arithmetic/index/general purpose)
12. Type of housing
13. K...IK.
14. Microprocessor
15. n-MDP [expansion unknown]
16. I^2L [expansion unknown]
17. K...RP.
18. ALU [arithmetic-logic unit]
25. TTLSh [probably transistor-transistor logic with Schottky diodes]
26. Accelerated transfer
27. K...IR.
28. Buffer register
29. Priority interrupt
30. K...AP.
31. Line driver
32. Line driver with inversion
33. ..BIS
34. Different purposes
35. p-MDR [expansion unknown]
36. Register ALU
37. Control
38. K...RU.
39. Microprogrammed memory unit

("exotic") circuits, although the need for their development and industrial production must be rigorously substantiated, both technically and economically.

On the basis of this approach, Soviet industry has been given the assignment of producing microprocessor integrated circuits by various production technologies. The basis characteristics of these circuits are shown in Table 3. The computational powers of the industrially produced MP BIS's will enable them to cover the needs of consumers.

Conclusions

1. Because of their extensive functional and technical possibilities, microprocessor integrated circuits are the most recent logical development of the element base for computers and can be used to design and build computer technological and digital automation equipment with practically unlimited fields of application.

2. The systems approach to the development and utilization of microprocessor integrated circuits, which consists of an integrated solution of the problems of creating computer facilities (on the programming and equipment levels), makes it possible to shorten the period for their development substantially and to economize on material and labor expenditures.

3. In order to satisfy the requirements of a majority of consumers, it is advisable to develop a general-purpose series of

microprocessor BIS complexes that have common structural features and are constructed on the basis of different engineering principles.

"LISTOPAD" -- AN AUTOMATED SYSTEM FOR ENCODING PROGRAMMABLE LOGIC MATRICES [Article -- pp 29-33]

Costs for the development of computers with microprogram control are being reduced because of the creation of microprogramming automation systems (SAMP). SAMP's based on microprogramming languages of the microassembler type are the ones most frequently used [1]. The basic shortcoming of such systems is their orientation on a specific computer that is being developed. This flaw is partially compensated for by the fact that the same SAMP can be used to develop different computer modifications that differ only in the set of microprograms.

In recent years, computer developers have begun to make wider use of programmable logic matrices (PLM) for microprogram storage [2], which makes it considerably simpler to realize such irregular parts of equipment as, for example, a command interpreter than when a PZU [permanent memory] is used. In addition to this, the special features of a PLM's structure make it possible to place quite powerful functional capabilities in a small volume [3,4].

In the development of computers using PLM's, it is necessary to have special equipment for both writing the microprograms and coding them. When writing microprograms it is necessary to take into consideration the programmability of the PLM's input bits. The encoding of a PLM also has its own specific features. A simple translation, as takes place in a SAMP for the encoding of a PZU, is no longer sufficient: it is necessary to have a minimization step for the list of PLM states obtained during the translation. The problem of encoding a PLM reduces to minimizing a system of Boolean functions with the criterion of minimality of the number of products in the disjunctive normal form (DNF) of the system; that is, the number of layers necessary in the PLM [5].

The proposed "Listopad" system was developed for the purpose of giving computer designers facilities for accelerating the development of microprograms and producing PLM codings without defects. In order to speed up the process of manufacturing and testing the crystals, the possibility of formulating data for a photosetting unit and for a system for synthesizing PLM tests was introduced into the system. The facilities for modeling and testing microprograms were allocated to a separate system and are not discussed in this article.

The "Listopad" system is a general-purpose PLM encoding means in the sense that it is not oriented to a specific microcommand system. The system's input language enables the user to introduce his own system of symbolic notations of variables and an arbitrary micro-operation syntax. The adjustment of the translator to the mnemonic notations selected by the used is carried out during the microprogram translation process.

The system's algorithmic basis is the approximative heuristic algorithm for minimizing the system of Boolean functions. The algorithm is realized on the basis of an approach [5] that is generalized to the system of Boolean functions.

The system supplies the user with a set of service raspechatki [possibly printouts] that make the problem of optimizing the encodings easier. Optimization is particularly necessary for encoding a PLM with a limited volume. The basic reserve for reducing the number of required PLM words is optimal selection of the microcommands' addresses. In view of the specific features of PLM's, the problem of optimum distribution of the microcommands by addresses differs substantially from the analogous problem for a PZU. The linear method of address distribution that has been adopted for PZU encoding is rarely optimal for the allocation of microprograms in a PLM. Instead of the standard address distribution carried out by the translator, in the proposed system the user can select addresses independently. In order to facilitate the introduction of changes in the address distribution, the microprograms are written in symbolic addresses, while the specific binary values of the addresses are given in tables.

The system has been realized on a BESM-6 high-speed computer, within the framework of a UPD-6 data control system, and includes a loading unit, a general-purpose translator, a directive unit, a minimization program, a unit for communicating with the systems for manufacturing check tests and the control program for the photosetting unit, a unit for checking the logical identity of the encodings and the microprograms, and a set of service programs for documenting the intermediate and final results of the system's operation.

The text of a problem for the system is introduced from either punched cards or a VT-340 terminal console. The loading unit begins the processing of the original text. It re-encodes the text into the system's internal code and prints indicated parts of it. The text in the internal code is sent to the translator's input, in the work of which two phases can be distinguished. In the first phase the translator processes the list of syntactical tables and adjusts the set of mnemonic notations of the input and output variables to the given user and itself to the specific syntax of the micro-operations. In contrast to the system presented in [6], the adjustment of the translator takes place during each use of the system. This enables several users to make simultaneous use of the system for the microprogramming of different computers.

In the second phase the translator carries out a syntactical analysis of the microprograms. In contrast to microprogramming languages of the assembler type, in the general case the translation is made according to the principle "one of several." The translator signals with diagnostic reports about syntactical errors. The result of the translation of syntactically correct microprograms is a list of PLM states.

In accordance with the list of directives given by the user, the directive unit formulates the necessary number of tasks, determines the output data's required form, and transfers control to the minimization program (or the unit for communicating with the systems for manufacturing and testing PLM crystals).

The minimization program perceives the list of states produced by the translator as a system of incompletely determined Boolean functions. It exposes logically contradictory lines in the list of state and signals about them with diagnostic reports. The result of the program's work is a logical copy of the PLM's encoding that can be entered (in the archive) on any information carrier and then used to produce a photographic model of the PLM and to synthesize monitoring tests. The minimization program operates with the following limitations on the list of states: number of inputs $\leqslant 40$; number of outputs $\leqslant 40$; number of lines $\leqslant 4,896$.

The user has the capability of checking the logical identity of the microprograms and any encoding from the archive. This last level of information monitoring in the system is performed by the checking unit. The system supplies the user with documentation that includes raspechatki of: the microprograms' texts, the lists of states, the PLM encodings, and tables of the states' locations in the PLM cells that are in several different forms.

With the help of the "Listopad" system, microprograms for microcomputers based on a set of high-threshold, large-scale integrated circuit KMDP's have been developed and encoded in PLM's.

Conclusions

The "Listopad" system makes it possible to use PLM's as the basis for producing flawless encoding of microprograms in a control memory, as well as to enter and encode in a PLM microprograms for a computer with an arbitrary microcommand system and a microcommand length of up to 40 bits. The system supplies the user with a set of service raspechatki that serve to accelerate the iterational process of minimizing the number of layers in the PLM. Experimental operation of the system has confirmed the vitality of the principles upon which it is based.

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ON ONE APPROACH TO ALGORITHMS FOR THE MINIMIZATION OF INCOMPLETELY DETERMINED BOOLEAN FUNCTIONS AND ITS APPLICATION TO THE ENCODING OF PROGRAMMABLE LOGIC MATRICES [Excerpt -- pp 37-38]

Conclusions

The proposed approach to an approximate solution of the problem of obtaining the shortest DNF [disjunctive normal function] engenders a class of algorithms that are distinguished by the heuristic estimate that is used. The DNF that is obtained with the help of any algorithm does not depend on the order of the assignment of the elements in the original sets. The algorithms of this class allow generalization to systems of Boolean functions, interval assignment of the original sets, and K (marking logic). This makes it possible to use this approach to solve practical problems relating to the minimization of systems of Boolean functions of large dimensions that arise during the encoding of programmable logic matrices.

SOFTWARE FOR THE CIRCUITRY ENGINEERING DESIGNING OF LARGE-SCALE MICROPROCESSOR INTEGRATED CIRCUITS [Excerpt -- pp 45-48]

The PAS [programs for analyzing nonlinear switching circuits] complex is constructed on the bloc principle. It consists of separate but interrelated blocs, with the help of which it is possible to organize two types of programs: analysis of bipolar circuits (PAS1) and analysis of MDP circuits (PAS2). In addition to this, there is an independent bloc that is a program for the automatic determination of the parameters of MDP transistor models (PARAM). In turn, the blocs are constructed of interrelated modules (subprograms) that can be replaced, depending on the specific production process, the necessary accuracy, and the form of the analysis.

The PAS blocs can be divided into two types. The first type includes those containing original information input subprograms, the input language translator and subprograms for formulating a mathematical model of a circuit. After the completion of operations by blocs of the first type, all information that is not needed for further operations is eliminated from the computer's main memory and the blocs of the second type, which contain calculation control subprograms, subprograms for the calculations themselves and the models of the elements, and result printout subprograms, are engaged.

The PAS programs were realized on the basis of a remote terminal console connected to a BESM-6 high-speed computer by a communication line. The console consists of a "Videoton-340" alphanumeric display, a "Konsul-260" electric typewriter and a YeS 9021 unit that includes a tape puncher and a punched-tape reader. For the BIS [large-scale integrated circuit] developer it is sufficient to type the information about the circuit being analyzed on the display's screen and tell the machine to solve the problem. The results of the analysis can be obtained in the form of tables and graphs on the display's screen, the electric typewriter, punched tape and an ATsPU-128 alphanumeric printer. Thus, the terminal console has been used to create a working place for the BIS designer that has quite developed software that makes it possible to achieve a high degree of dynamism in the development of electrical circuits. In addition to this, it is possible to use the PAS programs on the basis of a "Videoton-340" display with the help of the "Dimon" system.

Results of Operation

For a long time, the software for circuitry engineering designing on the basis of the PAS complex was used in the development of microcircuits with medium and high degrees of integration. The PAS programs were used to develop the electrical circuits of the K587 and K588 series microprocessor complexes of microcircuits, which were manufactured by high- and low-threshold KMDP processes, respectively. Each of the microcircuits in these complexes contains 4,000-8,000 transistors and the majority of them have an irregular structure. Besides this, the PAS complex was used in the development of the K564RU2 (a KMPD main memory with a capacity of 256 bits) and K530AP2 (a bidirectional amplifier manufactured according to the technology of transistor-transistor logic with Schottky diodes) series. It has also been used in the development of programmable logic matrix BIS's based on ESL technology and a whole series of other circuits with different degrees of integration.

During the operating process, circuits containing up to 500 transsistors have been analyzed. The analysis programs were used at all stages of schematic designing: the selection of the configuration of the individual nodes in an electrical circuit, the determination of the elements' geometrical dimensions, the calculation of the individual assemblies and the set of assemblies, the determination of the BIS's specific temporal parameters with due consideration for the topology, production technology and external conditions, and so forth.

Two basic stages in the development of the electrical circuits of microprocessor BIS's can be distinguished:
in the first stage, before the planning of the topology, it is necessary to analyze the general temporal diagram of the BIS's operation, determine the critical paths for the passage of signals and eliminate the possibility of signal competition. In connection with this, it is necessary to analyze large-volume circuits. Therefore, it is advisable to use for these purposes less than absolutely accurate models of the active elements, which gives a gain in the amount of machine time used;
in the second stage, after the development of the topology, as a rule more accurate models of the active elements, which allow for the variation in the technological parameters, are used.

It should be mentioned here that the process of developing the electrical circuits of BIS's is an iterative one: when making calculations with due consideration for the topology and variation in the technological parameters, it is frequently necessary to make a complete change in the electrical circuits of the individual assemblies.

During the operating process, the PAS programs repeatedly underwent modification for the purpose of increasing their capabilities. At the present time, a rather high degree of accuracy and a high operating speed have been achieved. For example, it required 18 minutes on a BESM-6 high-speed computer's central processor to analyze the circuit of the synchronization unit of a KMDP BIS for an arithmetic unit, which circuit contained 260 transistors. In connection with this, the dynamic analysis was performed in 1.2 s under the influence of two input signals; the transient process's results were printed at 120 points.

Conclusions

1. The software for the circuitry engineering designing of microprocessor BIS's requires a substantial increase in the capacities of the analysis programs.

2. The software for the circuitry engineering designing of microprocessor BIS's that has been developed on the basis of the PAS complex is distinguished by the possibility of analyzing circuits with quite large volumes, using acceptable amounts of machine time. The PAS input language makes it possible to enter extensive information, in compact form, about the circuit being analyzed.

AN APPROACH TO AUTOMATING THE CIRCUITRY ENGINEERING DESIGNING OF MICROCOMPUTERS [Excerpt -- pp 48-50, 53-56]

In order to design microcomputers, the developer must analyze and take into consideration the entire set of structural, logical, temporal and electrical parameters of the microprocessor's BIS [large-scale integrated circuit]. The substantial complexity of BIS's -- their functional saturation, nontrivial function algorithms, unique circuitry engineering and structural decisions used by the element base developers -- all lead to a situation where the many possibilities of BIS's remain hidden to computer developers and some are interpreted incorrectly. This can result in a lowering of the quality of the development of microcomputers or entail design errors.

The use of the programming tool that is widely used in element base designing to accelerate the development of automation in microcomputer designing is not possible. Logical modeling does not give a complete picture of the operation of a proposed variant of a circuit, allowing for the time lags and the load-bearing capability of the elements. Programs for the circuitry engineering analysis of electrical circuits, the advantage of which is the possibility of obtaining temporal diagrams of the

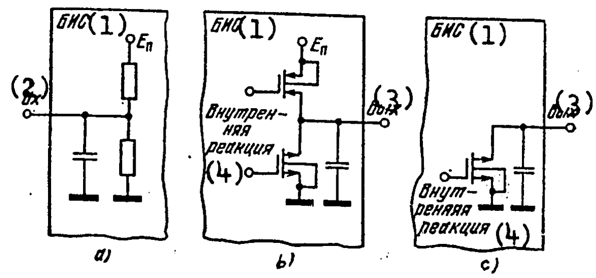

Figure 1. Models of inputs (a) and outputs (b, c) of KMDP BIS microprocessor for joining interpreters with electronic circuit analysis program.

Key: 1. BIS
2. Input
3. Output
4. Internal reaction

circuit's operation and the electrical level of the signals at given junctions, also cannot satisfy a microcomputer developer who is working with a set of BIS's, each of which contains thousands of transistors.

Existing programs make it possible to analyze electronic circuits containing no more than 500 transistors and, in addition, have calculation times that are quite long for problems involving circuits with volumes that are close to a program's maximum capacity.

Thus, at the present time the circuitry engineering designing of microcomputers does not, for all practical purposes, have a reliable and fast apparatus for the automation of the design process.

The purpose of this article is to discuss one of the possible macroapproaches to the analysis of electrical circuits presented in modular form, the role of which is played by large and medium-sized integrated circuits. Such an approach makes it possible to carry out microcomputer modeling with the help of a program for the analysis of the basic electrical circuits into which interpreters of the microprocessor set's BIS's have been introduced as library elements.

Program for the Analysis of Microcomputers

The practical realization of the proposed method for the logical-temporal interpretation of the functioning of electronic circuits is possible in two variants of the interpreting program: autonomous operation and operation in combination with an electronic circuit analysis program.

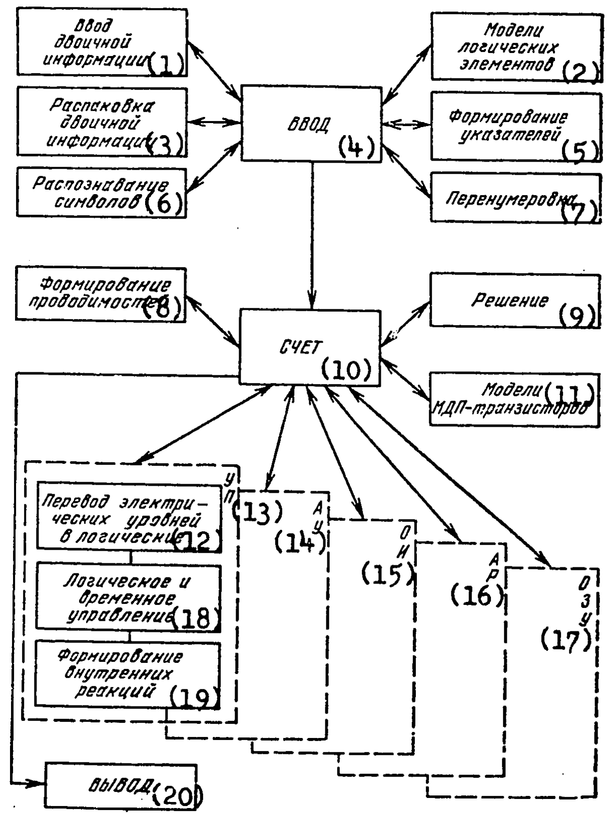

Figure 2. Block diagram of microcomputer analysis program.

Key:
1. Binary information input
2. Models of logic elements
3. Unpacking of binary information
4. Input
5. Formation of indicators
6. Symbol identification
7. Renumeration
8. Formation of conductances
9. Solution
10. Calculation
11. Models of MDP transistors
12. Transfer of electrical levels to logic levels
13. Control memory
14. Arithmetic unit
15. OI [possibly information processing]
16. AR [possibly address register]
17. Main memory
18. Logical and temporal control
19. Formation of internal reactions
20. Output

Autonomous operation of the interpreters makes it possible for the developer to obtain, quite simply, a picture of a BIS's output responses to various input actions; that is, to represent the operating algorithms of individual BIS's and the possibilities offered by the element base chosen for the microcomputer much more fully and, in a certain sense, graphically. When operating autonomously the interpreters are independent programs that are notable for a high operating speed and their own information input and output capabilities.

There are even broader possibilities when the interpreters operate in conjunction with the electronic circuit analysis program. This variant makes it possible to investigate the functioning of individual BIS's as well as sets of actually associated integrated circuits and attached active and passive elements; that is, it makes it possible to perform a circuitry engineering analysis of actual microcomputer units. In Figure 2 we see the block diagram of a microcomputer analysis program (PAME). The program was developed as a tool for automating the designing of digital computing systems based on a microprocessor KMDP BIS complex. The PAME program itself is based on the circuit analysis program (PAS) that has been widely used and thoroughly proven in the development of microprocessor BIS's and makes it possible to analyze circuits containing up to 500 transistors.

The PAME program contains all the basic blocs of the PAS program, which were developed for operation in conjunction with interpreters, and in its interpreting section there are five BIS interpreters in the complex of microprocessor KMDP BIS's. The program's interpreting section can be enalrged by connecting the interpreters of other integrated circuits that are used in the development of a specific microcomputer configuration.

The PAME program is written in the FORTRAN algorithmic language for a BESM-6 high-speed computer. It has a simple and convenient input language that is maximally close to the PAS's language. The results of the analysis of the circuits can be printed in the form of graphs of the transient processes at arbritrary junctions in the circuit being analyzed.

Preliminary results obtained during the development stage of the PAME program make it possible to drawn several conclusions. For instance, in order to carry out a circuitry engineering analysis of a conventional computing system containing 8 arithmetic unit BIS's (type 587IK2), 5 control memory BIS's (type 487RP1) and 64 main memory BIS's (type 564RU2), the PAME program's interpreting section requires about 8 sheets from the main memory of a BESM-6. In this case, a PAME program constructed on a PAS base can be contained entirely on 32 sheets in the computer's main memory. The use of special methods for the efficient utilization of the main memory (such as the concept of static loading of the program's sections) makes it possible to increase the volume of the circuits being analyzed.

The operation of the PAME program's interpreting section is distinguished by its high operating speed, since access to the interpreters from the analysis program is carried out after iteration methods have been used to solve the system of equations describing the electrical circuit being analyzed for a given time spacing. Thus, the interpreter-programs do not participate in the iterative solution process and do not cause its convergence to deteriorate. The BIS interpreters themselves do not have iterative cycles, and their operation over a given time interval is carried out in a single pass. Therefore, the basic amount of time consumed during the machine analysis of microcomputer units with the help of the PAME program is spent on analyzing the electrical circuitry composed of those microcomputer components that are not covered by the interpreters, as well as the interpreters' input and output elements (see Figure 1); that is, the machine analysis of microcomputer units can be performed in real time.

Conclusions

The proposed approach to the logical-temporal interpretation of the functioning of an integrated circuit during the circuitry engineering designing of microcomputer units can be realized if various modern, large computers are used, since -- in the first place -- large additional computer resources are not needed, and -- in the second place -- the microcomputer analysis program (PAME) that uses such an interpretation principle has a calculating time that is basically determined by the operating speed of the electronic circuits used as the basis of the analysis program.

The PAME program can be supplied to the users of microprocessor complexes as part of the complex's software. This will help speed up and improve the quality of the process of the circuitry engineering designing of microcomputers.

CIRCUITRY ENGINEERING OF A MICROPROCESSOR COMPLEX OF LARGE-SCALE INTEGRATED CIRCUITS FOR TRANSISTOR-TRANSISTOR LOGIC WITH SCHOTTKY DIODES [Excerpt -- pp 56-57, 62]

In this article we present example of circuitry engineering solutions for the input and output stages, the elements of the arithmetic-logic unit, the registers and the main memory used in the series K589 microprocessor complex of large-scale integrated circuits utilizing transistor-transistor logical with Schottky diodes [3,4].

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ASYNCHRONOUS MICROPROCESSOR SECTIONS [Article -- pp 62-70]

Efforts to limit the number of different types of large-scale integrated circuits (BIS) used in computer technology have led to the appearance of a new element base: microprocessor BIS's. Computer equipment based on microprocessors is small, consumes little power, is highly reliable, and costs relatively little. As a result of the promise offered by this innovation, in foreign countries there have appeared a large number of different microprocessor BIS complexes [1-5]. Many of these complexes have command systems of approximately the same composition that are implemented with the same technological base and have about the same productivity for the solution of type problems. The development of a microprocessor complex requires large expenditures of both economic means and time, so it is advisable to develop a general-purpose complex that makes it possible to build microcomputers with varying degrees of productivity.

Starting from the condition of insuring extensive areas of utilization, the following requirements are made of a developed complex of microprocessor BIS's: the possibility of building different versions of the microprocessor (that is, the possibility of constructing both a simple, low-speed and small-register model and microcomputers with parameters close to those of minicomputers); trunk-type communications between the modules; a minimum number of different types of BIS's in the microprocessor complex; the use of standard OZU [main memory] and PZU [permanent memory] setups in the system.

One of the main propositions arising from these requirements is the use of the principle of microprogram control; another is the construction of the processing and control circuitry in the form of sections. Such a structure makes it possible to lengthen the digital configuration of the information processing units and to enlarge the information capacity and word length of the microcommands in the microprogram control units. Furthermore, in order to insure autonomous operation of every BIS in the microprocessor complex, as well as the possibility of exchanging information with units having different operating speeds, the following proposals were advanced: an asynchronous exchange of information among the BIS's in the microprocessor complex and the introduction of synchronization circuits in every BIS in the complex.

In order to insure low power consumption, a high degree of interference rejection and a sufficiently high operating speed, KMDP technology was chosen. It imposes the following limitations on BIS development: maximum crystal size; degree of integration; average contact delay -- 30-50 ns; power voltage -- 7-15 V (high-threshold technology).

Allowing for the technological limitations, the limitations on the number of BIS housing output (≤ 42) and the basic requirements for the complex, a minimal complex of microprocessor BIS's has been developed that consists of two asynchronous microprocessor sections: information processing and microprogram control.

The Information Processing Section

This is an arithmetic unit (AU) BIS that is autonomous and controlled by a microprogrammed, asynchronous, four-bit digital information processing module, and is used to construct computer equipment operating units with different word lengths that are multiples of four. The AU BIS contains 2,700 transistors and includes the following functional units (Figure 1): a parallel arithmetic-logic unit (ALU); a bloc of general-purpose registers (RON) (R0-R7); a shifter unit; a state register; a working register (A); a microcommand register (RMK); three 4-bit channels (K1, K2, K3); exchange units (1, 2, 3); a microcommand interpreter (DSh); a synchronization unit (BS); an expansion unit.

The AU BIS's system of microcommands is shown in the table on the second page following.

The parallel arithmetic-logic unit performs the following operations: addition by units, addition, subtraction, addition modulus 2, conjunction, disjunction, inversion, copying. The

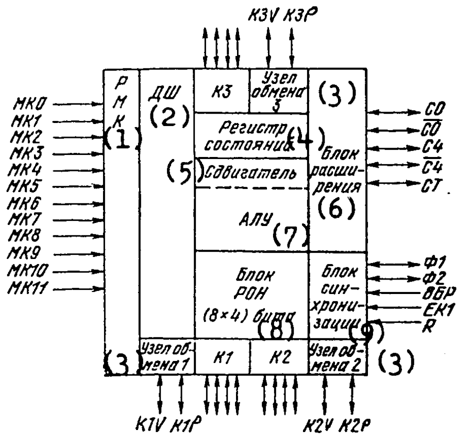

Figure 1. Block diagram of an AU BIS.

Key:
1. Microcommand register
2. Microcommand interpreter
3. Exchange unit
4. State register
5. Shifter unit
6. Expansion unit
7. ALU
8. General-purpose register bloc (8 x 4 bits)
9. Synchronization unit

ALU state indication signals -- for expansion and overflow -- are also formed in the ALU.

The bloc of general-purpose registers is used to store information inside the AU BIS and contains 8 four-bit general-purpose registers. The registers' contents enter the ALU's input through two lines. The entry of information into one of the registers is accomplished over a write-enable line.

The shifter unit performs the operations of logical or cyclic shifts one position to the right or left and also forms the AU BIS's state signals: "sign" and "comparison with 0."

The code of the operations' results is entered and stored in working register A(0-3). When information exchange operations are being carried out, working register A performs the function of a buffer register of the external channels K1-K3.

State register RS(0-3) is used to indicate the AU's states. It includes: a comparison-with-zero trigger [RS(0) = TSR "0"]; an overflow trigger [RS(1) = TPP]; a sign trigger [RS(2) = TZN]; an expansion trigger [RS(3) = TR]. The state signals are entered in RS and sent into K3 if there is a "transfer state" (VS) indicator in the microcommand. The code of a microcommand entering the AU BIS is entered and stored in the microcommand register RMK(0-11).

The microcommand interpreter (DSh) forms the control signals. The interpreter's inputs are connected to the RMK's output and, in addition, the interpreter is gated by strobe signals from the synchronization unit.

Channels K1, K2 and K3 are used to receive and transfer information. K1 and K2 carry information to and from working register A. K3 transfers information from RS to working register A.

System of AU Microcommands

0	1	2 3 4	5 6 7	8 9 10	11	Формат	Операции
0	0	коп.1	P_i	P_j	вс	PP	<P_j> ⊗ <P_i> → A, P_j ; ⊗ – опер. по коп.1
1	0	коп.1	P	коп.2	вс	A	α [<A> ⊗ <P_j>] → A ∀ A, P_i; α – опер. по коп.2
0	1	коп.1	конст.	коп.4	вс	K	[<A> ∀ <PC> ∀ МЗ] ⊗ конст. → A ∀ A, PC
1	1	коп.1	P_i	коп.3	вс	O	K1 ∀ K2 → A, <A> ⊗ <P> → A, P_i A → K1 ∀ K2

Операции		Мнем	Разряды МК команд			Загрузка РС ВС=1				Описание операции
КОП 1			2	3	4	Т"0"	ТЗН	ТПЛ	ТР	
Сложение с 1	+1	СЛЕ	0	0	0	↕	↕	↕	↕	D = (<A> ∀ <P_j>) + 1
Вычитание	–	ВЧА	0	0	1	↕	↕	↓	↓	D = (<A> ∀ <P_j>) – (<P_i> ∀ конст.)
Пересылка A		ПЕА	0	1	0	↕	↕	•	0	D = <A> ∀ <P_j>
Умножение лог.	∧	УМЛ	0	1	1	↕	↕	•	0	D = (<A> ∀ <P_j>) ∧ (<P_i> ∀ конст.)
Сложение	+	СЛА	1	0	0	↕	↕	↕	↕	D = (<A> ∀ <P_j>) + (<P_i> ∀ конст.)
Сложение лог.	∨	СЛЛ	1	0	1	↕	↕	•	0	D = (<A> ∀ <P_j>) ∨ (<P_i> ∀ конст.)
Неэквивалентность	∀	НЭК	1	1	0	↕	↕	•	0	D = (<A> ∀ <P_j>) ∀ (<P_i> ∀ конст.)
Пересылка B		ПЕВ	1	1	0	↕	↕	•	0	D = <P_i> ∀ конст.
КОП 2			8	9	10					
Сдвиг лог. вправо	↦	СЛП	0	0	0					[(<A> ⊗ <P_i>) ↦] → A
Сдвиг лог. влево	↤	СЛЛ	0	0	1					[(<A> ⊗ <P_i>) ↤] → A
Сдвиг цикл. вправо	⟜	СЦП	1	0	0					[(<A> ⊗ <P_i>) ⟜] → A
Сдвиг цикл. влево	⊸	СЦЛ	1	0	1					[(<A> ⊗ <P_i>) ⊸] → A
Инверсия	¬	ИНВ	0	1	0					¬(<A> ⊗ <P_i>) → A
С переносом ∀ с займом		ПЕЗ	1	1	0					(<A> ⊗ <P_i>) + (0 ∨ <TP>) → A TP
D → A ∨ P_i		АКР	1	1	1					(<A> ⊗ <P_i>) → A, P_i
D → A		АКК	0	1	1					(<A> ⊗ <P_i>) → A
КОП 3			8	9	10					
D → K1		ВМ1	0	1	1					(<A> ⊗ <P_i>) → A, <A> → K1
D → K2		ВМ2	0	0	1					(<A> ⊗ <P_i>) → A, <A> K2
K1 → A,...		ПМ1	0	1	0					K1 → A, <A> ⊗ <P_i> → A
K2 → A,...		ПМ2	0	0	0					K2 → A, <A> ⊗ <P_i> → A
K1 → A,... D → K2		ПВ2	1	1	0					K1 → A <A> ⊗ <P_i> → A, <A> → K2
K2 → A,... D → K1		ПВ1	1	0	0					K2 → A <A> ⊗ <P_i> → A, <A> → K2
D → P_i, K1		РВ1	1	1	1					<A> ⊗ <P_i> → A, P_i, A → K1
D → P_i, K2		РВ2	1	0	1					<A> ⊗ <P_i> → A, P_i, <A> → K2
КОП 4				9	10					
K3 ⊗ конст.		ПМ3		1	1					K3 → A <A> ⊗ конст. → A
PC ⊗ конст. D → PC		КРС		0	0					<PC> ⊗ конст. → A, PC
D → PC		АРС		1	0					<A> ⊗ конст. → A, PC
A ⊗ конст.		АКА		0	1					<A> ⊗ конст. → A

Обозначения :

D – (D_1, D_2, D_3, D_4) – результат операции по КОП 1

C – (C_1, C_2, C_3, C_4) – перенос из 1, 2, 3, 4 разрядов

T "0" – ↕ = ¬(D_1 ∨ D_2 ∨ D_3 ∨ D_4)

ТЗН – ↕ = D_4; ТР – ↕ = C_4

ТПЛ – ↕ = C_4 ∀ C_3

• – содержимое триггера не изменяется

Примечания :

1. Загрузка РС при ВС=1 зависит только от КОП 1; исключения указаны в таблице
2. Операция ПЕЗ в операциях КОП 1 СЛА и ВЧА выполняется как (<A> ⊗ <P>) + <TP> → A, в операции СЛЕ – <A> + <TP> → A, в остальных операциях по КОП 1 – (<A> ⊗ <P_i>) → A

Exchange units 1, 2 and 3 control the reception or transmission of information by (c) AU BIS, generate the signals (KIV) that accompany transmitted information, and note the reception of information with other signals (KIP).

The expansion unit is used for the discrete (in four-bit units) lengthening of the arithmetic unit's word length without connecting any additional equipment. The lengthening is accomplished by combining the $C4_i$-CO_{i+1} and $\overline{C4_i}$-$\overline{CO_{i+1}}$ outlets. In the highest-order halfbyte the ST outlet is connected to the "ground" line, while in the rest it is connected to the power line.

The synchronization unit is used to organize the microcommand implementation cycle. This cycle begins when a VBR signal or a positive F2 signal front enters the unit, and consists of three sequential stages: reception, reading and entering. Signals at the F1 and F2 outputs indicate all three states of microcommand implementation. The transmission of control signals to these outputs from without makes it possible to delay the implementation cycle of any of the microcommands and also to operate in the external synchronization mode.

The Microprogram Control Section

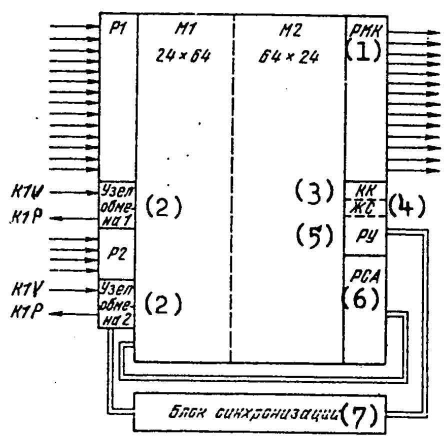

Figure 2. Block diagram of UP BIS.

Key:

1. Output register
2. Exchange unit .
3. "End of command" indicator
4. "Expectation of reception of states" indicator
5. Control register
6. Following-address register
7. Synchronization unit

This is a control memory (UP) BIS that is an autonomous, asynchronous module for processing digital information and is used to build microprogram control units with different information capacities and different microcommand and command digital configurations. The UP BIS includes the following functional units (Figure 2): a permanent memory of the "programmable logic matrix" (PLM) type; input registers R1(0-13) and R2(0-3); a following-address register RSA(0-5); information exchange circuits 1 and 2; a synchronization unit (BS); a control register (RU); an input register RMK(0-13).

The PLM-type permanent memory is used for the storage and readout of microcommands. The PLM consists of two programmable logic submatrices (M) and a programmable layer of inverters. The first submatrix is equivalent to 64 24-input "and-not" circuits, while the second is equivalent to 24 64-input "and-not" circuits. Communications in the submatrix are programmed by the user and are entered rigidly during the manufacturing process.

Input registers R1(0-13) and R2(0-3) are used to receive and store information entering from without. The need for changing the information in R1 and R2 is determined by the contents of the control register's (RU) triggers.

Information exchange units 1 and 2 are intended for the organization of the asynchronous reception of information in input registers R1 and R2. When signals arrive from the control register's appropriate outputs, the information exchange circuits change over to a state of readiness to receive information. If a signal accompanying the transmitted information appears at the K1V and/or K2V inputs, the information exchange circuit generates signals that gate information reception into R1 or R2 and response signals K1P and/or K2P, which indicate the completion of information reception.

Control register RU(0-3) stores the indicators of the UP BIS's internal units' operating modes. RU(0) is the "end of command" (KK) indicator trigger. The KK indicator is specified by the programmer in the microprogram's last microcommand and permits the reception of information in R1. RU(1) is the "expectation of reception of states" (ZhS) trigger. The ZhS indicator appears in the microprogram when branchings with respect to states are necessary, and permits information reception in R2. In addition to the basic indicators KK and ZhS, there are additional triggers in the RU that provide different UP BIS operating modes.

The internal synchronization grid of the UP BIS's functioning and the external synchronization signals F2 and KK are formed in the synchronization unit (BS).

The BIS complex's basic parameters are: power voltage E_p = 9V$\pm$10 percent; operation execution cycle in the AU BIS -- 2 μs; microcommand formulation cycle in the UP BIS -- 1.5 μs; static power consumption of the BIS -- 10 mW; dynamic power at maximum BIS working frequency -- 200 mW; "0" voltage at information outputs for I_{out} = 0.5 mA -- $<$0.5 V; "1" voltage at information outputs for I_{out} = 0.5 mA = $>(E_p$ - 0.5 V); static interference rejection reserve -- 2 V.

The modular nature of this complex's structure, microprogram control, the trunk-type communications, and the developed system of microcommands together with the asynchronous external and completely autonomous internal synchronization insure that computer equipment based on it will have broad capabilities and great flexibility. The area of utilization of this KMDP complex is from the simplest controllers to high-productivity micro- and minicomputers, and from multiprocessor and multicomputer information and control complexes to microcomputer networks.

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A MULTIFUNCTIONAL COUNTING DEVICE [Excerpt -- pp 95-96, 103, 108]

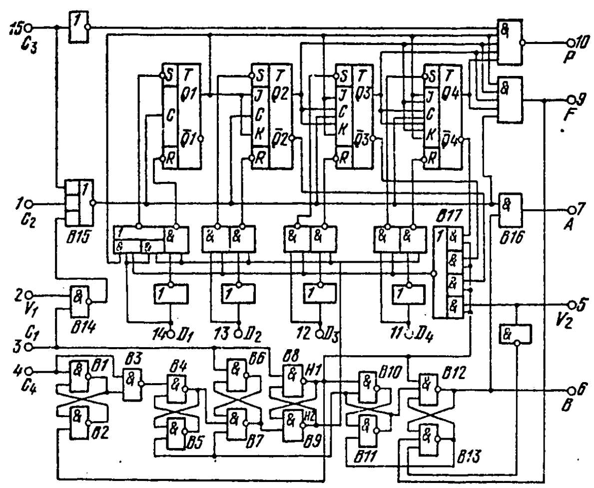

Figure 3. Functional diagram of counting device.

The inclusion in a microprocessor complex of circuits that make it possible to perform the functions of frequency dividers and pulse shapers expands the complex's logic capabilities for the construction of multiprocessor devices. As a supplement to the series K580 multiprocessor complex, the K589KhL4 multifunctional counting device has been developed. It performs the

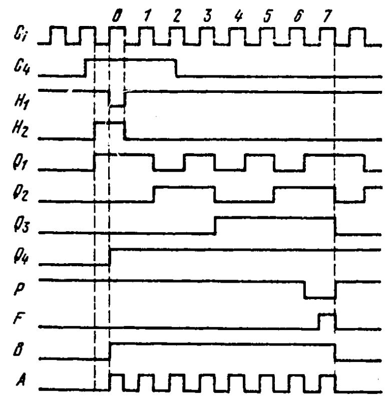

Figure 4. Temporal diagrams of counting device.

functions of a frequency divider, a discrete delay line, a pulse bundle shaper, and a pulse duration shaper with a variable coefficient of the function being performed. It contains a programmable frequency divider and special shaper circuits. There are also additional inputs that are used to connect several microcircuits for the purpose of increasing the word length.

Conclusions

1. The analysis of digital, large-scaled integrated circuits by the sequential Descartian graph method makes it easier to understand the functioning of highly complex circuits.

2. The microcircuitry of the multifunctional counting device that has been developed makes it possible to use it effectively in different pieces of computer and digital automation equipment.

A SEMICONDUCTING MAIN MEMORY MODULE FOR MICROCOMPUTERS [Article -- pp 139-149]

In a microcomputer, as a rule, the card on which the processor is located additionally contains only the microcommand memory (PZU [permanent memory], PPZU [semipermanent memory]) and a small (usually 64 bytes) ultrahigh-speed OZU [main memory] (SOZU) or a minimal OZU and PZU (PPZU) complex. Any further increase in the memory's volume is obtained by a modulus-by-modulus enlargement of the OZU and PZU (PPZU) in that proportion dictated by the specific nature of a particular computer's utilization.

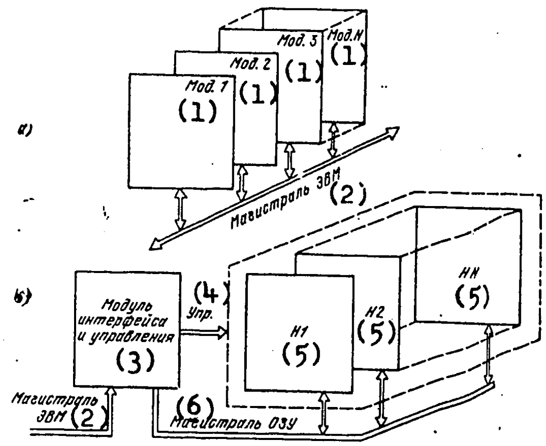

Figure 1. Diagram of the enlargement of a microcomputer's memory: a. all OZU module circuits located on one card; b. with control on a separate card and enlargement by means of connecting storage cards to the main line.

Key:

1. Module .
2. Computer main line
3. Interface and control module
4. Control
5. Storage card .
6. OZU main line

Depending on its design, an OZU module can have one of two types of structures (Figure 1). In the first type (Figure 1a), the OZU's information capacity is enlarged by parallel connection to the computer's main line of functionally complete modules that have their own control and interface circuits and are structurally contained on a single printed-circuit card. In the second type (Figure 1b), the control and interface circuits are on a separate card, and the memory is enlarged by connecting storage cards without control circuits to the OZU's main line. It should be mentioned here that the memory's structure (Figure 1b) can have different modifications (for example: an interface card, a control-regeneration card, storage cards and so on). In connection with this the equipment redundancy is minimal and the storage cards can have greater capacities than in the first type.

For a microcomputer, the most preferable OZU structure is the one in Figure 1a, which makes it possible to have a minimum number of types of OZU cards, simplify the computer's design considerably, and make it organizationally more flexible. At the same time, when designing the storage section of the module

Параметр (1)	Тип ОЗУ (2)				
	(3) Модуль ОЗУ—НЦ03Д	(4) in—481-1 на БИС ЗУ—2107В	(5) М—416-М для ЭВМ Imp-16C	(6) MSV11-B для LSI-11	(7) MSV11-A для LSI-11
Емкость (8)	8К×16	16К×8	8К×16	4К×16	4К×16
Время выборки, нс (9)	550	450	550	550	475
Цикл обращения, нс (10)	750	600	1400	—	1150
Потребляемая мощность, Вт (11)	11,0	8,0	—	12,7	17,4 (статика) (12) 42,2 (динамика) (13)
Габаритные размеры, мм (14)	300×180×12,0	203×157×12,2	280×216×25,4	228×132×12,7	266×228×22,9
Удельная мощность, мВт/бит (15)	0,09	0,063	—	0,19	0,65
Удельная плотность компоновки запоминающих элементов, бит/см³ (16)	202,3	336,9	85,33	186	52

Key:
1. Parameter
2. OZU type
3. OZU-NTs03D module
4. in-481-I based on 2107V ZU BIS
5. M-416-M for IMP-16C computer
6. MSVII-B for LSI-11
7. MSVII-A for LSI-11
8. Capacity
9. Access time, ns
10. Memory cycle, ns
11. Consumed power, W
12. Static
13. Dynamic
14. Dimensions, mm
15. Specific capacity, mW/bit
16. Specific density of arrangement of memory elements, bits/cm³

on the basis of ZU [memory unit] BIS's [large-scale integrated circuit] and the control circuits on the basis of medium-scale integrated circuits (SIS), the equipment redundancy connected with the enlargement of the memory is not great. Basically, in order to enlarge a microcomputer's memory, there are structural locations in its frame where one or several additional memory cards are inserted.

Below we present a description of the special features of an autonomous OZU-NTs03D module, which is constructed from semiconducting IS's [integrated circuits]. The module was developed for the basic "Elektronika NTs-03D" model of a series of microcomputers, but can also be used for a number of other computers.

The element base of the module's memory section consists of K565RU1A ZU BIS's of the dynamic type, with a capacity of 4,096 bits, that were manufactured by n-channel MDP-technology.

The module's operation is controlled by TTL [transistor-transistor logic] circuits (series K155 and K170 IS's). The 32 K565RU1A microcircuits, which are arranged on the card in 2 rows of 16 circuits each, form a memory matrix with an information capacity of 16 Kbytes (8,192 x 16-bit words). The entire module is contained on a 300 x 180 mm printed-circuit card. Its basic specifications are presented in the table on the preceding page. For the sake of comparison, we also list the specifications of the in-481-I OZU module produced by the Intel Company (United States) [1], the M-416-M ferrite ZU for the IMP-16C computer manufactured by National Semiconductor (United States) [2] and the ferrite and semiconductor OZU's for the LSI-11 computer produced by the Digital Equipment Corporation (United States) [3].

The good characteristics of the Intel Company's in-481-I OZU are the result of the fact that this module is intended for use in a microcomputer operating with eight-bit words, and in connection with this has a different memory matrix organization from those of all the others listed in the table. The reading or entry of 8 bit positions instead of 16 requires less equipment and leads to a considerable reduction in the power consumed. By comparing the data in the table, one can see that for an equal information capacity, the semiconducting OZU modules have substantially better characteristics than those based on ferrite cores.

The OZU contains the following functional parts (Figure 2): a memory matrix, an address register (Register A), a data register (Register D), a phasing circuit, a regeneration circuit, a multiplexer (A/RA), a recognition circuit and a control circuit. In addition to its normal functions of organizing the OZU's cycle and controlling the reception and transmission of information, the OZU module's control circuit performs additional functions to provide communications with the subscriber (using the interface that is provided) and to switch the inputs during exchange and regeneration.

From the processor or other units, the module receives: 16 address code bit positions A<0...15>, data code bit positions D<0...15>, and control signals. The address and the data arrive in the line shapers over the same main lines. The read data D<0...15> arrive in the processor over the same A, D lines, as does the kvitirovaniye [translation unknown] signal "Answer" (OTV). In all, 21 lines are used for exchanges with units that are external relative to the module: 16 A, D lines and 5 control lines.

The control circuit insures the OZU module's operation with other units in three exchange modes: "Read," "Enter," "Read

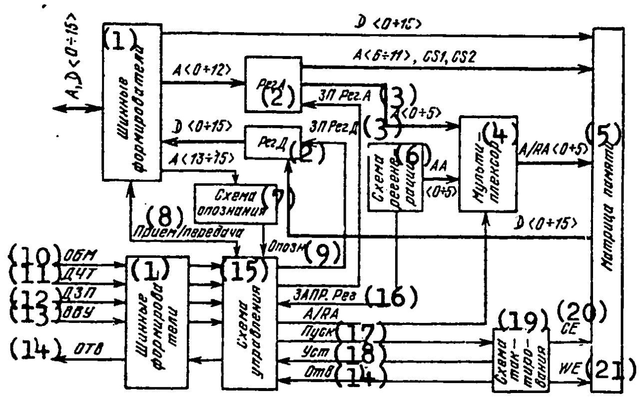

Figure 2. Functional diagram of NTs03D OZU module.

Key:

1. Line shapers
2. Register
3. Enter in Register
4. Multiplexer
5. Memory matrix
6. Regeneration circuit
7. Recognition circuit
8. Receive/transmit
9. Recognition
10. "Exchange"
11. "Data for reading"
12. "Data for entry"
13. "Access to external units"
14. "Answer"
15. Control circuit
16. Regeneration inquiry
17. Start
18. Set
19. Phasing circuit
20. "Enter read data in data register"
21. "Enter"

(Modification) Enter." Temporal diagrams of the OZU module's operation in different exchange modes are shown in Figure 3.

Any exchange mode begins with an OZU module inquiry by an "Exchange" (OBM) signal. If the module's number is recognized according to the three highest-order bits in the address code A< 13...15>, this signal insures the entry of the address in the address register and the preparation of the control circuit for operation.

In the "Read" mode, a "Data for reading" (DChT) signal enters the OZU module. On the basis of this signal, the control circuit generates a "Start" signal for the phasing circuit, while the line shapers switch to the transmission of data that have been read, from the OZU into the computer's main line. This same signal serves as the reading indicator. On the basis of the "Start" signal, the phasing circuit (which is constructed on the shift register) forms the basic phasing signals that are needed for the module to operate in the given mode: "CE," for turning on the ZU [memory unit] crystals, "Enter in Register

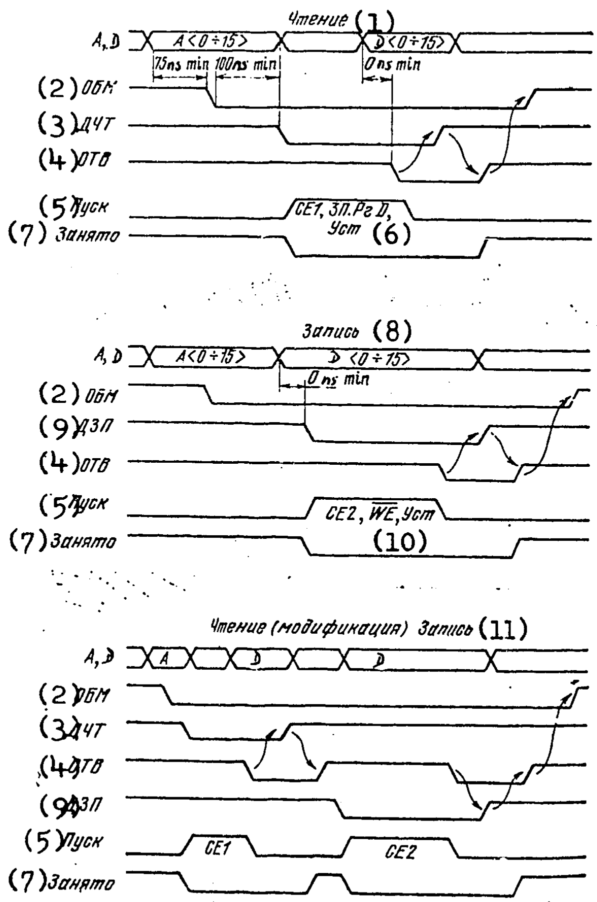

Figure 3. Temporal diagrams of OZU module operation in different exchange modes.

Key:
1. Read
2. Exchange
3. Data for reading
4. Answer
5. Start
6. CE1, enter in Register D, set
7. Engaged
8. Enter
9. Data for entering
10. CE2, WE, set
11. Read (modification) enter

D" and "Answer," for entering the data that have been read in the data register, and "WE," for entry in the memory matrix in the entering mode. The data that have been read are accompanied by an "Answer" kvitirovaniye signal that is read after the erasure of the DChT signal.

In the entering mode, after the address is cleared the data code and a "Data for entering" (DZP) signal, which in this case also serves as the reading indicator, is placed in the main line.

In the exchange mode, a "Read (modification) enter" signal causes the information to first be read and then entered for the same address in the OZU module. For an OZU, this exchange mode is not in pure form that mode that is understood for a dynamic-type ZU, when the reading and entering are carried out during the time of action of a single CE signal (in the absence of CE, the ZU's crystals are in a storage mode and require an insignificant amount of power). In this case, for the exchange interface the duration of the CE signal is lengthened by the amount of time needed to replace the data that have been read and the data for entering in the main line. Increasing the duration of the CE signal leads to an increase in the power used by the memory matrix.

Considering the specific conditions for the use of an OZU module in a microcomputer (a significant amount of time -- ~300 ns -- for the replacement of information in the A, D main line), in the exchange mode the reading cycle relative to the DChT (a CE1 signal is formed) is carried out first, followed by the entering cycle according to the DZP (CE2). This made it possible to simplify the control circuit and the phasing and to reduce the power consumed by the module in the exchange mode. For this same purpose (reducing the required power) and despite the fact that there is a buffer address register in K565RU1A ZU crystals, in the module there is an address register (Register A) that is external relative to the memory matrix and makes it possible to obtain a minimum duration of the CE signals during the reading and entering cycle, although this also leads to an increase in the total cycle time in all exchange modes.

The K565RU1A integrated circuits that are the basic elements of the OZU module are dynamic-type memory units that require periodic restoration -- regeneration -- of the stored information. In these ZU's, information regeneration is carried out in the entering mode as well as the reading mode. When one access to the ZU crystal is carried out, 64 memory cells are immediately regenerated. Since the reading cycle takes less time and is simpler to form than the entering cycle, regeneration is usually performed during reading and the crystal selection signals (CS1, CS2) are in a turned-on state. In order to restore all the information in the OZU module's memory matrix, it is necessary to perform 64 such cycles during the regeneration period. For this reason, the module contains a simple, fully autonomous regeneration circuit that consists of the following series-connected units: a pulse generator (GI), a frequency divider (DCh) with a variable division factor, and a 6-bit counter (SCh) of regeneration addresses (0...5). The pulse generator's frequency and the frequency divider's division factor were selected so that the 64 regeneration cycles are distributed over the entire regeneration period. This made it possible to achieve a more uniform temporal distribution of the power required in the regeneration mode. The regeneration address changes before each new regeneration cycle. The regeneration system's layout is shown in Figure 4.

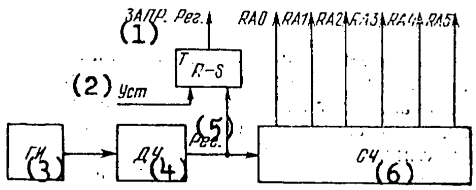

Figure 4. Regeneration system of OZU module.

Key:

1. Regeneration inquiry
2. Set
3. Pulse generator
4. Frequency divider
5. Regeneration
6. Regeneration address counter

From the frequency divider's outlet, the regeneration pulse moves to a trigger, where it is stored. The regeneration inquiry signal ("Regeneration inquiry") moves from the trigger into the control circuit, in which the regeneration inquiry and any exchange inquiry have equal priority. When these inquiries are superimposed in time, the control circuit processes them in sequence. In this case there is an increase in either the exchange cycle with the OZU module, by the duration of the regeneration cycle, or in the regeneration period between the cycles of regeneration of a single address, by the time of the exchange cycle, which is easy to allow for in the master clock (GI) when necessary.

Resetting of the regeneration inquiry trigger to "0" takes place at the end of each regeneration cycle. Such a regeneration system eliminates additional losses of working time (and, correspondingly, of operating speed) on the part of the OZU module for the preparation of the regneration mode and makes this mode completely autonomous.

The "Engaged" signal (Figure 3) is an internal signal of the OZU module that is formed simultaneously with the "Start" signal and is present in both the exchange and regeneration modes. From the moment the phasing circuit starts up and the "Engaged" signal appears, a change in all the control signals at the

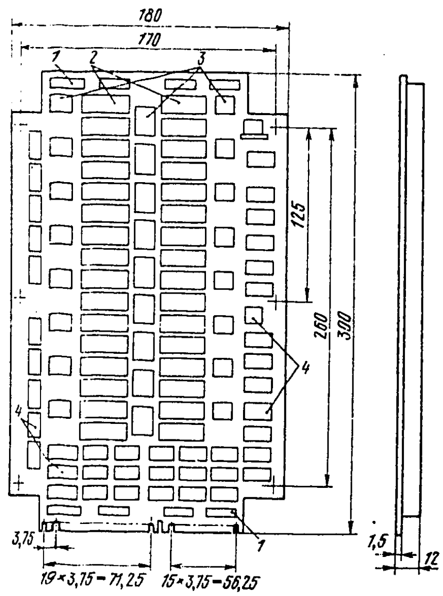

Figure 5. Layout of NTs03D OZU module on a card: 1. electrolytic capacitors; 2. K565RU1A ZU BIS; 3. uncoupling capacitors; 4. control circuits.

input does not affect the OZU module's operation in the initially assigned exchange mode, which insures protection of the module, with respect to its control inputs, from random malfunctions in the computer's main line during its operating cycles.

In the absence of exchange inquiries, all the fixing triggers in the control circuit are constantly in the zero state. The control circuit's trigger resets to "0" automatically. Therefore, a control signal to set the unit to "0" is not required for the OZU module's system.

In addition, it is possible to connect a signal for access to external units (VVU) to the memory module so that the OZU module's control circuit is blocked when it enters the computer's main line. A 16-bit code and the presence of a recognition circuit on the module make it possible to increase the volume of a microcomputer's memory to 128 Kbytes. When necessary, the VVU signal can be used as a high-order bit in the address code, which makes it possible to increase the memory's volume to 256 Kbytes.

Structurally, the OZU module is a card with a two-sided printed mosaic, on the printed elements of which no rigorous limitations are imposed (Figure 5). On the card there is no ground plane as such, although the conductors along which different power voltages are carred to the microcircuits installed on the card do form a grid. When taken in conjunction with the corresponding uncoupling capacitors, this makes it possible to reduce to a minimum the level of the noise arising during operation of the module's circuits. All of the elements on the card (both integrated circuits and discrete components) are on one side of the card, which makes it possible to automate the process of installing and removing the elements.

This design of the OZU module for microcomputers provides the following characteristics: asynchronous exchange of data with user, ease of enlarging the main memory and changing its configuration on a module-by-module basis, independent regeneration, and a high degree of technological feasibility from the production viewpoint. The inclusion in the module of a control circuit that insures exchange matching with users, in addition to a regeneration circuit and placement of all the circuits on a single princted-circuit card, made it possible to produce an autonomous, functionally and structurall complete main memory unit for microcomputers.

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INTERRELATIONSHIP OF MAXIMUM OPERATING SPEED AND DEGREE OF INTEGRATION OF LARGE-SCALE INTEGRATED CIRCUITS [Excerpt -- pp 155-156]

Conclusions

1. When realizing the maximum degree of integration of elements on a cyrstal, reducing the elements' dimensions does not lead to an increase in their operating speed because of the necessity for a corresponding reduction in the power consumed by each element.

2. Increasing the operating speed of elements without changing the thermal conditions of their operation is possible when the maximum degree of integration of the elements on a crystal is not used. In connection with this, the operating speed of the elements in a BIS [large-scale integrated circuit] can be increased by a maximum factor of W/A.

3. Increasing the linear resolving power of the methods for applying the elements of the figure on a crystal makes it possible -- when the maximum degree of integration is not sought -- to increase both the operating speed and the degree of integration of the elements on the crystal without changing the thermal conditions of their operation.

4. When selecting the element and structural base of a processing logic unit with maximum productivity, it is necessary to insure fulfillment of the condition $\tau_d \approx \tau_{com}$, which corresponds

to an optimum relationship between the operating speed and the degree of integration of the BIS's elements.

5. In the designing of BIS's for high-productivity computers, when realizing the optimum relationship between the elements' degree of integration and operating speed, it is advisable to use a matrix structure of the elements on the BIS crystal by using thermal shielding zones between the elements (microradiators) in order to organize the interelement connections.

In conclusion it is necessary to mention that in the analysis of BIS operating speed carried out above, in which we considered the limitations imposed by the problem of discharging heat and insuring the given temperature for the p-n junctions, we did not take into consideration the limitations imposed on the elements' linear dimensions and operating speed by the phenomena of electromigration and the increase in the ohmic resistance of conductors, which arise when there is a substantial decrease in the elements' dimensions and an increase in current density. The role of these phenomena becomes substantial and must be taken into consideration when the elements' and conductors' dimensions reach tens of nanometers.

ABSTRACTS

UDC 681.327.25-185.4

ASSOCIATIVE PARALLEL PROCESSORS AND MICROPROCESSORS

B.M. Malashevich

The author gives a brief analysis of the history and present state of development of associative processing devices, classifies them, and list the requirements for them. He points out the possibilities of associative parallel processors and the actuality of their practical realization at the present time, on the basis of microprocessor large-scale integrated circuits. Figures 7, references 9.

UDC 681.3.06

MICROCOMPUTER SOFTWARE BASED ON A SINGLE-CRYSTAL MICROPROCESSOR

A.V. Kobylinskiy, H.G. Sabadash, A.K. Teslenko

The authors discuss the composition of the software for a microcomputer based on a single-crystal microprocessor, as well as the structure of the program preparation and debugging systems for microcomputers based on general-purpose and microcomputers. They also discuss the advantages and shortcomings of such systems, as well as ways for developing them further. Figures 3.

UDC 681.325.5

QUESTIONS ON INCREASING THE OPERATING SPEED OF A MICROPROCESSOR WITH A TRUNK STRUCTURE

E.P. Ovsyannikova-Panchenko, L.M. Petrova, V.S. Kokorin, B.V. Shevkoplyas

The authors present two variants of designs for logic circuits for the internal main line of a microprocessor, both of which make it possible to increase a microprocessor's operating speed when performing sequential micro-operations. They discuss questions concerning the coincidence of main line transmission in a processor and formulate the conditions under which it is advisable to introduce an additional apparatus for analyzing the compatibility of micro-operations and the dynamic reorganization of the temporal flowchart. They investigate a probability model of the microcommand execution process and suggest specific layout variants for the construction of a unit for controlling the coincidence of micro-operations and blocs for analyzing microcommand codes. They also show that the amount of equipment needed can be reduced considerably through rational selection of the encoding of micro-operations, in addition to formulating an encoding algorithm. Figures 7, references 2.

UDC 681.3.056

ANALYSIS OF METHODS FOR CONSTRUCTING DEVICES FOR COMPARING A SET OF NUMBERS THAT ARE BASED ON LARGE-SCALE INTEGRATED CIRCUITS

I.P. Seleznev, B.M. Malashevich

The authors discuss methods of designing devices for comparing sets of numbers for extremes (maximum or minimum). They suggest modifications of sequential-type devices, with nonparallelization of operations and a unilateral structure, that are oriented on the realization, in the form of a large-scale integrated circuit assembly, of a single or standardized large-scale integrated circuit with a modular structure that provides a possibility of designing various comparison devices. They also present and illustrate with examples methods for determining the devices' operating speeds, as well as calculating and optimizing some of their parameters. Figures 4, references 3.

UDC 621.3.061

AUTOMATING THE DESIGNING OF LARGE-SCALE INTEGRATED CIRCUITS WITH DUE CONSIDERATION FOR THE OPTIMUM DISTRIBUTION OF THE POWER RESOURCE

A.V. Vorob'yev, Yu.P. Rodionov, A.V. Skvira

The authors propose a new method for designing large-scale integrated circuits that allows for optimum distribution of the power resource among the individual stages in the circuitry. They present a mathematical formulation of the problem of deterministic optimization of large-scale integrated circuits according to power parameters. They also develop algorithms and a program for the optimization of "DETOPT" large-scale integrated circuits. The method and the program have been approved in a number of semiconducting memory layouts. As an example, they present the results of large-scale integrated circuit optimization for a main memory with a capacity of 256 bits. Figures 4, references 7.

UDC 681.326.74.06

ON THE QUESTION OF THE MACHINE SYNTHESIS OF TESTS FOR DIGITAL LARGE-SCALE INTEGRATED CIRCUITS

B.V. Batalov, A.I. Berezenko, O.I. Tishchenko

The authors give a brief description of the methods used as the basis for a type program complex for the synthesis of check tests for logic circuits of the combined and sequential types. They evaluate the effectiveness of the utilization of the program complex for large-scale integrated circuits of the combined type, operational memories and large-scale integrated circuits in microprocessors. They also present methods for modernizing such a program that make it possible to improve the effectiveness of its use for large-scale integrated circuits that include regular masses of memory cells. Figures 4, references 8.

UDC 621.377.622.12

THE SHIFT REGISTER IN INSTRUMENTS WITH CHARGE CARRY

V.M. Gusakov, A.V. Zelentsov, V.I. Odinokov, Ye.S. Sel'kov

The authors discuss an 8-bit shift register in instruments with charge carry. The register is based on p-channel MDP's [expansion unknown] of transistor structures with framing circuits based on mutually complementary MDP-transistors. They calculate the coefficient of inefficiency of the charge transfer in the shift register, the maximum clock frequency of its operation, and the temperature dependences of these parameters. They also present the results of an experimental investigation of the shift register's characteristics. Figures 4, references 6.

UDC 681.327.67

ENGINEERING DESIGN FEATURES OF INTEGRATED MEMORY CIRCUITS BASED ON BIPOLAR STORAGE UNITS WITH AN INJECTION POWER SUPPLY

S.G. Isakina, M.A. Korolev, N.M. Lukanov, A.A. Orlikovskiy,

The authors discuss the basic factors that limit the operating speed of I^2L integrated circuits. They show that it is possible to increase the operating speed with the help of structures that have special, irregular alloying admixture distributions in a thin epitaxial layer, as well as by using transistorized structures of the reversed type. They also list the parameters of these structures and their electrical characteristics. Figures 7, references 6.

UDC 681.327.67

HIGH-SPEED INTERNAL STORAGE INTEGRATED CIRCUITS BASED ON AN INJECTION STORAGE UNIT WITH CURRENT CONTROL

A.A. Orlikovskiy, A.G. Sergeyev, V.N. Gladkov, T.Ya. Mamedov, V.N. Savenkov, V.N. Rybal'chenko

In this article the authors reveal a highly efficient method for controlling injection storage units that insures a high operating speed for the integrated circuits of a memory based on them. They analyze the transient processes in the storage unit that are related to current control and present substantiated experimental parameters of integrated circuits for operational memories of the transistor-to-transistor logic and ESL [expansion unknown] types. Figures 9, references 13.

UDC 681.327.67

REDUNDANCY IN SEMICONDUCTING MEMORIES

V.S. Borisov, V.V. Losev, V.A. Shakhnov

The authors discuss one method for improving the quality of semiconducting memory units (ZU) that consists of encoding the information being processed in memory cells (ZYa) with the help of interference-free codes. They present a number of design solutions for redundant ZU's that eliminate functional defects. The design solutions for redundant ZU's were developed with due consideration for the statistical results of the distribution of defective ZYa's. Figures 5, references 10.

UDC 621.3.049.77:382.323:372.54+58

INTEGRATED MICROCIRCUITS OF GYRATORS IN COMPLEMENTARY MDP STRUCTURES

V.N. Galkin, Yu.P. Mashkovtsev, B.I. Mikhaylov, A.M. Skvortsov, V.M. Shilkov

The authors analyze an actual gyrator as an inductance equivalent. They discuss the parameters of the amplifying stages in KMDP-structures [expansion unknown] from the viewpoint of their utilization in gyrators and present the results of an experimental investigation of prototypes of integrated circuits for gyrators. Figures 3, references 5.

UDC 658.562.6:621.382.8:519.2

UNIDIMENSIONAL SUPPLIER AND USER RISKS IN CONNECTION WITH AN ARBITRARY LAW GOVERNING THE DISTRIBUTION OF A CONTROLLABLE PARAMETER'S VALUES

A.S. Bondarevskiy, L.M. Popel'

The authors present expressions for calculating the values of the unidimensional supplier and user risks in connection with an arbitrary law for the distribution of a controllable parameter, a normal law for the distribution of the results of the control (an equivalent measuring conversion), right- and left-side boundaries of the tolerance field, and due consideration for departmental and delivery classification norms. They also calculate the risks related to controlling the input flow of the logic unit of an integrated circuit of the transistor-to-transistor logic type. Figures 3, references 12.

UDC 658.562.6:621.382.8:519.2

ON REDUCING ERRORS IN MULTIPARAMETRIC MONITORING

A.S. Bondarevskiy, L.M. Popel'

In multiparametric monitoring, which is characterized by rather large supplier and user risk values, it is recommended that the parameters, the monitoring of which has the least reliability, be repeatedly and selectively rechecked. The authors present expressions for indicators of the reliability of multiparametric monitoring: the probabilities of the truthfulness of the result of monitoring "defectiveness" and "serviceability." Figures 2, references 5.

UDC 621.382.2

LIMITING PROPERTIES OF A SEMICONDUCTING DIODE IN A TRANSMITTING CHANNEL

M.M. Ivanov, V.A. Malyshev, V.A. Shpirt

The authors discuss the change in the power transmitted through a semiconducting limiter diode connected in parallel in a superhigh-frequency channel when there is a change in the level of the incoming power. They present a technique for calculating the limiting characteristics, including with an allowance for the effect of self-displacement. They also compare calculated characteristics and experimental results. Figures 1, references 4.

UDC 621.382.3

RELATIONSHIP BETWEEN A CHANNEL'S PARAMETERS AND A FIELD TRANSISTOR'S CHARACTERISTICS

A.B. Yegudin

The author presents a simple method for measuring the distribution of the mobility of the charge carriers in a field transistor's channel with respect to its current-voltage characteristics, a method for determining the value of the parasitic and active parts of the channel's resistance for any distribution of the charge carriers relative to the depth of the channel, and the results of an investigation of the parameters of field transistor channels by the suggested methods. He takes note of the correlation between the electron mobility values and the noise factor of the investigated instruments at high frequencies. Figures 3, references 4.

UDC 621.317.327.4:382.2

SELF-CONTROLLED SEMICONDUCTING DEVICES IN THE SUPERHIGH FREQUENCY BAND

O.S. Orlov, V.A. Murav'yev, V.M. Kogan, Yu.V. Myasnikov

The authors discuss different types of self-controlled superhigh-frequency band devices that are based on semiconducting diodes and, depending on the type of output characteristics, are classified as limiting, stabilizing and blocking. They present a method for calculating a throughput-type limiting device with two diodes, and also suggest variants that realize the output characteristics of the N-shaped and piecewise-broken type. Figures 12, references 11.

UDC 621.382.28:621.382.2.029.64

MODELING AN OPTIMUM SEMICONDUCTING MATERIAL FOR VARACTORS

A.S. Berlin

The author suggests a quality factor for the semiconducting material for epitaxial varactors, on the basis of which (with due consideration for frequency and temperature requirements) he performs a comparative analysis of the properties of semiconductors, determines requirements for an optimum hypothetical material, and discusses triple compounds based on solid solutions of the A^{III}-B^{V} type. Figures 3, references 12.

UDC 621.383.9+93

FEATURES OF THE DEGRADATION OF PELLICULAR ELECTROLUMINESCENT DISPLAYS

F.I. Vergunas, V.I. Kononenko, V.I. Lur'ye

During the production of pellicular electroluminescent displays running on direct current and based on layers of Cu_xS and ZnS:Mn, the conductivity of these layers was monitored. During operation, in the degradation of the displays the authors noted that the brightness tended toward a steady-state value of 10 ± 1 kd/m^2, which is maintained for a period of 5,000-8,600 hours and does not depend on the power voltage or, consequently, the initial brightness. Figures 1, references 6.

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APPLICATIONS

HOLOGRAPHY AND OPTICAL DATA PROCESSING IN GEOLOGY AND GEOPHYSICS

Leningrad GOLOGRAFIYA I OPTICHESKAYA OBRABOTKA INFORMATSII V GEOLOGII I GEOFIZIKE in Russian 1979, pp 2-4, 193-194

[Annotation, table of contents and introduction from book edited by S. B. Gurevich, Order of Lenin Physico-Technical Institute imeni A. F. Ioffe, Leningrad, 500 copies, 195 pages]

[Text] Annotation

Reports read at the All-Union Seminar on Optico-electronic Methods of Processing Geological and Geophysical Data, held in Tomsk in 1978, served as the basis for the present collection. The main theme of the collection is the processing of large masses of geophysical data and the creation of new instruments and devices for the optical processing of geological and geophysical materials. Specific methods and devices are examined along with survey reports on that theme. The materials presented in the articles are of great importance for the development of work envisaged by the national economic plan. They provide the possibility for specialists, geophysicists and geologists to become acquainted with the new possibilities opened up by holography and methods of optical data processing in tasks of searching and prospecting for minerals.

CONTENTS

Introduction

The complexity of the problems to be solved in the search for petroleum, gas and solid mineral resources requires a considerable increase of computer capacities and the development of methods and means of effective processing of geological and geophysical data. Computer compleses based on second and third generation electronic computers existing at the present time do not completely meet contemporary requirements, in connection with which a number of important and necessary algorithms for the processing of geological and geophysical data often are not realized in practice. It should be expected that in proportion to the development of work on area systems of observations and seismic holography the requirements for the efficiency and operativeness of data processing will grow still more. In that respect much interest is aroused by the further improvement of digital means of data processing as well as the development of optical and optico-electronic methods which have considerable possibilities with respect to the processing and storage of large flows of data.

At the present time in a number of scientific and production organizations and VUZ's of the country experience has been accumulated in the development and use of optical computer systems, experience that confirms the prospects of development of that direction of automation of the processing of data of exploration geophysics and geology.

The First All-Union seminar on the optico-electronic processing of geological and geophysical data, held in 1978 in Tomsk, summed up definite results of investigations in that area.

The present collection contains reports read at the seminar that were devoted to questions in the development and investigation of optical computing devices and hybrid optico-electronic data processing systems. Some methodical and technological methods of processing, directed toward improvement of the methods and means of processing geological and geophysical materials, are examined.

The publication of the collection, in our view, will undoubtedly have a positive influence on the further conducting of investigations and will permit acquainting specialists with the results achieved in this area.

It is proposed to continue in the future the discussion of optico-electronic methods and means of processing geological and geophysical data and to issue subsequent collections of articles.

Professor S. B. Gurevich and candidates of technical sciences V. P. Ivanchenkov and O. A. Potapov

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THE PROBLEM OF PROCESSING LARGE MASSES OF GEOLOGICAL AND GEOPHYSICAL DATA AND WAYS TO SOLVE IT

Leningrad GOLOGRAFIYA I OPTICHESKAYA OBRABOTKA INFORMATSII V GEOLOGII I GEOFIZIKE (Holography and Optical Data Processing in Geology and Geophysics) in Russian 1979, pp 5-18

[Article by O. A. Potapov from book edited by S. B. Gurevich, Order of Lenin Physico-Technical Institute imeni A. F. Ioffe, Leningrad, 500 copies, 195 pages]

[Text] Annotation

Starting from the tasks facing geological and geophysical searches for petroleum, gas and solid minerals, the requirements for processing systems have been formulated. It has been shown that in the processing of large masses of geological and geophysical data great prospects are connected with coherent optical and high-speed optico-digital complexes. Processing circuits based on the use of a "Kogerent" laser installation are examined in the case of its use as a processor in an optico-digital system.

The solution of complex contemporary problems of geological and geophysical exploration for oil, gas and solid minerals requires making complexes of various technical means and methods. The timely processing of data obtained in that case is impossible without using enormous volumes of electronic computer machine time.

However, second generation computers characterized by a small immediate-access memory and a relatively low operating speed are unable to effectively and qualitatively process data obtained by field investigations. In connection with that, together with improvement of the methods of digital processing, in the last decade optical and optico-electronic methods of analysis of geological and geophysical data began to be used [1,2]. In that case much attention is given to the processing of seismic survey materials, which is explained mainly by the application of seismic surveying in searches for oil- and gas-bearing structures. This method differs from other exploratory methods by an incomparably greater volume of data and the application of multichannel registration on a real time scale. It suffices to say that one 24-channel seismogram with a 2-millisecond interval contains about 10^6 bits of information.

The processing of such a seismogram on a medium-sized computer (BESM-4 or Minsk-32) takes about 1 hour, and so a single computer is capable of processing in 2 or 3 shifts the material obtained by 3 or 4 seismic stations. To process the entire volume of data obtained in the field hundreds of electronic computers are needed for seismic surveying alone. If it is taken into account that there are other geophysical methods besides seismic surveying, it can readily be shown that further progress is unthinkable without radical change of the processes of geophysical data processing.

The same situation also exists in geology, where the information is either two- or three-dimensional. Thus a portion of the geological materials is usually presented in the form a two-dimensional distribution of the optical density of phototransparencies--these are aerial and space photos of the surface of the earth, photographs and microphotographs of paleontological and lithological-petrographic objects, photographs of landscapes, rock outcrops, etc. The information capacity of such photographic documents is very great. For example, an aerial photograph with a scale of 1:200,000 contains 10^7 - 10^8 bits of information. In the existing processing of geological materials, based on manual methods or on the use of electronic equipment, only an insignificant and not always the mose useful part of the data registered in the field is extracted.

The tendency toward steady complication of the processing of geological and geophysical data, and especially of seismic data, advances the following requirements for the hardware of a computer center:

1) the presence of autonomous high-speed data input and output devices, connected with the internal memory of the main processor;

2) the possibility of operating with a fairly large number of geophysical channels in the course of a brief time interval, for which the main processor must have disks or a large volume of memory on magnetic drums;

3) the presence of specialized processors that permit performing a broad set of operations (rapid Fourier transformation, convolution, correlation, various types of summation, etc);

4) a large volume of the immediate-access memory and high speed of the main and preliminary processors;

5) developed software that permits using various processing algorithms and rapidly modifying them in the process of the work;

6) the possibility of direct dialog of man and machine, that is, the computer must issue the results of processing in any of its stages in a form permitting the interpreter to rapidly evaluate them and if necessary to set new parameters or new kinds of processing.

At the present time there is practically no hardware satisfying the enumerated requirements. At the same time both Soviet and foreign experience show that making complexes of optical systems and electronic computers will permit solving many processing problems. Specialized optical devices are already capable of meeting the requirements listed as points 2-4 and 6.

The application in organizations of the USSR Ministry of Geology of large third-generation electronic computers (the YeS-1050, YeS-1060 or BESM-6), now being planned, will considerably expand the possibilities of computer complexes. Using the speed of the YeS-1050 computer, which is 500,000 operations per second on the average, and also taking into account the contemplated use of electronic special processors, computer-preprocessors and improved input-output devices, one can consider that processing capacity will increase in proportion to the increase of the computer speed, that is, to about 20 times that of a second-generation computer. There is no doubt that this will permit complicating the processing and expanding the range of problems solved. Moreover, the growth of the volumes of data requiring processing will be comparable with the increase of the capacity and productivity of computer complexes, as a result of which their efficiency also can prove to be insufficient to satisfactorily solve the problems of increasing the thoroughness, detail and precision of geological and geophysical methods of surveying. For example, increase of the geological effectiveness of seismographic work for oil and gas involves a need to apply digital methods of recording information and the use of area (holographic) systems of observations made by the method of multiple coverings. The large masses of information thus obtained must be efficiently analyzed by means of various complex algorithms, including two-dimensional and three-dimensional space-time transforms, the volume and importance of which in the overall cycle of processing will steadily increase.

In the solution of the problem of processing large masses of data, of special interest are optical methods, the effectiveness of which is due to the high informational capacity of a luminous field as an information carrier, the possibility of considerable increase of the rate of processing on account of parallelism of the processes of counting, transmission, processing and recording of optical information and, finally, the possibility of accomplishing an entire series of integral operations on two-dimensional (three-dimensional) masses of information. Since in optical processors the elementary operations are multiplication, integration, Fourier and Laplace transformations and convolution, even now it is possible to solve with them mathematical problems with an equivalent speed of 10^{13} operations per second, whereas for electronic computers the most optimistic estimates do not exceed 10^9 operations per second.

With such advantages of optical processing taken into consideration, optical methods of processing seismic data were first tested in the Central Geophysical Trust of the RSFSR Ministry of Geology in 1966 on the basis of a French laser device. Then that work was set up in the "Spetsgeofizika" trust, the "Soyuzgeofizika" Scientific-Production Association and other organizations of the USSR Ministry of Geology on the basis of the Soviet "Kogerent" optical apparatus. In the period since then the MOV (reflected wave method), KMPV (correlation method of refracted waves), VSP, MOGT and MOG (not further identified) optical methods of seismic data processing have been developed and introduced into production. By means of a coherent optical system operations of the calculation of unidimension and two-dimensional spectra and unidimensional and two-dimensional correlation functions are being successfully accomplished, as well as of frequency filtration with prescribed filter characteristics and two-dimensional space-time (fan) filtration of starting seismic-survey materials. In the stage of testing are operations of D-transformation of seismic time profiles and filtration by means of holograms (filters with a complex transparency function) to realize certain processing algorithms, for example, reverse filtration.

Such a set of optically accomplishable operations permits successfully applying optical methods of seismic data processing in the stage of preliminary analysis of the wave field to select the optimal field work procedure and the subsequent data processing, and also directly for seismic data processing and evaluation of the obtained results. The achieved speed of optical methods can be illustrated on the example of bandpass frequency filtration, which at the present time, with imperfect technology, can be done 20 times more rapidly and 20 times more cheaply than on the BESM-4 computer.

Besides seismic survey materials, methods have been developed and are being introduced for the optical processing of data obtained by aerogeophysical methods and gravitation and resistivity prospecting, and also materials of aerial surveys and other various geological information.

The processing technology can be illustrated by the block diagram presented on Fig 1. Geological or geophysical data visualized by a plotter on a photocarrier are microfilmed and presented on 24 x 36 mm photographic film. The photographic film obtained from the microfilming device or microplotter ("Kvant" model) is placed in the beam of coherent light of a laser installation. The necessary operations are accomplished, depending on the set program for the processing or analysis of the starting information. The result is viewed on the screen of an industrial television set and registered by optical and photoelectrical methods. The material proceeds from the output of the laser installation to the interpreter and if necessary returns again to the input for additional procedures of optical processing.

The laser installation, a diagram of which is presented on Fig 2, includes a helium-neon gas laser with a power of 3-10 MW in single-mode conditions, an optical system, a set of diaphragms and slit shutters, low and high pass filter systems, band-pass and fan filters; they are made up with 2-3 industrial television sets and photographic and photoelectrical registering equipment. The filtration is usually carried out separately in several Fourier transform planes.

During the complex processing of seismic data with the use of electronic computers and laser equipment the processing graph of Fig 3 is accomplished on the whole. The laser equipment is used for operations of preliminary

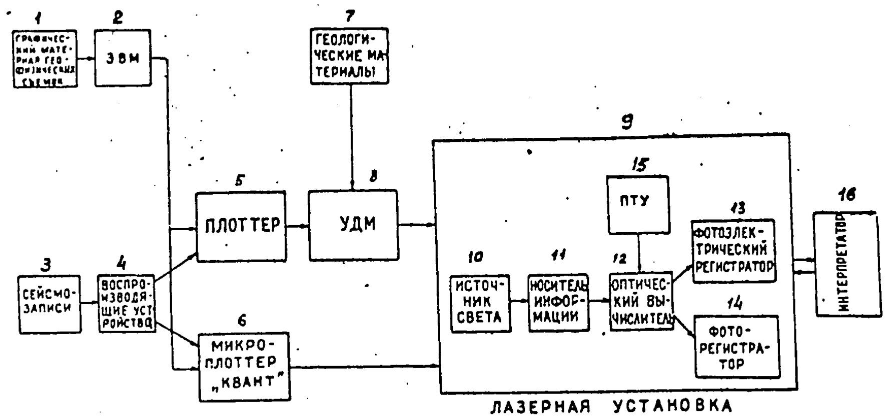

Fig 1. Block diagram of machine processing of geological and geophysical data on the basis of the "Kogerent" optical apparatus.

Key:

1 -	graphic material of geophysical surveys	9 -	laser device
2 -	electronic computer	10 -	light source
3 -	seismic recording	11 -	data carrier
4 -	reproducing devices	12 -	optical computer
5 -	plotter	13 -	optico-electrical register
6 -	"Kvant" microplotter	14 -	photo register
7 -	geological materials	15 -	industrial television set
8 -	microfilming equipment	16 -	interpreter

preliminary analysis of the wave picture as regards frequency and apparent velocity, operations of spectrum-correlation analysis of laser data before and after summation by a computer, and also procedures of additional or main frequency and space-time filtration of the summary sections are performed on the laser installation. The execution of separate procedures on the electronic computer and on the laser installation is different in time, which is a shortcoming of such a processing system. However, practice shows that the introduction of the presented graph provides a perceptible economic and geological effect resulting from the machine processing of the starting materials.

Side by side with important advantages, optical methods of data processing have definite limitations, of which difficulty in performing a large number of logical operations is of very great importance in processing data

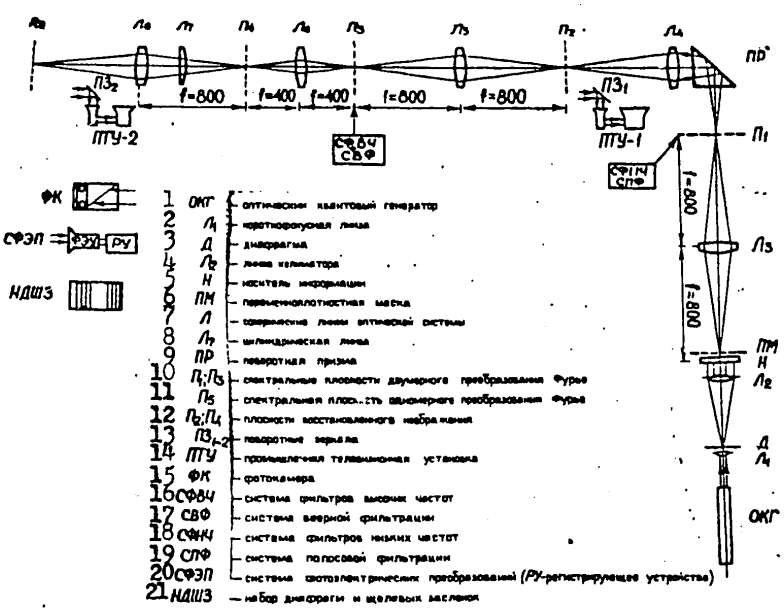

Fig 2. Diagram of laser installation.

Key:

1 - laser
2 - short-focus lens
3 - diaphragm
4 - collimating lens
5 - data carrier
6 - variable density mask
7 - optical system spherical lenses
8 - cylindrical lens
9 - rotary prism
10 - spectral planes of two-dimensional Fourier transform
11 - spectral planes of unidimensional Fourier transform
12 - planes of restored image
13 - rotary mirrors
14 - industrial television set
15 - photographic camera
16 - high pass filter system
17 - fan filtration system
18 - low pass filter system
19 - band-pass filtration system
20 - photoelectrical transformation system (registering device)
21 - set of diaphragms and slit shutters

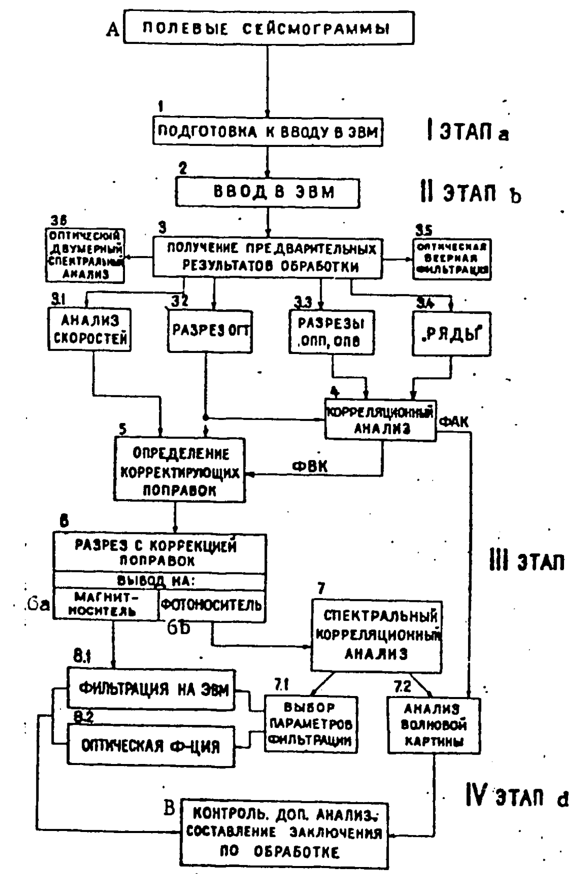

Fig 3. Diagram of complex processing of seismic-survey data.

Key:

A - field seismograms
B - control additional analysis and comparison of conclusions regarding processing
a - Stage I
b - Stage 2
c - Stage 3
d - Stage 4
1 - preparation for input into computer
2 - input into computer
3 - obtaining preliminary results of processing
3.1 - analysis of velocities
3.2 - laser section
3.3 - OPP and OPV [not identified] sections
3.4 - rows
3.5 - optical fan filtration
4 - correlation analysis
5 - determination of corrections
6 - section with corrections, input to
6a - magnetic carrier
6b - photo carrier
7 - spectrum correlation analysis
7.1 - filtration parameters selection
7.2 - wave picture analysis
8.1 - filtration by computer
8.2 - optical filtration

of seismic surveying. In connection with that, and also with the above-noted shortcoming, it is advisable to create hybrid optico-digital processing systems in which the control and logical functions are built into the electronic computer, and the performance of operations of processing large masses of data in the optical processors. Necessary for the realization of such a complex are devices that transform signals form an optical into an electrical form and the reverse, by means of which the optical processor and electronic computers can be combined into a closed processing circuit equipped with the corresponding software.

Such work on the creation of an optico-digital system of automatic data processing by the laser method has been started in the Scientific Production Association "Soyuzgeofizika" in collaboration with other organizations [3,4] on the basis of making up a complex of a Minsk-32 or M-7000 computer with a coherent optical system.

The optico-digital complex, a block diagram of which is presented on Fig 4, includes two main types of exchange between the computer and the coherent optical processor--through photo carriers and through a space-time light modulator or controlled transparency.

The selection of the M-7000 computer (Sm-1 or SM-2) is determined by the fact that according to the plan of the USSR Ministry of Geology it was selected as the basic one for the creation of computer centers of the expeditionary level and the equipment of it with an optical special processor will considerably expand the possibilities of processing seismic and other geophysical materials.

The selection of an analogous optical processor with a coherent light source (laser) is determined by the fact that with relative simplicity of the coherent optical processor a large number of equivalent parallel processing channels is realized, which is determined by the resolution of the optical system and the information carrier used. Thus, for example, during work of the "Kogerent" laser installation with the use of a 24 x 36 mm phototransparency and a resolution of the standard photomaterials used of 100 lines/mm, the equivalent number of parallel channels is of the order of $6 \cdot 10^7$. The coherent optical processor operates with the amplitudes and phases of the luminous field and permits solving a wide range of problems in the processing of two-dimensional complex functions given in the form of a distribution of the amplitudes or phases of the luminous field.

In cases where the dynamic range of processed data does not exceed 40 dB or when there is a possibility of preliminary programmed regulation of a seismic recording on a computer of up to 40 dB, photographic materials are used to connect the coherent optical processor and the computer with the purpose of: a) the readout of data from the computer and, after digital-analog transformation the preparation of a phototransparency on which the seismic information is represented by variation of the amplitude transmission of the transparency; b) the input of information in the

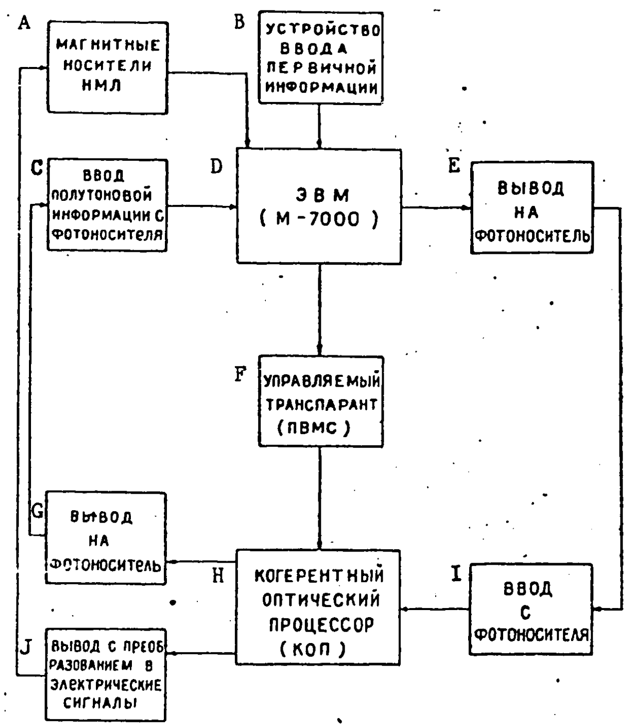

Fig 4. Block diagram of an optico-digital complex for the accelerated processing of geophysical data.

Key:

A - Magnetic carriers
B - Primary data input device
C - Half-tone data input from photocarrier
D - M-7000 computer
E - Output to photocarrier
F - Controlled transparency
G - Output to photocarrier
H - Coherent optical processor
I - Input from photocarrier
J - Output with transformation into electrical signals

coherent optical generator by means of a phototransparency; c) readout of the results of optical processing of seismic data in the form of a phototransparency; d) the input of data from the phototransparency into the computer after analog-digital transformation.

In cases of increase of the dynamic range of the system above 40 dB and for the purpose of reducing the distorting influences unavoidable in the obtaining of phototransparencies, a controlled dynamic transparency is used for data input into the coherent optical processor. The transparency is controlled by a computer with the use of a buffer memory after digital-analog transformation.

Data is read out of the coherent optical processor by a system of the "Vidikon" type with a linear characteristic of the entire plane of the screen, which assures the transmission of 128-256 gradations of brightness with subsequent coding of electrical signals and input through the buffer memory into the computer.

Also possible is a combined method of connection, when input into the coherent optical processor is accomplished by means of the phototransparent, and readout by use of the "Vidikon" system or a system for optical data readout of the "Fotomeyshn" type.

The functions are distributed among the components of the optico-digital complex in the following manner.

By means of the electronic computer and special input-output devices field recordings are introduced, edited and sorted, the velocity characteristics of the medium are determined, as are the input of kinematic and static corrections, summation and the obtaining of laser time profiles.

The operations most time-consuming for electronic computers are accomplished by means of the coherent optical processor: the obtaining of various kinds of unidimensional functions (autocorrelation, mutual and retrocorrelation and current correlograms), band-pass frequency filtration with given filter characteristics, space-time (fan) two-dimensional filtration, reverse filtration by means of filter-holograms, and D-transformations of laser time profiles.

The realization of the above-enumerated algorithms permits conducting kinematic, spectrum and correlation analyses of all seismic routes both before and after summation for the selection of optimum interference systems to improve the signal-to-noise ratio, determination of the velocity characteristics of the medium, and optimum frequency and space-time filtrations (possibly, variable in time and space); obtaining laser time profiles with preliminary deduction of regular wave-noises, band-pass and reverse filtration of initial and summary routes; accomplishing rapid D-transformation of laser time profiles; performing a number of other operations connected with two-dimensional Fourier transform and the obtaining of holograms.

If the M-7000 computer is provided with an electronic special processor and a coherent optical processor, the comparative productivity in the performance of individual operations per unit consisting of 24 seismic routes with a length of 5 seconds can be represented by the following table.

Operations	M-7000 with special electronic processor	M-7000 with coherent optical processor
1. Determination of spectra by routes	13 sec	0.02 sec
2. Determination of two-dimensional spectra	26 sec	0.02 sec
3. Band-pass frequency filtration	14 sec	0.04 sec
4. Reverse filtration	17 sec	3 sec
5. Space-time (fan) filtration)	14 sec	0.04 sec
6. Determination of unidimensional correlation functions	28 sec	4 sec
7. Determination of two-dimensional correlation functions	44 sec	4 sec
8. D-transformation	910 sec	45 sec

The presented data illustrate the advisability of including coherent optical processors in computer complexes.

The economic effect from their application will increase in proportion to the increase of cost only of the digital processing of geophysical (seismic) materials.

A still larger gain is obtained when two-dimensional images of geological information is used, as even the most modern electric computers cannot find room for the volume of information of an entire image in its memory.

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UDC 519.246.2:621.396.98-187

OPTICO-ELECTRONIC SYSTEM OF IMAGE ANALYSIS BASED ON AN OPTICAL CORRELATOR AND ELECTRONIC COMPUTER

Leningrad GOLOGRAFIYA I OPTICHESKAYA OBRABOTKA INFORMATSII V GEOLOGII I GEOFIZIKE (Holography and Optical Data Processing in Geology and Geophysics) in Russian 1979, p 134

[Annotation of article by N. I. Yurga and V. P. Tarasenko from book edited by S. B. Gurevich, Order of Lenin Physico-Technical Institute imeni A. F. Ioffe, Leningrad, 500 copies, 195 pages]

[Text] Annotation

A system is described that is intended for correlation spectrum processing, in particular, of filtration and half-tone images in Fourier and Walsh bases on the basis of M-6000 and YeS computers and an optical correlator, the video signal sensor of which is constructed on the basis of an LI 608 dissector with step scanning and can be changed stepwise from 512 x 512 to 64 x 64 elements. The 8-digit binary code on the output of the analog-digital converter permits quantizing the amplitude of the video signal of a digitized element of an image on 256 levels. A detailed analysis is made of the correlation spectrum properties of images for the purpose of separating the informational parameters of an investigated object on a YeS 1020 (YeS 1030) computer with the use of algorithms of two-dimensional rapid Fourier and Walsh transforms. The possibility of transfer of large volumes of data from the M-6000 to the YeS computer on punched or magnetic tape is envisaged for that purpose.

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ANALYSIS AND INTERPRETATION OF INSTABILITY IN A LIQUID-CRYSTAL MATRIX "WITH A MEMORY"

Leningrad GOLOGRAFIYA I OPTICHESKAYA OBRABOTKA INFORMATSII V GEOLOGII I GEOFIZIKE (Holography and Optical Data Processing in Geology and Geophysics) in Russian 1979, p 153

[Annotation of article by A. B. Beklemishev, V. P. Alampiyev, Ye. M. Makeyeva, A. P. Shevalev and V. V. Nemtsov from book edited by S. B. Gurevich, Order of Lenin Physico-Technical Institute imeni A. F. Ioffe, Leningrad, 500 copies, 195 pages]

[Text] Annotation

In the article an attempt is made to link experimentally observed instability in the electrooptical response of a liquid-crystal matrix "with a memory" with distinctive features of the form of the volt-ampere characteristics of the used composition and fluctuations of the resistivity and thickness of the film of material included in a real device. A resistant type of nonlinearity of the volt-ampere characteristics of liquid-crystal material has been confirmed experimentally, and the correlations between three different statistically probable types of nonlinear and linear characteristics have also been evaluated.

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PUBLICATIONS

COMPUTER TECHNOLOGY OF SOCIALIST COUNTRIES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 p 2

[Annotation from book edited by M. Ye. Rakovskiy, "Statistika" Publishers, 15000 copies]

[Text] Computer technology of socialist countries: a collection of articles under the general editorship of M. Ye. Rakovskiy. issue 5. Moscow: Statistika, 1979, 184 pages with illustrations.

Under the aegis of the Intergovernmental Commission on Cooperation of Socialist Countries in the Field of Computer Technology.

This international collection examines questions of research, development, application and utilization of experience gained with technnical and programming devices of computer technology created in accordance with an agreement on cooperation in the field of computer technology between socialist countries: Bulgaria, Hungary, East Germany, Poland, Cuba, Rumania, Czechoslovakia and the USSR.

The articles in this issue consider various aspects of application of computer hardware: standard applied program packages, operational or planned automated systems, methods for increasing programmer labor productivity, ensuring reliability of computer devices.

The collection is intended for workers employed in the design and utilization of Unified System computer hardware.

[207-8617]

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COMPUTER TECHNOLOGY OF SOCIALIST COUNTRIES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979, signed to press 4 Apr 79 pp 3-4

[Foreword from book edited by M. Ye. Rakovskiy, "Statistika" Publishers, 15000 copies]

[Text] The sudden increase in the production and, in particular, use of modern computer technology in socialist countries demands additional improvement in the efficiency of utilization of these devices in the national economy. Starting in 1973-74, virtually all newly planned automated control systems (ASU) for various links of the national economy are based on equipment and programming devices of the Unified System of Computers and International System of Small Computers (SM) elaborated with cooperation of socialist countries in computer technology. Program compatibility of computer models has, to a significant degree, increased the possibility of program exchange, reduced expenditures in development of systems by shifting to systems with high productivity without requiring conversion of previously used software. At the same time, it became possible to design and develop a fund of applied programs in the form of packages to solve the most common problems in various fields and standard plans of ASU. Expansion of the range of users and experience acquired in using programming devices and hardware also requires the mutual information of all experts involved in the use of unified system computers in order to promulgate advanced experience, avoid duplication of efforts and statement of problems for designers. This should significantly aid in resolving the problem of increased efficiency of use of jointly developed computing devices.

Questions on the use of computer hardware were partially examined in the third edition of the collection "Computer Technology of Socialist Countries" in articles concerning applied program packages (PPP). In view of the importance of the problem of efficient use of computers, the editorial board felt that this issue of the collection should be devoted to this problem.

Various aspects of computer hardware use were considered in the articles: standard applied program packages, operational or planned automated control systems, methods for increasing labor productivity of programmers, guarantying operating reliability of computer hardware, training of users. Reference information can be found at the end of the collection on programming devices developed in various countries, and descriptions of equipment, including the new SM computer devices, information about which is currently inadequate, are also given. This should expand the range of experts interested in this issue. The editorial board hope that the published materials will promote further propagation of experience of efficient use of computers developed in socialist countries.

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USE OF ELECTRONIC COMPUTER TECHNOLOGY IN SOCIALIST COUNTRIES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 1979 pp 5-10

[Article by D. G. Zhimerin, doctor in technical sciences, USSR]

[Text] Electronic computer technology is widely used in all spheres of human activity: in centralized management of industrial processes, control of technological processes, elaboration of plans, statistics and accounting, medical diagnoses, planning of technological processes and in the design and processing of scientific research information, etc. The wide front of use of computer hardware (SVT) requires the rapid accomplishment of a great deal of work, and, therefore, international cooperation in the design of applied program packages (PPP) and their mutual exchange satisfies the interests of countries participating in the elaboration of PPP.

The development of cooperation in the use of electronic computer hardware formed the basis for creating the Council on the Use of Computer Hardware (SPSVT) within the Intergovernmental Commission on Computer Hardware. In order to maintain the continuity of earlier developments, the Council was given the functions and duties of the working groups on ASU and automated design systems (SAPR) (the aforementioned working groups have been abolished). The Intergovernmental Commission on Computer Technology charged the Council with the accomplishment of a unified technical policy and coordination of cooperation of the countries--participants of the Agreement in the field of use of computer technology for efficient utilization of unified system and SM computers in the national economy.

Basic trends of work of SPSVT are as follows:

Defining the most important fields in sectors of the national economy with the use of SVT yields the greatest economy and social effect; cooperation in the preparation and elaboration of future plans and predictions for the use of electronic computer technology;

Elaboration and utilization in the countries of standard systems, planning decisions and applied programs with preliminary experimental verification in the developer country;

Issuance of instructional and methods material, which specify the volume and content of standard systems, planning decisions and applied programs designed within the framework of the Intergovernmental Commission on Computer Technology;

Analysis of requirements imposed by users on computer hardware in various sectors of the national economy and elaboration thereto of requirements for technical and programming devices;

Creation of means for more efficient development of applied programming software using methods of modular, structural and standard programming, as well as automation of work in the field of PPP design;

Elaboration of principles of specialization in the use of object- or problem-oriented systems based on interests, possibilities and experience of the countries;

Development of proposals for realization of the principles of exchange of applied program packages and plans of standard systems adopted by the Intergovernmental Commission on Computer Technology.

The SPSVT operates in conformity with the Conclusion on the Council affirmed by the 28th session of the Intergovernmental Commission and the Unified Plan of Cooperation in the use of computers and the International System of Small Computers.

The Unified Plan of Cooperation contains 140 positions. The plan is continuously being supplemented; for example, at the 2nd session of the Council, the Cuban delegation proposed including in the plan the development of programming packages for control of the sugar industry.

In order to accomplish the problems entrusted to the Council, at the 1st session of the Council it was acknowledged as advisable to assign the organization and coordination of work accomplished in the Unified Plan to the national sections of the Council. Thus, each national section of the SPSVT is responsible for several sections in the Unified Plan of Cooperation: for example, Bulgaria organizes, coordinates and manages development of PPP for calculation of beam, frame and bridge structures; Hungary is responsible for elaboration of programs for accounting, systems analysis and operating efficiency of computers and computing centers; East Germany is responsible for the development of PPP entitled "System of Data Base Management" DBS/R-OS; the USSR is responsible for development of PPP for on-line control of primary production of a machine construction enterprise; Czechoslovakia is responsible for development of PPP for technical preparation of production. This means that a responsible country organizes international cooperation for development of a specific programming device and, by agreement with the participant countries, confirms the technical assignment for work, the technical plan and the testing program. It bears responsibility to the Council for the timeliness and quality of development.

The Council may set up temporary working groups to accomplish some work in the overall plan which cease their existence after completing their assignments.

The basic problem of the national sections of the SPSVT at a given moment is the organization of work supervision for which they are responsible. At the same time, they must determine the work to be done in the period from 1981 through 1986. Development of methodological materials on organizational and economic ASU and SAPR should be basically completed in 1978-1980. Primary attention should be given to the creation of packages of applied programs and standard systems.

In conformity with the primary assignments on the problem of automated design systems defined at the 12th session of the Intergovernmental Commission on Computer Technology, the basic trends of cooperation were spelled out:

Creation of automated design systems in machine construction for manufacture of parts and assemblies of machinery, technology of machine construction;

Creation of SAPR in construction and energy;

Creation of SAPR in instrument construction, electrical technology and electronics;

Determination of SAPR most important and effective for use in the national economy of socialist countries;

Elaboration of technical requirements for technical devices and general programming software.

Organizational and methods foundations have been developed for the creation of SAPR under conditions of multilateral cooperation.

Out of the 28 methods materials on general systems questions of SAPR design which were at the disposal of the participant countries, the following should be mentioned:

Methods indications for the use in planning of PPP of automated drafting;

Recommendations on the use in SAPR of existing systems of data base management;

Technical requirements for special technical hardware and devices being designed in the Unified System and International System of Small Computers for use in SAPR;

Technical requirements for adaptation of existing data bases and development of specialized ones for SAPR, dialogue systems, automated programming systems, programming software for solving problems of computer graphics.

In the development of systems, applied programs and standard documentation there are 137 organizations participating from Bulgaria, Hungary, East Germany, Poland, Rumania, the Soviet Union and Czechoslovakia, with the following breakdown: Bulgaria 17, Hungary 17, East Germany 20, Poland 25, Rumania 4, USSR 43, and Czechoslovakia 11.

In 1978 testing was conducted on two PPP designed for analysis of electronic circuits which were developed by Hungary, as well as four PPP designed for planning and technological preparation of production of electronic units and hybrid film microcircuits, instruments of industrial monitoring and control, single and double-sided printed circuit boards developed by the Soviet Union.

In 1980 it is planned to design 13 automated planning systems (including 4 for planning facilities of machine construction and 9 for planning facilities of instrument construction, electrical technology and electronics), 17 applied programs for automated planning and 20 standards documents, monitors and input languages. Among these, we might mention:

Planning system of technological processes of manufacture for parts in the shape of bodies of rotation;

A system for planning and preparation of production of analog and digital electronic devices;

PPP for design calculations of geared transmissions;

PPP for planning electrical control circuits for technological equipment;

PPP for planning beam and frame bridge structures;

PPP for planning pipelines for electrical power plants;

PPP for analysis and parametric optimization of linear and nonlinear electronic circuits;

PPP for planning asynchronous electric motors;

Input languages of SAPR in machine construction to describe engineering and technical problems and to solve design problems;

The typical composition of base configurations of technical hardware and the overall programming software of SAPR of various levels, etc.

Experts from Bulgaria, Hungary, East Germany, Poland, Rumania, the Soviet Union and Czechoslovakia have determined the sectors in which SAPR can be most efficiently used. These sectors are as follows: radio electronics and electrotechnics, machine construction, construction, chemical industry, light industry and instrument construction. In this connection, a great deal of work must be done to create standard subroutines and components of SAPR designed for use in these sectors. Standard subroutines and components by 1980 will primarily be available for radio electronics and construction, sectors where standard decisions have been most successfully elaborated.

The joint development of programming devices in the field of organization and economic systems of data processing for specific sectors has been conducted since 1969. Users may receive from the joint program base such packets as "Package of applied programs for planning requirements" which envisages solution of problems of determining requirements of production for parts, assembly units, purchased items and materials necessary to accomplish the plan of goods production, and also analysis of startup periods of parts production, output of orders for purchased items and materials, etc. (the package was developed by Bulgaria and the Soviet Union); "Methods of optimization" (developed by East Germany); "Generator of data base processing programs" which executes basic functions on data processing (program developed by Poland); "Package of applied programs of technical preparation of production" (developed by Czechoslovakia); "Package of applied programs on economic statistics" (developed by Hungary).

The Unified Plan of Cooperation for 1978-1980 envisages preparation of PPP on systems control of data bases and production quality, elaboration of information software as well as the creation of PPP of multiple level ASU of machine construction enterprises, PPP for control of instrument management, etc.

The Council on the Use of SVT is faced with developing work on cooperation in the field of designing organizational and economic systems in such sectors as agriculture, construction, mining, communal management, etc.

One of the efficient directions of computer use which is being developed at a rapid rate is the design of automated systems for the control of technological processes and production (ASUTP). The chief goal of incorporating ASUTP is improvement of the technical and economic indicators of the controlled system, i.e., to enhance productivity of equipment, economize raw materials, materials and energy carriers, improve quality indicators of the product and, in consequence, to enhance labor productivity. The efficiency of these systems can be judged by the following examples.

Implementation of ASUTP in clinker leaching in an alumina combine with overall expenditures for creating and fitting a 200,000 ruble system yields an annual savings of over 200,000 rubles, especially because of a 1700-ton increase in alumina output, 3800-ton increase in output of soda products, and economy in thermal energy and reduction in the number of service staff.

The use of an automated system for control of bioluminescence by means of optimization of technological processes guarantees an increase in equipment productivity of 1%, an increase in the output of annual rolling by 0.5% and reduction of fuel consumption in the heater sumps by 2%. The annual economic effect is 1,700,000 rubles with expenditures of 3,500,000 rubles for creation of ASUTP.

A system for control of mine transport equipment in open-pit mines, because of better on-line distribution of dump trucks in the excavators and continuous monitoring of dump truck loads raises the coefficient of utilization of vehicular transport by 7 to 10% and yields an annual economic effect averaging about 700,000 rubles, which permits payback of all expenditures for creation of the system in 6 months.

A similar system incorporated in open coal pits permits an increase in coal yield in active capacities by 4 to 5%.

The greatest success in incorporating ASUTP was achieved by sectors of heavy industry--energy, chemistry, ferrous and nonferrous metallurgy, etc.

For automation of technological processes a series of International System of Small Computers was created. The use of microcomputers will greatly expand the range of application of computer technology--on their basis will be created systems for control of small and medium plants, local systems of control for complex analytical devices.

More complex automated control systems can be created on the basis of distributed networks of microcomputers whose action will be coordinated by a central computer.

In 1981-1990 heavy industry will shift from automatically controlled technical processes to automated processes, where man does not participate in control, while the system controls processes beginning with feed of initial materials to warehousing or unloading of the ready product.

In the same period work on the creation of ASUTP in machine construction and other sectors of industry will be expanded on a wider scale.

The wide range of work on the creation of ASUTP will require research to be done in the development of automated systems of ASUTP planning.

The rapid development of automation of technology and industrial processes requires the combined efforts of socialist countries. The most urgent directions of scientific and technical cooperation are the following: matching methods, standard materials and standards for basic components of systems design or the system as a whole; development of ASUTP hardware; creation of efficient algorithms for control of technological processes and programming devices for their realization; development of standard systems for specific groups of technological processes.

For preparation of proposals on cooperation in ASUTP and elaboration of concrete plans, a Temporary Working Group on ASUTP was formed at the 2nd session of the Council.

The use of electronic computer technology for automation of planning and design, creation of automated systems of management of organization and economic and technological processes has several general methodological questions whose elaboration within the international collaboration was entrusted to the Section on General Systems and Methodological Questions for the use of SVT.

Mutual exchange of programming devices, multilateral cooperation in their development, a continuous state of information on the use of PPP form the necessary prerequisites for enhancing the efficiency of cooperation in the use of computer technology.

[207-8617]

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DIALOGUE SECTOR INFORMATION SYSTEM BASED ON THE YES-1040

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 1979 pp 11-19

[Excerpts from article by P. Braun, G. Hornjak and Z. Pasztor, Hungary]

[Excerpt] The experimental use of information systems considered in this article began in September 1976 with the incorporation of a system of remote data processing [1].

In elaborating the system, which operates upon user interrogations, in addition to the simplicity of inquiries, a major requirement was standardization of interconnections between the inquiry system and the data banks servicing it. The essence of the latter requirement consists in the fact that with maintenance of existing operating conditions data are transmitted from the banks in a standardized form for remote data processing, i.e., the data are displayed on a screen.

In the system it is possible for standardized access with banks of different contents (economics, energy) and different structure, and it is also possible to supply users with information tables of general interest. The user works with the tables according to preset rules.

Program of Preparation and Organization of Dialogue

The load and systematic actualization of the data bank is done by means of a special language of table definition using a communications program. A temporary connection between the data banks (it is an offline type for the system) makes it possible to perform local data processing only; system requirement for a power source occurs within a relatively short period of load and actualization.

The smallest capacity of RAM is necessary for the resident portion of the inquiry system using the VTAM access method. The system only occupies a large portion of the memory when the terminals are activated, i.e., upon interrogation, using the roll-out procedure in the MVT operating system. After the interrogation cycle, the occupied region of RAM is freed, and a roll-in function is used to restore the temporarily suspended processing.

The YES-1040 electronic computer works with the OSMVT operating system. Connected to the multiplex channel of the computer is a programmed control device for data transmission (type VT-55 000) designed on the basis of the YES-1010 computer and a CCA interface (developed by the "Videoton" enterprise. Asynchronous, linear communications devices CLA of the YES-1010 computer guarantee communication at a rate of 1200 baud along commutated communication lines. The terminals are type VT-340 displays and microprocessor displays type VTS-56100, which carry out the functions of the AP-70. Both kinds of devices were developed by the Videoton enterprise. A matrix dot printer as well as a tape reader and puncher can be connected to the VTS-56100 displays.

The program of the VT-55 000 device which guarantees control of communications lines and terminals creates a unified homogeneous system connected to the YES-1040 computers from the "point-point", "station-station" and "multistation" links and the physical network containing VT-340 and VTS-56100 terminals.

The CCA device necessary for creation of the system and the program of the supervisor which accomplishes control of the emulator in the data transmission control device were developed at the Institute of the Videoton enterprise. The program emulator [2] was built at the VYEIKI computing center.

Systems testing has been completed, and it is now available to users for 2 hours per day. Updating of interrogated information is done daily.

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MICROPROCESSOR DATA PROCESSING SYSTEM FOR FORMATION OF ROLLING STOCK AT SHUNTING STATIONS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 19-26

[Excerpts from article by Cs. Hazay (Hungary)]

[Excerpts]

The efficient operation of a shunting station has a significant effect on car turnaround, better utilization and, consequently, an increase in the available car park.

The computer system developed by the Institute of Computer Technology, by order of the Ministry of Railroad Transportation of the Hungarian Peoples Republic, should relieve maintenance personnel from nonproductive work, eliminate operate error and, furthermore, provide management of the shunting station with information on the flow of the technological process.

The handling capacity of the processor is 250 symbols per second; it can service a maximum of 16 operators. A rather simple keyboard display containing only buttons and indicators may be used with the processor memory.

The processor memory, after shaping the message (32 symbols long), sends it as an interrupt request to the processor. As a result, for the processor this reduces the need for program exchange to 1/32.

One of the advantages of a two-processor system is that the processors may monitor the operation of one another, and in the event of error, the properly operating processor may display information which facilitates error correction.

The use of microprogramming requires that interfaces with peripheral devices, functioning under the control of the processor, transmit data independent of the processor under autonomous conditions with direct access to memory through the specified resident buffer regions. Instead of a problem awaiting termination of operation of peripheral devices, the physical processor may be loaded with a program that can be run at this time. Interfaces with peripheral devices are special processors of a multiprocessor system. Upon reception of an instruction, they must independently perform data exchange.

Construction of the MAV-51 System. The system (Figure 1) is oriented toward manual input as well as to output into paper printers. Data are reproduced with the aid of a 132-position printer. By means of an 80-position printer, operator instructions and error reports are fixed. The shunting station communicates with neighboring shunting stations by means of Telex.

The system mainly consists of electromechanical peripheral devices of the Unified System (YES) of Computers. This is a guarantee for its realization. The peripheral printer outputs interface with the central processor via a "small interface."

The central processor of the system (Figure 2) is a dual processor device constructed of modules of the IKVT microcomputer (Institute of Coordination of Computer Technology).

The processors consist of modules of the M-51 microcomputer with a word length of 16 bytes. The modules are connected by a duplex line system. Communication between modules occurs under "master-slave" conditions. The module accessing the main line system receives its control through a priority system in order of sequence. After receiving control of address output to the main line, another module is selected for participation in control. The system of main lines thus can control not only the module of the central processor, but also the modules of interface with peripheral devices.

Peripheral device interface modules can exchange data independent of the processor using direct memory access. It is natural that the parameters required for exchange are received by the module from the module processor. Let us examine the function of the basic module.

Processor Module. It consists of a microprocessor (word length 16 bytes, 42 instructions, negative numbers represented in auxiliary code, operations with fixed decimal, four register-accumulators, magazine register for 16 levels, possibility of direct addressation, four methods of addressation) with the integrated circuits of the clock generator necessary for it and interrupt service. The processor has access to most of the main lines. The access circuits to one main line are situated inside the module. Circuits required for access to other main lines must be placed on a separate main line.

PZU/OZU Module. One module stores two K words ROM and two K words RAM. The four K word memory built into the module using a special field may be built in K word blocks in any addressable region K words long.

Main Storage Module. One module permits realization of read-write memory with a maximum of four K words. The location of the built-in region (four K words) may be changed as desired.

Console Module. This module is optional for system operation and may be used as an auxiliary device for servicing and debugging programs. The module contains not only ICs necessary for servicing, but also performs ordinary service functions for the minicomputer. The latter performs the built-in ROM console program. For loading programs, a punched tape reader may be connected to the console.

Small Interface. The module can perform interfacing of two peripheral input devices and two output devices. The module contains microprogramming control device. The microprogram cycle is about 1 microsecond. The module controls slow peripheral devices and thus the programs which service the coupling devices periodically replace each other in the control device.

Disk Coupling Module. The module also contains a microprogramming control device. The microprogramming cycle determined by the rate of transmission from the disk is 180 nanoseconds. With the aid of the module, as many as two YES-5060 devices can be connected to the microcomputer.

Keyboard-Signal Panel Coupling. Coupling is done with the aid of a pair of modules, one of which renews information on screens of up to eight 32-position signal panels. Renewal is done through the main circuits with direct memory access. The other module couples a maximum of eight keyboards, generating sign-by-sign interrupt requests. Data exchange occurs with the aid of the keyboard-signal panels separately for each device with binary frequency coding.

Main-Main Coupling. With the aid of this module, the main circuits are mutually accessible for the processor: one module receives information about the address from the processor module and exchanges data through the main circuit related to the other processor.

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SYSTEM OF PROGRAMS AND HARDWARE FOR MONITORING DIGITAL CIRCUITS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKY STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 27-36

[Excerpts from article by D. M. Grobman, B. G. Sergeyev and Ye. N. Filinov]

[Excerpt]

The use of integrated circuits has clearly simplified the problem of planning and manufacturing computer technology devices (VT), increased their speed and reliability. However, the problem of testing removable units which primarily represent rather large and complex digital circuits has been greatly complicated.

Below are described the structure and basic technical decisions of automated monitoring systems (ASK) developed at the Institute of Electronic Control Computers. The ASK considered primarily solves problems of logic monitoring of digital component units (BE) and consists of program packages (for the M-4030 computer) which automate the process of test synthesis, at a complex of equipment for automation of circuit testing.

ASK Program System

System Structure: The main problem which is solved with the aid of ASK program is the construction of diagnostic tests for digital circuits which are designed to detect and localize isolated constant errors. Selection of this class of failure is explained by the fact that they are most likely, and because the tests which verify isolated failures technically detect their multiples.

There are three basic approaches to resolving the problem of test synthesis:

Manual compilation of tests with subsequent verification of their validity and completeness;

Automated construction of random tests;

Regular automated construction of tests.

Unfortunately, none of these methods assures the successful resolution of the problem within an acceptable time. Therefore, all programs realizing these methods are combined in a unified automated system of test synthesis (ASST).

Conclusion. The ASK described above was put into operation in sections as it was developed. All ASST programs and the test complex underwent practical testing, including the functional monitoring device, processor, logic signal discriminator, and punched tape program master.

The ASK was used to synthesize tests, monitor and debug component units of first phase SM computers.

Analysis of the results of prototype ASST operation showed that in the M-4030 computer with a memory capacity of 256 kbytes, circuits can be simulated which contain up to 4000 gates to study the efficiency of tests. Construction of random tests and diagnostic lexicons is done for circuits consisting of 2000 to 3000 gates, regular construction of tests for circuits whose number of gates does not exceed a thousand and where there are no delay elements. It is worth noting that with an increase in circuit dimensions, machine time for simulation increases linearly, which in the construction of tests and lexicons is a faster increase than the square of the number of gates. This limits the possibility of ASST.

The limits of the currently used configuration of the test complex is the number of communication channels with the control object (no more than 192). However, the structure of the complex foresees the possibility of a virtually unlimited increase in their number.

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AUTOMATED CONTROL SYSTEM BASED ON THE YES-1032 COMPUTER

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 5, 1979 signed to press 4 Apr 79 pp 37-43

[Excerpts from article by W. Baranek, K. Wohtyniak, G. Pilko and M. Perchel, Poland]

[Excerpts]

The Mera-El'zab computer plant, for which the system described below was developed, appears in the makeup of the Mera Association. The plant produces the following peripheral computer devices: perforators, perforator-reader complexes and screen consoles.

Nature is medium mass production with a large number of modifications and new items. The production arrangement system is nested with specified technological mass production lines, for example, production of electronics boards.

Production involves great material expenditures and an average variety of consumable materials.

The plant card file of material indices contains about 30,000 items.

The plant has accumulated a great deal of experience in technical preparation of production and output of documents, materiel management, planning at different levels, etc. Information was rewritten from the documents onto punch cards and was loaded by a reader into disk memory, making it possible to achieve a certain level of automation of production. However, with the increase in the number of control subsystems, problems arose which were related to the lack of integration of these subsystems, the abrupt increase in the amount of preparation of computer information carriers. It was decided to construct a new system based on screen consoles of local manufacture. A configuration was elaborated for a local computer which is shown in Figure 1. Programming software of this system included the Unified System Disk Operating System, Control System of Conditions with Time-Sharing and User Program.

In the local computing system, the maximum distance from the screen console Mera-7910 to the control device Mera-7902 is equal to 600 meters. At greater distances a remote system should be used.

Technical Preparation of Production

Subsystem of Material Management. Subsystem of Item Sale. Subsystem of Personnel (Labor and Wages). The system described has been used at the Mer-El'zab computer plant for about one and one-half years.

Functional reliability of the computing center is determined by the formula

$$P = \frac{T_{EO}}{T_{EO} + T_{ORG} + T_{EM}} \times 100,$$

where P equals functional reliability of the computing center, in percents; T_{EO} is effective operating time; T_{ORG} is organizational downtime; T_{EM} is emergency downtime.

The average magnitude of reliable operation of the computing center P_{AVG} in the course of a week is 91%.

Conclusion. The system described above yields an incomparably greater effect than the system using the loading method. Efficiency of system operation was enhanced because of optimum configuration and programming software which makes it possible to integrate the subsystems required to realize the formulated goal.

Based on the needs of the plant, the system used has the following configuration: operative memory 512 kbytes; six magnetic tape memory control device; disk memory with total capacity of 240 Mbytes; one punched card reader; two automated digital control panels; a control device with 32 screen consoles and 12 mosaic printers.

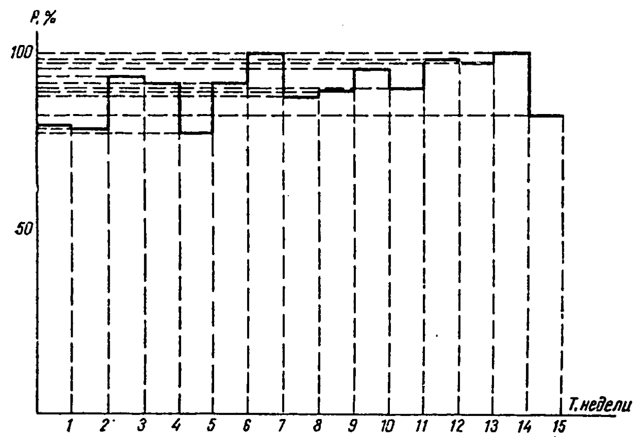

Figure 6. Graph of Reliability of Computing Center

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SYSTEM OF CALENDAR PLANNING OF MINI-TYPE PRODUCTION

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79, pp 43-50

[Excerpts from article by I. Molnar, Hungary]

[Excerpts]

The Calendar Planning System of Production (SKP) is the commercial name of the MINITIP system developed to control small enterprises engaged in the manufacture of parts and assembly of end products under shop conditions. The system is primarily used in machine construction, electrical and electronics industries. In these areas it may be proposed to enterprises which manufacture products costing 0.5 to 1×10^9 forints. In Hungary positive results have been obtained in the use of the system in planning production of automobile and reinforcement parts (for example, production of bumpers). According to provisional estimates, expenditures for introduction of the system including capital investments and expenditures for organizational improvement are payed back in 3 to 4 years because of more efficient utilization of resources necessary for production.

The system can be successfully used at enterprises which do not perform data processing by computer, i.e., have no great experience in using computer technology devices. At these enterprises the use of computer technology should be begun after resolving individual subtasks.

SKP is a system of modular structure which operates using a central data bank (Figure 1).

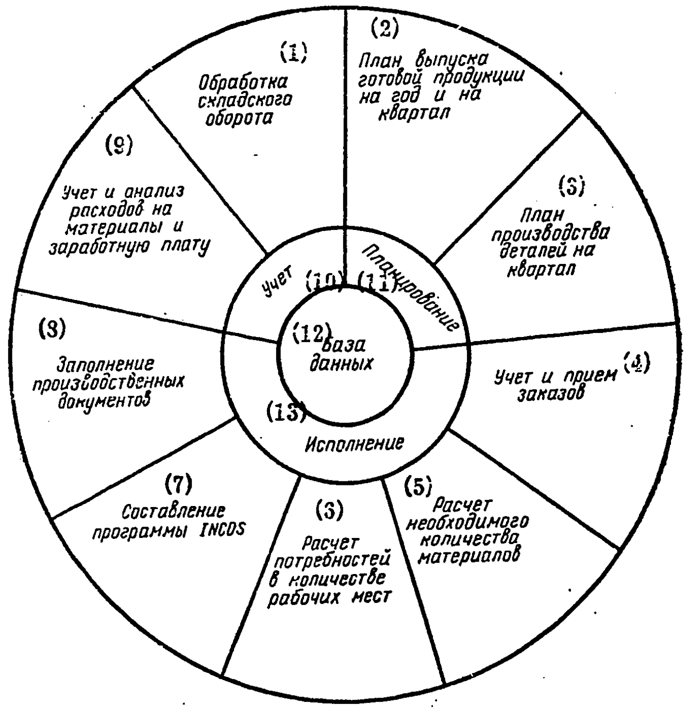

Figure 1. Structure of Calendar Production Planning System MINITIP

[KEY: 1 - Processing of warehouse turnaround; 2 - Plan of manufacture of ready products per year and per quarter; 3 - Plan of production of items per quarter; 4 - Accounting and reception of orders; 5 - Calculation of necessary quantity of materials; 6 - Calculation of needs for work areas; 7 - Composition of INCOS program; 8 - Completion of industrial documents; 9 - Accounting and analysis of expenditures for materials and wages; 10 - Accounting; 11 - Planning; 12 - Data base; 13 - Execution.]

The minimum configuration of SKP considered in elaborating the program package contains: a central processor (YES-2012), magnetic disk memory (YES-5052), a card punching station (YES-6122, YES-7191), and an alphanumeric printer (YES-7184).

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DATA BASE CONTROL SYSTEM DBS/R FOR SUBSYSTEMS OF THE COMPLEX "WORK FORCE"

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 50-63

[Excerpt from article by Ju. Bittner and M. Günther, East Germany]

[Excerpt]

The goal of elaborating a complex of subsystems is to create means for satisfying the larger part of intra-plant and extra-plant needs for information which arise in calculating wages and in planning the number of workers, amount of work time and wage fund. The solution of these problems requires numerous analyses (patient statistics, norms statistics, wage fund analysis) and overburdens the Division of Personnel, Social Welfare and other enterprise divisions as well as organs of inter-agency level with routine work.

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AUTOMATION OF PRODUCTION OF PROGRAMS OF THE INTERNATIONAL SYSTEM OF SMALL COMPUTERS USING LARGE AND SMALL COMPUTERS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79, pp 64-73

[Excerpt from article by A. A. Stognyy, I. V. Vel'bitskyy and V. P. Klimenko]

[Excerpts]

Problems of programming and enhancing labor productivity of programmers are mainly resolved in two directions:

Creation of good problem-oriented language;

Development of good programming technology, i.e., creation of methods and means which determine high occupational culture of programming.

At the Institute of Cybernetics of the Ukrainian Academy of Sciences a third path has been proposed for resolving these problems. It consists of redefining the principles of data processing in the computer itself. Analysis conducted at the Institute on problems of programming showed that the problems in programming are due not so much to poor algorithmic languages or poor programming technology, as they are to poor principles of data processing in the computer itself. These principles are obsolete and have ceased to correspond to the information being processed in a modern computer. The basic distinctive feature of this information is its large volume and complicated hierarchical structure.

A primary shortcoming in current computers, we feel, is that the process of digital data processing is organized so that there is no direct relationship between the data and the programming which processes them (the relationship between them is not explicit, and is through man).

In the proposed approach to processing digital information, the interface between data and the program which processes them is made on a somewhat different plane [3,4]. The logic arrangement of the program is combined with the logic structure of the data, and the functions of processing of the corresponding structures are specified individually. To describe (assign) the logic arrangement of the program and data, it is proposed to use the most familiar and evident language--the language of weighted oriented graphs (in contrast to currently used procedurally oriented programming languages, various metalanguages of the Bekusov-Naurovskiy form, stack automatons, etc.). The logic structure of the data is set in these graphs by recording on arcs or symbols or some predicates which characterize certain properties of the data. The logic arrangement of the program is determined by recording on arcs of the corresponding linear statements of the type assignment statement and procedure statement. Therefore, any route in this graph determines the permissible sequence of input data and the corresponding sequence of statements for their processing. If the information being processed does not correspond to the logic structure of the data assigned by said graph, the processing of this information is blocked by definition. The program described in this approach does care what kind of data it processes.

This principle of digital data processing corresponds with a computer arbitrarily called a R-computer. The general scheme of its operation is as follows. Data to be processed is fed symbol by symbol through an input device to the control device of the R-computer (in contrast to ordinary computers in which the data to be processed is fed through the input device into computer memory). The program of the S-computer assigned the order of sequence of symbols in the data to be processed and performance of the corresponding actions for each of them. If this order does not correspond to the actual sequence of symbols in the data to be processed, for example, because of errors, the R-computer, in contrast to an ordinary computer, stops or shifts to a special program of error elimination in input data.

With this approach to the processing of digital data, the technology for manufacturing programs for the R-computer is altered. This technology is called R-programming technology. The process of programming in R-technology is clearly divided into two stages. In the first stage the structure of the data to be processed is formally defined independent of any algorithm for subsequent processing. In contrast to current practice in R-technology, before planning the data processing algorithm, a formal definition of this data is made. Then all operations in R-technology are evolved with respect to this formal definition of data to be processed.

For automation of operations in R-technology, the Institute of Cybernetics of the Ukrainian Academy of Sciences (Kiev) manufactured a technological programmer complex RTK for the Unified System of Computers which is oriented for systems and applied programmers. The most effective use of RTA application in problems of processing textual information. Related to this class of problems are problems of construction of translators from universal and problem-oriented languages and hardware languages:

operating systems, automated control systems (ASU), automated planning systems (SAPR), applied program packages (PPP), data base interface language, information retrieval systems, etc. Examples of specific work performed in R-technology using the RTK technological complexes are translators from procedurally oriented languages Fortran, Basic, Pascal, about ten Assemblers and problem-oriented languages, automated system of microprocessor programming, automated system of accounting of vacant and occupied separate quarters of the city of Yerevan based on the SUBD BANK and RTK disk operating system of the Unified System, system of automation of editing work (RTK OS YES), programming support of language interface VTSKP (RTK OS YES), etc.; and the list goes on. RTK has now been requested by over 200 organizations, mainly users of the Unified System of Computers. The total volume of mathematical software produced in R-technology and incorporated into industrial operation is at least 30,000 instructions. Experience in performing these operations shows that productivity of labor of the programming team increases at least by a factor of two to three. Assimilation of R-technology and technological complexes RTK requires from two or three weeks to two months.

Documentation for the RTK YES computers is supplied in an established order by letter of the interested organization to the Institute of Cybernetics of the Ukrainian Academy of Sciences (Kiev, 252207).

R-technology and RTK programmer technology complexes for automation of production of programs of the International System of Small Computers using large and small computers may be applied in three directions. First of all, technological programmer complexes RTK of the Unified System of Computers may already be effectively used to produce programs of the International System of Small Computers. In the course of performing specific operations, the complexes may be changed since the RTK complexes are produced by "submersion" into the corresponding operating systems. As a result, this eliminates duplication of operating subsystems and the professional programmer can enjoy the service of the operating system without any substantial constraints. The RTK in essence is an expansion of the operating system which is oriented to the production of programs in new technology. RTK maintains continuity with existing programming software, both general and special, and gives the user the possibility to operate in any language available to the corresponding operating system. The user may describe his subject region and thereby develop the RTK in any programming language, whose translator is connected to the computer operating system.

Second, for production of programs in R-technology for the International System of Small Computers operating in the technological process and facility control loop, a special processor can be produced and on its basis, a problem-oriented complex of program production. This trend is particularly effective for programming microprocesses which will be used to construct the International System of Small Computers and be directly built into control loops. This direction should be realized on the basis of experience gained in constructing computers of the "MIR" series and interactive methods of program production for them.

Third, all mass produced models of the International System of Computers should be fitted with instruments for operation in R-technology. For this purpose, the operating system of the Internal System of Small Computers delivered to the user should contain technological programmer complexes RTK SM EVM. In the provided documentation, in addition to user instructions, there should also be the corresponding method materials in R-technology. And finally it is advisable to realize the RTK metasystem in all SM computers produced. Expenditures for its manufacture are small; however, this system will make it possible to greatly resolve the problem of algorithmic language for mass users of the SM computers. This problem is particularly important for small computers since the regions of their application and the contingent of users most rapidly changes and is less predefined. Because of this additional work, users can themselves operatively create the required input language based on specific conditions under which the SM computer operates. The input language will be sequentially evolved according to changes in needs.

Therefore, a typical feature of the modern stage of evolution of computer technology is an increase in the role of small computers which could be operatively built in to various control loops. The tremendous user market of these computers, the attraction to their operation of a large number of nonprofessional programmers almost completely precludes the traditional approach to the manufacture of programs for them. New programming devices on one hand should be rather simple for assimilation by the mass user, and on the other hand should be rather powerful for possible organization of special combinations for production of efficient applied program packages. These devices may be effectively built on the basis of SM computers, MIR series computers and the R-technology of programming described in this article.

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STRUCTURE OF PROGRAMMING SOFTWARE OF CONTROL COMPUTER COMPLEXES OF THE INTERNATIONAL SYSTEM OF SMALL COMPUTERS WITH MAIN CIRCUIT STRUCTURE

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 73-78

[Excerpt from article by B. N. Naumov, Ye. N. Filinov and V. P. Semik]

[Excerpts]

Programming software of control computer complexes established on the base of hardware of the International System of Small Computers (SM EVM) [1] differs greatly from the programming software of YES EVM, as a result of the technical features of the SM computers and the field of application of small computers.

The following items must be taken into account in elaborating programming software for small computers:

Limitation of computer resources (small word length, limited volume of main memory, etc.);

Use of computers to control technological processes in real-time scale;

Use of computers directly in control facility;

User operation with this system under dialogue conditions generally without intermediaries (operators and systems programmers);

Wide selection of peripheral devices (commmunication devices, assemblers, memories, and data displays, etc.);

Wide range of fields of application, broad spectrum of solvable problems; orientation mainly for problems of moderate complexity.

Requirements imposed on technical and programming devices of SM computers, the basic ones of which are the latitude of spheres of application, high operating efficiency at low cost of manufacture, make the realization of the principle of rational combination of universality and specialization extremely vital [2]. For complexes of SM computers with main circuit structure [3] the solution of this problem is greatly facilitated because the architecture of these complexes provides for the creation of efficient systems of functional separation (SRF) by connecting syntactic and semantic expanders--specialized processors which provide simultaneous execution of varied functions.

Programming devices of the SM computers have been elaborated in stages. The programming software system (SPO) supplied with the first serial models includes:

Punched tape and disk operating systems designed for elaboration, debugging and development of programming software and execution of programs under single program conditions;

Real-time punch tape and disk operating systems designed for execution of programs under multiprogram conditions (up to 128 simultaneously executed problems) in a real-time scale;

Program packages for solving scientific and technical problems and data processing by methods of mathematical statistics.

When working with hardware of minimal configuration, programming systems in Assembler and independent dialogue systems with input languages of the Basic type are used to solve computing problems and for operation with peripheral equipment. The macro language and Fortran-IV is used in disk configurations.

The next stage in the elaboration of SPO of SM computers is the creation by the efforts of all countries--participants of the agreement--of an expanded set of operating systems and applied program packages. At this stage the following operating systems have been created:

A disk background-operating base system of one user designed for solving real-time high priority problems under operating conditions and preparation of programs and data processing under background conditions. Under background conditions the system assures preparation of programs in Assembler, macro language, Fortran-IV and dialogue languages.

The basic purpose of the system is to create problem-oriented complexes based on newer models of the SM computers for control of laboratory equipment, test installations, control of scientific experiments, automation of monitoring and measurement, etc.;

A generator of multiprogram operating systems with a large number of priority levels (up to 250) for various hardware configurations (both disk and non-disk) and a wide selection of systems functions.

Among the operating systems generated may be included programming systems in Assembler, macro language, Fortran-IV, and Fortran expanded for solving real-time problems in dialogue languages and in COBOL.

Generated operating systems can assure operation of a broad spectrum of problem-oriented complexes including those designed for control of complex technological processes and facilities, automated planning, etc.;

A disk dialogue multiconsole operating system with time-sharing oriented for solution of information problems and control of data bases.

The system is designed for utilization in automated systems of organizational management, in systems of experiment control, systems of automated planning, data processing of an economic nature and other systems where assembly, storage and processing of data are required under conditions of collective access to the data bases of many users from different terminals including remote terminals.

The systems provides users with a wide range of possibilities including the following:

Creation and management of data bases on disks of a hierarchical dendritic structure (total volume up to 200 megabytes);

Elaboration, debugging and execution of programs in high-level dialogue language oriented toward processing of line data;

Simultaneous sanctioned access to data bases of many users (up to 40);

Interconnection between user problems;

Organization of distributed data bases in multicomputer complexes;

Simple communication with a wide set of external devices included in the nomenclature of SM computer hardware;

A time-sharing disk operating system designed for preparation and debugging of programs in expanded basic language and performance of scientific and technical calculations under conditions of collective use.

The system may be used in problem-oriented complexes designed to solve accounting and statistics and scientific and technical problems, in instructional systems, etc.;

A test monitoring operating system which facilitates the process of debugging, error search and performance of technical maintenance of control computing complexes.

In addition to the enumerated operating systems, a set of applied program packages has been developed which realizes the most prevalent methods of logical and mathematical data processing, as well as program packages which implement technological functions.

Logical mathematical packages execute the following:

Interpolation, approximation and smoothing;

Solution of systems of linear algebraic equations;

Operations on matrices;

Analysis of eigenvalues;

Data processing by methods of mathematical statistics;

Numerical solution of differential equations;

Numerical integration;

Calculation of special functions;

Solution of the general problem of linear programming;

Solution of the transportation problem;

Solution of the one-dimensional problem of integer programming;

Solution of problems of grid planning, etc.

The technological packages include the following:

A package of programming modules which expands the resources of basic operating systems for remote data processing;

A computer graphics package;

A data base management package.

Problem-oriented packages are created on the base of operating systems and procedurally oriented packages, including the following:

Simulation program packages of continuous, discrete and continuous-discrete processes;

Program packages oriented to the solution of economics problems;

Programs packages for data processing in automated lab experiment systems;

Program packages for instructional systems;

Program packages for office work;

Program packages for identification and optimization in control systems, etc.

In the future, programming software of SM computers with main frame architecture will be developed in the following directions:

Expansion of the set of programming modules which realize logical and mathematical data processing;

Expansion of the set of technological programming modules including the creation of data bases for real-time systems;

Elaboration of programming components which assure efficient operation of elaborated syntactic and semantic equipment expanders;

Development of existing operating systems for efficient operation of multiprocessor configurations, creation of special operating systems for high productivity and high reliability systems, elaboration of programming software for computer grids and multifunctional operating systems;

Creation of programming systems and high-level languages for solving real-time problems, parallel computations, analytical conversions and systems programming;

Creation of a system of programming based on advanced methods of technology for industrial production of programs and programming documentation for microprocessor systems, microcomputers as well as for problem-oriented complexes of various purpose.

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[207-8617]

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APPLIED PROGRAM PACKAGES FOR IDENTIFICATION, SIMULATION, ANALYSIS AND SYNTHESIS OF AUTOMATED CONTROL SYSTEMS

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[Abstract, Excerpts from article by I. Tomov, N. Madzharov and I. Stoychev, Bulgaria]

[Excerpts]

Below is considered the elaboration of an applied program package designed for automation of some of the stages of the process of planning automated control systems.

Elaboration of the SSPA package is based on the SSP package (scientific programs in Fortran).

The package of applied programs SSPA is intended for operating with the YES-1020 computer (or higher) under control of DOS or OS. It is generated and used in eight computing centers in Bulgaria. The SSPA package was used to solve problems in planning of control systems in the metallurgry, cellulose-paper and food industry, for planning tracking systems and automated electric drive systems, in engineering, etc. The results of use of program packages, the desire for improvement of specific subroutines expressed by users, and the growing interest in problems of planning of discrete systems served as the basis for elaboration of a second version of the package (package SSPA II) which was delivered to users in 1979.

Let us cite the brief characteristics of specific subroutines designed for solving the corresponding problems in the enumerated planning stages.

Identification of control objects.

Simulation. The SSPA package contains several programs which are used in various mathematical descriptions of systems.

Analysis. Stability of linear stationary systems in the SSPA package is analyzed by two methods according to lag.

Synthesis of automated control systems. In the SSPA program package are included subroutines for synthesis of continuous automated control systems in frequency and time regions (in distance space). The SSPA II package, in addition to improved versions of the subroutines, also contains subroutines for synthesis of discrete control systems.

In conclusion, it is worth noting that the SSPA II package covers a wider range of problems than some known applied program packages of similar value [17]. The overall concept of the SSPA and SSPA II packages permits use of standard configuration of YES computers which makes it possible for wide application of these packages. However, this concept imposes somewhat higher requirements on the knowledge of engineer planners to be able to work in Fortran language. Consequently, it was useful to have cooperation between the "automation" departments of Moscow Engineering Institute and "automation and remote control" department of Higher Computer-Electrotechnical Institute imeni Vi Lenin in Sofiya, which was aimed at creating programming software for problems of automated control systems for package and dialogue operating conditions. It may be expected that in the future this cooperation will permit an increase in the quality and efficiency of work on creation of programming software for solving problems of such a promising direction of technical progress as automation of production.

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APL PROGRAMMING SYSTEM--EFFECTIVE TOOL OF ANALYSIS AND SYNTHESIS OF DIGITAL SYSTEMS

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[Excerpts from article by A. Petkov, K. Yanev, and K. Boyanov, Bulgaria]

[Excerpt]

Below is proposed the next approach to synthesis of combinatorial schemes using the interactive APL system: the use of fast approximate methods to obtain a series of solution variants, after which the user is able to determine whether it satisfies any of these solutions or the search must be continued.

System synthesis includes: input subsystem, subsystem of realization of adopted procedures (processing) and output subsystem. With the aid of the input subsystem, the fields of application of Boolean functions are set. The processing subsystem realizes procedures of discovery of dead block coverage of a completely defined function and expansion of a completely defined function with a small number of variables and their minimization. Furthermore, the possibility is provided for retrieval of the total minimum coverage of the system of Boolean functions. The subsystem includes procedures of optimization by instructing the system. The output subsystem is designed to infer the results.

All enumerated procedures and subsystems are under the general control of the monitor program which carries on a dialogue with the user and determines the operating conditions of the system.

The input subsystem may preset the fields of application of analysis of a function using decimal equivalents of sets or by trinary vectors of intervals of the appropriate fields.

The discovery procedure of general coverage of the system of Boolean functions realizes approximate algorithms including discovery of dead lock coverage of each function of the previous procedure and the next maximum reduction of general coverage with retrieval of the total minimum implicant.

Furthermore, a procedure is used for retrieval of the optimum solution under user control.

The output subsystem presents different opportunities for organizing inferred information.

The proposed subsystem contains 2,000 statements and is realized on the YES-1040 computer. Each subsystem occupies two library regions (32 kbytes each).

APL system operates under the control of the YES disk operating system occupying 160 kbytes of main memory. It is adapted for operation with a modified operator console YES-7074-01 or YES-8501 terminal [6].

The APL system was tested using the modified YES-7074-01 console operating as a local terminal connected to the multiplex channel. Various combinations of Cyrillic symbols were used to image the special APL symbols.

Within the bilateral cooperation between the Scientific-Research Institute of Electronic Computers (Minsk) and the Institute of Computer Technology (Sofiya) a specialized local terminal was developed for operation of APL on the basis of a printer with a special printwheel. Participating in the elaboration were the Institute of Mathematics of the Bulgarian Academy of Sciences. Creation is planned for a remote terminal which includes the local terminal in the nomenclature of the YES computer.

[207-8617]

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REALIZATION OF APPLIED PROGRAM PACKAGES FOR TECHNICAL AND ECONOMIC PLANNING

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[Excerpts from article by V. A. Pavlechko, USSR]

[Excerpts]

Functional aspects of applied program packages for technical and economic planning (PPP-TEP). The package is oriented toward automation of calculation of the optimum plan in machine and instrument construction enterprises, primarily with unitary, small serial and serial production. PPP-TEP may be included in ASU in both full volume and as a separate complexes.

The number and composition of automated functions at each specific enterprise are established as a function of such factors as methods of planning and accounting used at the enterprise, aspects of organization of production and methods of calculation as well as the degree of information independence of the problem.

PPP-TEP permits calculation of the optimum plan of an enterprise at the stage of plan elaboration, after obtaining control figures for basic technical and economic indicators, and also to optimally distribute the enterprise plan in planned periods. The number of criteria of optimalness by which it is possible to calculate the enterprise plan is not limited.

Operation of PPP-TEP is assured on the YES computer with a volume of main storage of at least 128 kbytes and operating under the control of the DOS YES disk operating system in version 2.0 or higher.

Generation time on the YES-1022 computer under conditions of a specific object is 2.5 hours. The duration of the calculation problem solution of an optimum plan of an enterprise for 100 items and 108 constraints in terms of five local criteria for the compromise version is 18 minutes.

[207-8617]

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ON ONE APPROACH TO REALIZATION OF PRINCIPLES OF CLOSED SYSTEMS FOR DEVELOPMENT OF DATA BASE MANAGEMENT SYSTEMS (SUBD) OF INTEGRATED DATA PROCESSING SYSTEM (SIOD) FAMILY

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[Excerpt from article by I. I. Zolotnikov, G. B. Malev, A. A. Kelekhsayev]

[Excerpt]

Special programming systems are used for management of data bases--data base management systems (SUBD).

The integrated data processing systems SIOD 1 and SIOD 2 are widely used as automated enterprise management systems (SUBD). Though these systems have many merits, they are not free of substantial shortcomings. If the structure of the data base corresponds to that shown in the figure in any of its "subsets," these systems have the features of a closed SUBD, i.e., for creation and servicing of such data base and to obtain information from the data base, the user must make negligible programming efforts. But if the structure of the data base is wider than shown, a large volume of programming work must be done to realize these functions. In any event, programming of the arrangement of data base entries is completely entrusted to the user.

The SIOD 1 and SIOD 2 provide for input of input data only from punched cards or mag cards.

The above systems have no devices to guarantee the integrity of the data bases. All these shortcomings make it necessary to have great labor expenditures to create a programming complex designed for control of the specific data base of ASUP.

[207-8617]

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FIRST COMPATIBLE TESTS OF HARDWARE AND PROGRAMMING DEVICES OF THE INTERNATIONAL SYSTEM OF SMALL COMPUTERS (SM EVM)

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[Article by Yu. A. Lavrenyuk, V. V. Belynskiy, B. P. Golubev, V. M. Zenin, USSR]

[Text] In June-July 1977 in Moscow the first international tests were conducted on computer hardware of the system of small electronic computers (SM EVM). The tests were done on the basis of a plan affirmed by the chairman of the Intergovernmental Committee on Cooperation of Socialist Countries in Computer Technology (MPK po VT). This plan is prepared annually by the Coordinating Center of MPK po VT. In accordance with the operating positions of main designers of SM EVM in the council, the compatible tests have been conducted with the participation of representatives from at least two countries. In the case considered by us, the Commission on Conductive Tests included representatives of all countries participating in the Agreement on cooperation in the field of elaboration, production and application of computer hardware, representatives of Bulgaria, Hungary, East Germany, Cuba, Poland, Romania, the Soviet Union and Czechoslovakia. The commission also included coworkers of the Coordinating Center of MPK po VT. The chairman of the commission was Je. Slawinski (Poland).

The following items were tested: two types of processors SM-1P and SM-3P, two types of main memories, three types of magnetic disk memories, two magnetic disk memory control devices, an alphanumeric CRT terminal, an I/O punched tape device, four types of printers, and three operating systems. A list of the hardware which underwent testing is given in the table.

Two types of tested processes correspond to two architectural trends in computer hardware adopted for the first phase of SM EVM. The directions differ from each other in the system of instructions, methods of organization of information exchange between devices, methods of processing interruptions and some other characteristics. The list of SM EVM hardware provides for four processors: SM-1P and SM-2P relate to a single architectural direction, SM-3P and SM-4P to the other direction. The SM-1P and SM-3P processes which underwent testing are 16-bit parallel central processes with microprogramming control and multiple level interrupt system. Productivity of these models is the lowest among models contained in the product list. It is calculated in conformity with the methods on standardization SM EVM 019-78 "Evaluation of productivity of processes according to mix characteristics" and constitutes in solution of problems of operative control one hundred and forty thousand and one hundred and sixty thousand operations per second.

Table 1

Device*	SM EVM Code	Country-Developer
Processor, SM-1P	SM-2101	USSR
Processor SM-3P, built into monitoring and measuring equipment	SM-2103	USSR
Ferrite main memory	SM-3100	USSR
Ferrite main memory	SM-3101	Poland
Mag disk memory cassette type IZOT-1370	SM-5400	Bulgaria
Mag disk memory cassette type MERA-9425	SM-5401	Poland
Control device (controller) of mag disk memories SM-5400 and SM-5401 for SM-3 and SM-4	SM-5105	USSR
Mag disk emory with fixed heads type MD	SM-5500	Hungary
External mag disk memory control device (based on SM-5500 memory)	SM-5501	USSR
Alphanumeric CRT terminal VT-47100	SM-7206	Hungary
Combined punched tape I/O device type MPR 51/301	SM-6200	Hungary
Alphanumeric mosaic printer DARO-1156	SM-6301	East Germany
Alphanumeric mosaic printer DZM-180	SM-6302	Poland
Alphanumeric parallel printer VT-24112	SM-6316	Hungary
Alphanumeric parallel printer VT-25150	SM-6321	Hungary
Single-disk replaceable cassette	YES-5269-01	Bulgaria

* Basic technical specifications of devices are given in section entitled "Information on new devices of YES and SM computers" of this collection.

Peripheral devices are connected to the SM-1P processor across a type 2K radial interface which permits the connected devices to exchange data under monopole conditions at a rate of up to two hundred and seventy thousand 16-bit words per second. The type 2 systems interface is determined by methods material on standardization of SM EVM 005-76 which establishes the set and designation of interface buses, signals transmitted through them, communication algorithms, and electrical and structural realization of outputs to the interface.

The SM-3P processor, main memories and peripheral devices are combined in the complex by means of a main circuit interface of the "common bus" type which permits the connected devices to exchange data under monopole conditions at a rate of up to one million three hundred thousand 16-bit words per second. The systems interface "common bus" is determined by methods material on standardization SM EVM 003-76 which establishes the structure and designation of interface lines, communication algorithms, requirements for functional and time characteristics of signals and physical realization of the interface.

The compatibility tests were run to determine the suitability of prototype computer devices for operation in the SM EVM system and also to determine the possibility of their industrial serial production. The following tests were done for this purpose:

Correspondence of prototypes to technical specifications;

Correspondence of prototypes to technical standards documents adopted for the SM EVM;

Proper combined operation of technical devices under the control of operating systems;

Program compatibility and conformity of technical hardware to requirements of systems programs.

In addition, the technical design and operating characteristics were evaluated, the nomenclature of the component items was analyzed and the completeness and quality of technical documentation was verified.

The devices were tested both independently and in test complexes. This verification made it possible to determine whether or not the rules of systems interfaces were accurately maintained in elaboration and manufacture of these devices.

During the combined tests of the technical prototypes, three test complexes were put together which contain various device sets: one SM-1 complex based on the SM-1P processor (Figure 1) and two versions of the SM-3 complex based on the SM-3P processor (Figure 2). All devices marked for testing were put into these complexes.

The devices forming the test complexes were tested under the control of operating systems using complex problems which represented the set of tests for devices appearing in the complex. In addition, additional tests were run by executing several program selected by the committee.

Basic programming software of these technical devices including three operating systems was tested simultaneously to the above devices:

Disk operating system (DOS SM-1) for control of computing complexes (UVK) constructed on the basis of the SM-1 processor;

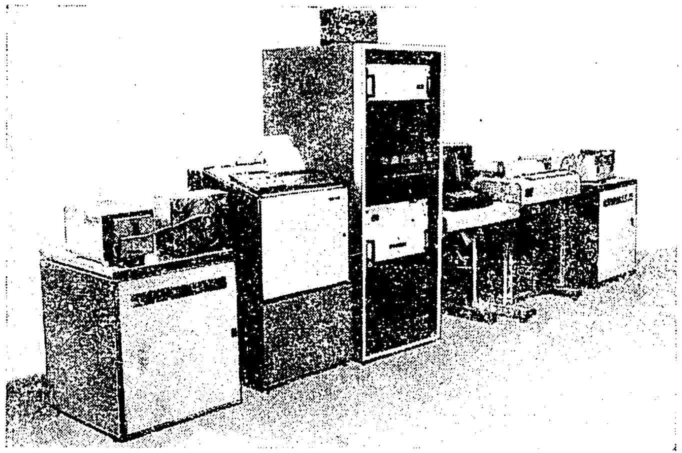

Figure 1. Overall view of SM-1 complex.

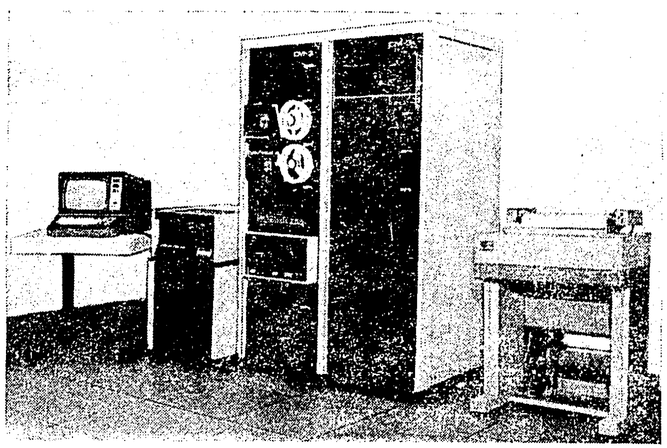

Figure 2. Overall view of SM-3 complex.

Disk operating system (DOS SM-3) for UVK constructed on the basis of the SM-3 processor;

Tape operating system (LOS SM-3) for UVK constructed on the basis of the SM-3 processor.

These operating systems permit users to efficiently utilize possibilities of the UVK by providing them with a broad spectrum of services in program and data preparation. Disk operating systems organize the work of these UVKs which have external magnetic disk memories.

The DOS SM-1 was developed by Soviet experts. This system performs the following functions under both dialogue and package conditions: translation, editing, arrangement, debugging and control of user program execution written in the languages Mnemocode, Fortran-II, Fortran-IV, Algol and Basic. In addition, the system guarantees storage of systems programs and user programs and data in the form of disk files with rapid access and provides convenient means for operating with the files. The generation devices of the DOS SM-1 make it possible to obtain the necessary version of the system in conformity with the configuration of the complex.

The DOS SM-3 was developed jointly by experts of Bulgaria and the Soviet Union. This system provides translation of initial texts written in the languages Macroassembler and Fortran-IV, editing of symbol texts, arrangement and debugging of user programs stored on disks and punched tape, construction of libraries of programming modules and control of user program execution under both dialogue and package conditions. The DOS SM-3 stores systems programs and user programs as disk files with rapid access and provides developed and convenient devices for operating with the files (identification and protection, creation, increment and replacement of files). The generation devices of the DOS SM-3 make it possible to obtain the necessary version of the system in conformity with the configuration of the complex and requirements of specific application. During the generation process the system permits driver programs to be connected to it for additional peripheral devices.

The LOS SM-3 was developed jointly by experts of Hungary, the Soviet Union and Czechoslovakia. This system arranges the operation of the UVK SM-3 of minimum configuration which includes the following: the SM-3P processor, 8K-words main memory, punched tape I/O device, alphanumeric printer and CRT terminal. Instead of a punched tape device, a magnetic tape cassette I/O device may be used if the methods of interaction and information formatting are the same as for the punched tape device. The LOS SM-3 may be supplied to the user on either punched tape or magnetic cassette tape. The LOS SM-3 makes it possible under dialogue conditions to translate, edit, arrange, debug and execute user programs written in the languages assembler, basic and the input language of the dialogue programming system DS-SM. The input language DS-SM is a high-level dialogue language designed for conduct of computing work in the field of automation of scientific experiments, the sphere of teaching, in scientific and technical and economics research. The LOS SM-3 contains packages of standard subroutines which assure multiplication and division of numbers with fixed decimals, calculation of elementary functions and execution of operations on numbers with a floating decimal.

Tests of the operating systems DOS SM-1, DOS SM-3 and LOS SM-3 were run with the aid of special control problems written in various programming languages and with the aid of additional demonstration problems.

All devices and operating systems presented for testing successfully passed them and are recommended for the use in the SM computer system. All devices have been given SM EVM codes (according to the rules of the SM EVM committee, codes are given only if the device successfully passes testing).

Typical of the tests carried out is that within a short time a single committee simultaneously tested a large number of computer devices. As a result, it was proposed firstly that the country organizing the tests carry out a preliminary combined test of all devices in the test complex. Secondly, the country participating in the Agreement was to create testing grounds for the SM EVM computers and fit them in the near future with processors and other SM EVM equipment. And finally, during conduct of the tests more attention should be given to verification of program compatibility and proper operation of technical hardware in the complex under the control of the operating systems and using control programs. The control programs themselves should be provided in a form so that the operation of the devices approaches real operating conditions. Realization of these proposals will make it possible, we feel, to greatly enhance the quality of test work.

Testing confirmed both the functional possibilities of the elaborated technical and programming devices as well as their ability for combined operation in computing complexes. The set of computing devices which underwent the tests permits construction of automated control systems of various types.

[207-8617]

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VERIFICATION OF THE OPERATING EFFICIENCY OF THE YES-1021 COMPUTER

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[Article by L. Obruča, Ja. Pač (Czechoslovakia)]

[Text] At the fifteenth session of the Intergovernmental Commission on Cooperation of Socialist Countries in the field of computer technology it was decided to develop methods for testing the operating efficiency of computers. (The term 'operating efficiency of computers' implies the reliable and efficient application of computer functions--and not only operating reliability as is sometimes considered--determined by the corresponding Technical Conditions or TU.) In the elaborated Temporary Position are cited the forms of primary blanks for preparation of records of operation and failures of computers--"Operating Journal" and "Record of Failures", as well as secondary blanks "Monthly Report on Operation" and "Quarterly Reports". The first three blanks are filled out by the user, the fourth one is completed by the appropriate National Organization on Technical Service (NOTO). The reports are centrally processed and are sent to the Coordination Center in Moscow.

In Czechoslovakia, the Division of Quality Control of NOTO on the basis of the Temporary Position, in 1976 developed a format plan for the Monthly Report. After confirmation, the blank will be used by statistics branches with the designation VT(FMHTS) 1-12. These blanks are used to transmit Monthly Reports for centralized processing.

The reports contain information about failures as well as the method of eliminating breakdowns and recovery time of computer efficiency. These data are transmitted to the manufacturing plants of the EVM-1021, servicing organizations and the Division of Efficiency Study at the Research Institute of Mathematical Computers (VUMS). Feedback is therefore arranged for quality control of technical equipment and elimination of its operating shortcomings.

The operating efficiency of programming software is monitored separately with the aid of claims. Claims for the operating system MOS are taken by VUMS, claims on applied programs by the organization NOTO.

The resources of the so-called complex interfactory team (MP KRB) are used to eliminate operating shortcomings detected; it was organized within the framework of the trust "Plants of Automation and Computer Technology". This team consists of about ten permanent members, and if necessary may be increased to 40 men--experts from enterprises and plants which participate in the elaboration, production and service of the YES-1021 computer. The activities of this team are mainly aimed at overcoming organizational deficiencies which may appear in several official interplant relationships where the solution of a problem is flowing through several administrative levels, and second--for direct solution of problems. Personal contact of workers from organizations participating in the entire installation and utilization process of computer hardware plays an important role in the work of the MP KRB.

The MP KRB consists of five working groups: programming software, service and installation of the computer, operating documentation, reliability, improvement of technical hardware. The supervisors of the working groups form the Presidium of the MP KRB which gathers at operational meetings where they exchange operating experiences, and further plans are made and the activities of the individual groups are coordinated. If necessary, experts can be brought in from organizations which directly participate in the elaboration of computers or are working in cooperation.

The MP KRB issues an information brochure "Operating Information of the YES-1021 Computer". This manual is sent out in two copies to each user of the YES-1021 computer (for technical and operator maintenance of the computers in computing centers). The manual is issued at least three times a year and is about 20 pages long; it contains all kinds of vital information on both the operation of hardware and on programming software. There may be, for example, specific indications and advice on independent elimination of computer shortcomings, reports on advanced operating experience, information on rationalizer suggestions which enhance the operating efficiency of computers, etc. Because of the initiative of the MP KRB, it was possible to interest the workers of technical service of the YES-1021 computer in using the system of defect-free labor.

Completion of the Monthly Report Form on Computer Operation

The report blank is completed by the computer user and is sent by him at the beginning of each month to the NOTO organization. When planning the report blank VT(FMHTS) 1-12, it was felt that the greatest problems in computing centers would occur in connection with determination of efficient machine time. For these reasons, the report blank contains a general on-time base of the computer P_{ON} which can be established according to the difference in values of on-time readouts at the computer console at the end and beginning of the working period. These data are independent of the method of distribution of computer time. The values of prevention time are based on requirements for prevention formulated in the operating manual. From the example of form completion shown in this text, we can clearly see the difference between the number of device failures and the number of computer failures: if nine failures occur during the test period, then only three of them led to computer failure, i.e., it was impossible to use the computer until these failures were eliminated. In the other six cases of device failures, the nonfunctioning device was replaced with a spare, and the computations continued.

Storage of Data from Report Blanks

Based on the data from the report blanks, monthly reports are drawn up, and on their basis quarterly reports, which are sent to the Coordination Center in Moscow. As a result, there is an increase in the amount of the statistical sampling (i.e., in our case, the number of failures), and thereby this reduces the interval of statistical scattering of the computed point values of individual indicators of reliability such as the average between failures $\hat{T}_0$, average recovery time after failure $\hat{T}_r$, etc.

Integration of individual partial inaccuracies due to the subjective nature of the current method of preparation and gathering of data on computer operation occurs in the same way.

Notations of reliability parameters used above were selected according to the proposed CMEA standard.

Use of Data on Operation of the YES-1021 Computer to Improve its Operating Reliability

To increase operating reliability as a basic component which determines computer operating efficiency, the critical parameters which have a decisive effect on computer reliability indicators were defined at MP KRB.

According to YES computer standards, the main indicators of computer reliability are average time between failures T_0, average time between malfunctions T_S, average recovery time after failures T_V and the coefficient of technical utilization K_T.

In the foreign literature, for example in [1], it is indicated that in computers designed for commercial or scientific and technical computations (not to control real-time processes), the average time between failures may equal 4 to 40 hours. From the results of tests of the YES-1021 computer at the manufacturing site, it is known that such levels of T_0 are also achieved.

According to the data cited in [2], it is possible with sufficient accuracy to determine a certain complex indicator of system operating efficiency K_E, its actual throughput or productivity P_B, which is characterized by the number of successfully executed problems per unit of time, as compared to the theoretical throughput (productivity) of a troublefree device P_T:

$$K_e = \frac{P_B}{P_T} < 1. \qquad (1)$$

Accordingly, there is the so-called operating efficiency which can be defined thus:

$$K_e = \frac{T_{OS}}{T_{OS} + T_{VOS}}, \tag{2}$$

where T_{OS} is the average time between failures and malfunctions in hours; T_{VOS} is average recovery time after failures and malfunctions in hours.

In conformity with what has been stated above, point evaluation of these quantities equals:

$$\hat{T}_{\text{ос}} = \frac{T_{\text{н}}}{n_{\text{о}} + n_{\text{с}}}; \tag{3}$$

$$\hat{T}_{\text{вос}} = \frac{\Sigma t_{\text{в}} + \Sigma t_{\text{вс}}}{n_{\text{о}} + n_{\text{с}}}. \tag{4}$$

If we substitute (3) and (4) in (2), we find that

$$K_{\text{э}} = \frac{T_{\text{ос}}}{T_{\text{ос}} + T_{\text{вос}}} = \frac{T_{\text{н}}}{T_{\text{н}} + \Sigma t_{\text{в}} + \Sigma t_{\text{вс}}} = K_{\text{г}}, \tag{5}$$

where N_0 is the number of failures; N_S is the number of malfunctions; Σt_V is recovery time in failures; Σt_{VS} is recovery time after malfunctions.

Operating efficiency as seen in (5) coincides with the coefficient of readiness K_G, i.e., the confidence limit that in a specific time interval the computer will be able to operate. This definition is only valid if the average time value corresponds to the magnitude of mathematical expectation. If these average quantities T_{OS} and T_{VOS} are changed, their transient values $\hat{T}_{OS}$ and $\hat{T}_{VOS}$ permit us to shift to a number which at the limit changes to the value of the confidence limit.

For ordinary parameters of the Ryada-1 computer, based on inaccuracies which may be the result of different understandings of device failures in the computer system, it is possible to consider that $K_G = K_T$, where K_T is the coefficient of technical utilization of the computer. Based on verification of user claims during the period of operation, we established a nominal of K_T as a basic parameter for defining operating efficiency of specific YES-1021 computers. User computer requirements were satisfied when this value was attained or exceeded.

We know [3] that great experience in the control of quality and reliability of computers has been gained by the Minsk Computer Plant imeni S. Ordzhonikidze. In the documentation which accompanies every computer, detailed instructions are given for managing operator and technical journals and for completing report blanks which are sent to the manufacturer. In the plant laboratory, the report data are processed and suggestions are made for improving quality and reliability of new computers. The users are sent the generalized data which describe the reliability of specific devices in computers and the results of the valuation of computers belonging to them; therefore, the user finds out whether his computer can reach the average value of operating efficiency. Because the computers of the Minsk plant are serviced mainly by the user's technical personnel, the specific application of this information depends on the user.

Based on this experience, experts of the MP KRB came to the conclusion that for the YES-1021 computer, the average value between failures is rather high, however, its value does assure acceptable operating efficiency of the computer. In addition, we carefully studied the possibility of applying the experience of the Minsk plant (including the Saratov system) to centralized control service. We concluded that the collection on the use and failures of computers and the analysis and evaluation of these data are necessary to interest personnel in achieving or exceeding a nominal coefficient of technical utilization. This can be achieved by both material and moral encouragement. Because the personnel in centralized control service work in the NOTO, it was relatively simple to elicit this interest: a commission was created of workers of the service division (technicians) of MP KRB and the division of quality control of NOTO to control operating reliability, which at regular sessions each month analyzes monthly reports. The commission is more thoroughly involved with computers which have not achieved nominal coefficient of technical utilization. It considers individual failures, and discovers their cause: non-observance of preventive maintenance or deterioration of operating conditions; for long-term repairs it establishes whether or not spare parts were delivered on time, an expert was summoned, etc. For other computers such analysis is done by technicians, which is a certain kind of self-monitoring.

As a result of activities of this commission over several months, nominal coefficients of technical utilization were achieved for almost all computers. The coefficient of technical utilization of the YES-1021 computer of serial production is now reaching the level cited in GOST 16325-76, section 1.6.5.

Accounting of Malfunctions

Until now we have been occupied with methods of accounting and evaluation of computer failures or devices. But when working with computers, there are short-term interruptions in calculation which are either caused by operators and programs (fault of maintenance personnel or of the program) or technical errors (technical interruptions of computers of this kind are called "malfunctions" in the Soviet literature, "intermittent failure" in English, and "prechodna porucha" or "selhani" in Czech . According to the most recent suggestions of the Working Group on YES Computer Reliability, the definition of malfunctions is as follows: "Malfunction is an event characterized by the temporary curtailment of computer (hardware) operating efficiency. Operating efficiency itself is restored without repair or adjustment.").

FSU confirmed for FMHTS Number 3836/78
To:
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MONTHLY REPORT ON RELIABILITY OF YeS COMPUTER

Standard Title VT (FMHTS)1-12

REPORT PERIOD
19___ month___
Explanation: FMHTS-
Federal Ministry of Metallurgy and Heavy Industry
FSU = Federal Statistics Institution

Organization completing monthly report
Address of computing center

1. Report on computer reliability (time, in hours)

(a) Шифр ЕС ЭВМ	(b) Заводской номер ЭВМ	(c) Дата начала работы	(d) Время включения $T_{вк}$	(e) Время действительного технического обслуживания ($T_{то}$)	(f) Время восстановления при отказах $\Sigma t_в$	(g) Количество отказов $n_о$
1	2	3	4	5	6	7
ЕС-1021	XXX	XXX	170,3	15,8	2,0	3

[Key: a. code of YeS computer; b. computer plant number; c. operating start date; d) on time; e. time of active technical maintenance; f. recovery time after failure; g. number of failures]

II. Report on reliability of devices in computer comples (in hours)

Порядковый номер (h)	Шифр устройства (i)	Количество устройств ЭВМ (j)	Суммарное время: во включенном состоянии $T_{вк}$ (k)	Суммарное время: действительное техническое обслуживание $T_{то}$ (l)	Суммарное время: восстановление при отказах $\Sigma t_в$ (m)	Количество отказов $n_о$ (n)
8	8	9	10	11	12	13
21	ЕС-2021	1	170,3	10	0	0
22.	ЕС-3221	1	170,3	5	0	0
23	ЕС-5558	1	170,3	5	0	0
24	ЕС-5515	1	170,3	5	0	0
25	ЕС-5058	5	850,0	30	3,5	2
26	ЕС-5022	6	300,0	20	14,5	4
27	ЕС-7031	1	170,3	10	1,75	2
28	ЕС-7172	1	170,3	10	0	0
29	ЕС-6016	1	170,3	10	0,25	1

[Key: h. sequence number; i. code; j. number of devices; k. on time; l. active technical maintenance; m. recovery after failure; n. number of failures]

Continuation

(h) Порядковый номер	(i) Шифр устройства	(j) Количество устройств ЭВМ	Суммарное время			(n) Количество отказов n_o
			(k) во включенном состоянии $T_{вк}$	(l) действительное техническое обслуживание $T_{то}$	(m) восстановление при отказах $\Sigma t_в$	
а	8	9	10	11	12	13
30	ЕС-7902	1	10,0	1	0	0
31						
32						
33						
34						
35						
36						
37						
38						
39						

(o) Дата отсылки	(p) Печать предприятия-пользователя ЭВМ	(r) Кто подтверждает отчет (фамилия, подпись, дата)	(s) Кто составил отчет (фамилия, подпись, дата)

[Key: o. remittance date; p. seal of computer user enterprise; r. report confirmation (name, signature, date); s. report writer (name, signature, date)]

III. Report on failures

(t) Порядковый номер	(u) Шифр устройства	(v) Описание отказа и способ устранения — ремонт	(w) Затраты времени для устройства $\tau_{ин}$
а	14	в	15
40	ЕС-5058	Замена источника (ЗИП) (x)	0,5
41	ЕС-5058	Выборка не закончена; замена (y) ИС МН8440 на ТЭЗ-V1	13,0
42	ЕС-5022	Не проходят КПТО; замена ИС МН8472, МН8410, ТЭЗ-10VZ; задача № 13 (z)	3,0
43	ЕС-5022	Нельзя зарядить ленту; замена ИС (aa) МН8420, 8430, ТЭЗ-ОСНО	13,0

[Key: t. sequence number; u. device code; v. failure and repair; w. time lost; x. replace source; y. sample not complete: replace; z. do not pass KPTO, replace; aa. tape doesn't magnetize; replace]

Continuation

Порядковый номер (t)	Шифр устройства (u)	Описание отказа и способ устранения — ремонт (v)	Затраты времени для устройства, ч (w)
а	14	в	15
44	ЕС-5022	Ошибки чтения; замена конденсатора С 100 МКФ, ТЭЗ-RSTD (bb)	2,0
45	ЕС-5022	Сигнал «СНЕК»; настройка (cc)	6,0
46	ЕС-7034	Не печатает знак; замена конденсатора С65 (dd)	1,0
47	ЕС-7034	Не печатает один разряд; замена транзистора KUY12, ТЭЗ-VOKL (ee)	0,75
48	ЕС-6016	Зажим перфокарт; настройка механизма (ff)	0,25
49			

[Key: t. sequence number; u. device code; v. failure and repair; w. time lost; bb. read error; replace capacitor; cc. SNEK signal; adjust; dd. does not print sign; replace capacitor; ee. one digit doesn't print; replace transistor; ff. punched card jammed; adjust mechanism]

To determine the causes of interruption--whether there has been a malfunction or a failure--the problem or some part of it where the malfunction took place is repeated, or an attempt is made to reenter data from the input devices, according to the nature of the malfunction.

Accounting of events occurring in computer operation in such detailed form to unambiguously determine whether or not it is a malfunction or a failure is unfeasible until automated objective accounting of events in computer operation is set up.

Comparative analysis of the data on operation of computers is currently depreciated by the fact that the data on malfunctions and failures are confused because of different methods of evaluation, although these data are extremely useful for improving computer operating efficiency. The average time between failures is used for the programmer as an indication of how to select the appropriate points of return and monitoring in long problems (RETRY and CHECK-POINT), in order that the reliability of problem realization is high and computation time is acceptable.

A frequent occurrence of malfunctions due to contamination of information media is the signal for testing the cleanliness of the atmosphere of the computer room and monitoring care of the media.

Averaged requirements for the number of peripheral devices (mainly external memories) aids in precisely determining the makeup of spare equipment required.

Malfunctions due to external factors in the case of short-term loss of the power grid can to some extent be recorded on the YES-1021 computer using a so-called power grid monitor, which is a standard part of the power plant control computer. If this type of malfunction appears very often, it is necessary to use a portable generator or other computer power supply resistant to effects in the primary grid.

Physical causes of malfunction are very wide ranging. They may be random phase shifts which produce metastabled effects: the output of the digital circuit sometimes (it may be several times greater than circuit response time under normal conditions) shows a logically indeterminate level. This effect may occur, for instance, because of non-observance of technical specifications concerning phase relationships of signals at the circuit input which randomly appear in a synchronous connection of separate parts of the computer. In other cases, the cause may be the incorrect synchronization of circuits where the time diagram is not observed. The reason for the described effect may likewise be degradation failure. Failures caused by incorrect values of signal amplitude also belong to this category.

Observations of the effects described above aid in timely prevention of "degradation" of the system, which can lead to total failure.

All the above shows how important it is to know the reliability indicators T_S and T_{VOS} of a specific computer because the results of central accounting and evaluation of these indicators are of low reliability. Let us note for orientation purposes that the average time between failures T_O is about 1.5 to 10 times greater than the average time between malfunctions T_S [4].

It is necessary to emphasize that the number of malfunctions n_S which is recorded in the observation of operation of one computer is relatively small and thus transient estimates $\hat{T}_{VOS}$ and $\hat{T}_S$ should be replaced by interval estimates for 90% reliability intervals according to Czechoslovak standard ChSN 36,7001. This requirement also pertains to T_O and T_V.

Conclusion

Monitoring of computer operation has important value not only for the obligatory statistical accounting organized by competent state statistics branches, but also to establish feedback in the quality control and computer operating efficiency system.

It is necessary to emphasize that actual monitoring of computer operating efficiency assures adequate quality of special components on which the operating efficiency of the end devices depend. This conclusion is well known but its realization involves several practical problems. Despite the actually great expenditures involved in monitoring and evaluating, additional changes and elimination of detected deficiencies, they must be done since low computer operating efficiency causes the user to lose confidence in the product.

Let us cite the list of shortcomings which cause problems in the more detailed recording of data on computer operating efficiency and their evaluation:

1) Conditions are not established for interesting the workers participating in the collection, transmission and evaluation of data on computer operating efficiency;

2) With the exception of the relatively short period of warrantied operation, it is impossible to require more detailed data on computer operation, especially data on failures, their causes, methods of localization, etc., until the VT(FMHTS) 1-12 blanks are completed;

3) Shortcomings often found in computer operation take a long time to eliminate, and consequently some workers feel it is useless to monitor them. As a result of this, reports on the operating process and failures are incompletely compiled;

4) In spite of the fact that data on computer operating efficiency and failures can be processed by computer, much of it is manually processed: about 90% of the total time of operation is consumed in obtaining recordings of data on use and only 10% is used to record data on failures and other unplanned and unexpected events in the process of computer operation. Consequently, it is advisable to introduce a programming system for automated job accounting and fill in the blanks mechanically. The recordings should be generalized in data bases about operation and failures, on events in the operating process and their analysis. The current introduction of the primary blank for preparation of recordings on operation and failures of computers according to the Temporary Position is delayed or impossible because of variation in blank format. The question of machine processing of these data is also unresolved;

5) Workers in quality control departments or operational monitors have limited rights to take steps based on analysis of the tested operating processes. For that reason, measures are not adequate to improve the prepared plans.

Elimination of these shortcomings will make it possible to monitor computer operating efficiency and evaluate it, will promote further improvement of the YES computer operating efficiency.

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[207-8617]

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SYSTEMS PROGRAMMING SOFTWARE FOR INDUSTRIAL TESTS OF PERIPHERAL DEVICES. DEVICES FOR PROCESSING STATISTICAL INFORMATION.

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 133-141

[Excerpts from article by S. Voynov, N. Seanyagina and K. Boyanov, Bulgaria]

[Ecerpts]

Introduction of peripheral devices (PU) forming the nomenclature of the Unified System, it is necessary to test both the correctness of operation and their reliability and compatibility. The use of all-purpose computers for such testing is economically unprofitable. An essential shortcoming of systems which use specialized computers for this purpose are the limited resources with respect to the PU corresponding to actual operating conditions.

In study [1] a system is described which simulates systems (imitator) on the basis of minicomputers and a specialized monitor (adaptor) ensures close to actual operating conditions of the tested peripheral device.

In the current studies considered systems programming software for testing peripheral devices and the possibility that it provides for statistical processing of errors recorded during tests.

Conclusion. The programming system described is used in industrial tests of peripheral memories produced by the enterprises of Bulgaria. Its modular structure permits replacement of several test procedures as a function of new requirements imposed on the products or on modification of a given external memory. Information systems make it possible to process statistical information required for the manufacturer as well as monitor the operation of the PU, by detecting bugs arising during the warranty period.

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PROBLEMS OF RAISING QUALIFICATIONS OF PERSONNEL IN BASE PROGRAMMING SOFTWARE.

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 142-144

[Article by V. S. Alexeyeva and G. A. Lepin-Dmitryukov, USSR]

[Text] The shift to the new generation of computing systems of high productivity with an enormous set of base programming software devices has greatly sharpened the problem of programmer training. It is already impossible to reflect all the devices of the YES EVM operating systems in training courses and even more to teach programming in several algorithmic languages. It was necessary to find a means for more narrow specialization of training which would ensure preparation of the graduate for successful independent assimilation of operating system hardware and applied programming software not covered within the instructional plan.

At the Leningrad Institute for Increasing the Qualification of Workers of Industry and Urban Management in Control Methods and Technology (LIMTU) the training of programmers for the disk operating system (DOS YES) was done in two basic specializations: "programmers of DOS YES EVM" and "systems programmers of DOS".

The first of these specializations assumed the training of problem oriented program developers for elements of ASU programming software. The basic disciplines in this specialty are "disk operating system", "data management in DOS", "programming in assembler language" and "programming in PL 1 algorithmic language." To study automation devices for elaboration of programming systems of ASU, students attended a course "Systems of ASU Programming Software". In addition to the aforementioned basic disciplines, the instructional plan also included small courses entitled "Foundations of ASU Elaboration" and "Technical Hardware of the YES Computer System".

The specialization "systems programmers of DOS" is oriented to the training of personnel in the operation of ASU programming software. The basic disciplines "disk operating system" and "systems of ASU programming software" are aimed at a thorough study of operating system hardware and methods of elaboration and utilization of applied programming packages. This specialization included cycles of laboratory work done by the students at the computer control console. The laboratory work included simulation of various nonstandard situations occurring in the operation of a system and requiring rapid programmer response. As a result, the graduates of the Institute assimilated habits of computer operator work. This also made it possible to improve overall methods of operator training.

The course "Systems of ASU Programming Software" thoroughly examined questions of elaboration of applied programming packages (PPP) and is illustrated by several widely used PPP of various functional designations--questions of generation and monitoring of operating programs. The course and graduate studies of the students in this specialization were oriented towards the analysis of operating system component function and elaboration of service programs to expand DOS possibilities. The complex of text displays of the YES-7906 and packets of applied programs of the data base type were widely used in the course work.

By 1975 the specialization was defined "programmers of OS YES EVM" whose instructional plan is similar to the appropriate specialization for DOS YES.

The continuous expansion of the possibilities of operating systems and automation devices for elaboration of applied programming software led to the need of an even narrower specialization for programmer training. Training in a short period of time of a programmer who has to assimilate an enormous volume of information on base programming software and learn to efficiently use operating systems hardware in his developments, was almost impossible. The only possible solution to this problem is the sequential training of problem-oriented programmers: at first on base programming software devices which make it possible for the graduates to develop programming modules by using algorithmic languages of the system and then, after acquisition of some work experience, on devices for elaboration and operation of applied programming software systems.

Training of programmers on base programming software of the computer for the disk operating system, for example, may be shortened to two months of instruction if the student is oriented to the use of one algorithmic language (assembler, PL 1 or COBOL). During this period it is possible to teach the technique of programming complicated programs, to examine all functional resources of the operating system, to carry out a series of laboratory studies on the function of the operating system under real conditions.

To increase the inefficiency of instruction on programming technology and task control language devices of the operating systems, modern technical hardware should be used. For example, at LIMTU a dialogue instruction system for remote package processing of assignments is being incorporated that uses the YES-7906 complex. Experimental operation of this systems showed its high efficiency in the study of input languages of the operating system.

The quality of training of programmers at the Institute for Enhancement of Qualification is also affected by the lack of instructional and methods materials in several disciplines. They must be prepared at a high methodological level in an extremely short time in order to reflect the latest versions of the operating system.

The successful solution of the problems of enhancing qualification of programmers in base programming software of the computer is one of the major factors for efficient elaboration and operation of automated control systems. A basic condition for resolving these problems is the high qualification of the instructors.

For training instruction personnel it is necessary to have constant methods work of the appropriate departments and scientific research work of instructors which is a fundamental source for acquiring practical skills in the utilization of base programming software devices in ASU. Instructors must keep in close touch with the latest technical documentation on base programming software and have adequate time for methods work on the computer. One source of information on problems of monitoring base programming software of computers can be the consultation of instructors for computer users.

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PROBLEMS OF RAISING QUALIFICATIONS OF EXPERTS IN ASU PROGRAMMING SOFTWARE BASED ON APPLIED PROGRAM PACKAGES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 144-147

[Article by L. A. Ivanov and V. Ye. Sizov, USSR]

[Text] Developers of working program complexes (applied programmers) have been given powerful operating systems containing programming components with a total volume of several million instructions; the variety of applied programming packages (PPP) on the world market numbers in the tens of thousands. Assimilation of these resources to tackle specific ASU jobs requires special and sufficiently high knowledge and skills which are quite different from the knowledge and skills of programmers who worked on the first and second generation computers.

The problem of training (and retraining) programmers who are able to efficiently work under the new conditions has become urgent: the complexity and keenness have intensified because, faced with a large number of different PPP, in essence there is no scientifically justified utilization structure developed and the general principles have not been defined for increasing the qualification of specialists in development and operation of PPP. On the whole, there are none of the necessary instructional plans, programs, methods guidebooks and training methods. Work experience in increasing qualifications is small and has been inadequately investigated, generalized and propagated.

Experience gained in four years of training specialists in programming software for third generation computers at LIMTU allows us to formulate the following assumptions. It is necessary above all to indicate that in raising qualifications, we should mark the limits of training for users who are not professional programmers but who need to obtain, while using certain PPP, specific solutions to management problems, and the training of professional programmers. In spite of the fact that both categories deal with the same object (manipulate the same group of PPP), their interaction with the package, the nature of the job, knowledge and skills greatly differ. Training should naturally be done in different groups with various plans and programs. Below we will discuss issues related to the training of professional programmers.

Experience shows that it is currently impossible to train universal programmers who freely master all of the enormous abundance of modern programming software; moreover, practice showed that this is not necessary. The wide range of application of computer technology required programmers to tackle individual special jobs with a unique knowledge of a narrow range and led to the separation of the once monolithic profession of programming into discrete specializations. The major divisions are as follows:

Development programmers of basic programming software;

Development programmers for specific applied packages;

Problem-oriented programmers creating program components for discrete subsystems of automated control systems;

Programmers assuring creation and use of complexes of remote data processing programs;

Programmers tackling scientific and engineering jobs of a computer nature;

Programmers of automated planning systems (SAPR);

Programmers of automated control systems for technological processes, especially programmers for machine tools with numerical programming software;

Programmers of programming software monitoring services.

As a rule, a program tackles a single type of job (it works within the framework of one specialization) for a long time; technically, it is not used to solve questions of other specializations. This situation permits us to determine the following technology of training (enhancing qualifications) of programmers. The knowledge and skills of a programmer should be differentiated on two levels: basic and special. Basic implies the fundamental information required for a programmer of any specialization; special reflects the specifics of a concrete specialization.

Initial training of a programmer consists in imparting to him the minimum necessary set of basic knowledge and skills and special knowledge of one concrete specialization. Knowledge and skills are improved in the process of practical activity of the programmer.

Retraining (enhancing qualifications) is related as a rule to assimilation of new specializations and most often comes down to the acquisition of knowledge and skills at a special level.

When considering the totality of basic knowledge and skills, it is necessary to note that on one hand it is desirable that their volume be as small as possible so that their mastery only takes a comparatively short period; on the other hand, the volume should be adequate for mastery of complex special programming software. We should also bear in mind that the minimally required volume of basic knowledge imparted to programmers during the initial training process should give them an opportunity for subsequent independent improvement--mastery of new objects of programming software. In favor of this, knowledge and skills of the basic level should be thorough and include fundamental issues of modern programming software. The basic level should include the following:

A clear presentation of fundamental concepts of construction of a system of third generation computer programming software and automated control systems;

Knowledge of basic resources of modern operating systems and the ability to use them in elaborating and exploiting ASU programs;

Knowledge of basic programming in two languages--Assembler and a high level algorithmic language;

A knowledge of the general characteristics and principles of organization of applied programming packages and basic methods of working with the package;

The ability to elaborate relatively simple programs and use basic components of the operating system: translators, editor, librarian, service programs.

A high level of basic knowledge imposes high requirements on trainees. Those entering the Institute for Increasing Qualifications are obliged to have higher physical and mathematical or technical education, practical work experience in creating programs and the minimum necessary knowledge and skills of the basic level.

In a short article it is impossible to examine the requirements for special knowledge in all the above specializations of programming. For example, we may cite that as a result of training, programmers can provide creation and use of data bases and obtain knowledge on the following questions:

Purpose and composition of major data base management systems (SUBD) and outlook for their development;

Arrangement and use of basic ASU PPP realizing SUBD functions;

Organization of data base processing under package conditions and remote access;

Elaboration of structures and programming complex of ASU data bases.

Much attention is given to the acquisition of practical skills which is promoted by performance by the students of laboratory course and graduate work conducted on modern computers. As a result of training, students learn how to:

Select SUBD for concrete elaboration;

Elaborate the structure of data bases;

Determine necessary composition of programming devices for data bases and elaborate individual programs;

Exploit basic ASU PPP realizing SUBD functions.

The problem of raising qualification of specialists in ASU programming software, including specialists in ASU programming software based on PPP, should be resolved as part of the overall problem of raising ASU efficiency and using computer technology in all CMEA countries.

To combine the efforts of specialists from CMEA countries in training personnel, the authors feel the following jobs are of top priority:

1. Elaboration of unified concept and methods of training and retraining specialists in ASU programming software based on PPP (goals, jobs, basic content and instructional technology);

2. Elaboration of coordinated training plans and programs;

3. Determination of coordinated structure of instruction--methods materials, composition of coordination plan of elaboration handbooks, exchange of handbooks.

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INFORMATION ON NEW SM EVM COMPUTER HARDWARE.

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 148-154

[Article by V. M. Zenin and Yu. A. Lavrenyuk, USSR]

[Text] The SM-2101 processor (Fig. 1) is a desk-top model with the case removed that can be mounted on a standard rack. The SM-2103 processor (Fig. 2) also mounts on the standard rack.

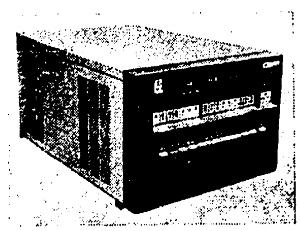


Fig. 1. SM-2101 processor

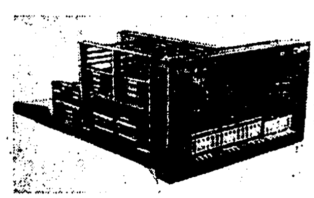


Fig. 2. SM-2103 processor

Technical Specifications

Code	SM-2101	SM-2103
Developer	USSR	USSR
Type	Parallel	Parallel
Capacity	16	16
Productivity in tackling operating control jobs, thousand operations/sec.*	Microprogramming 140	Microprogramming 160

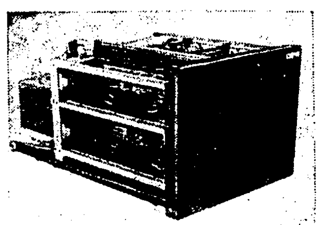
* Note: Productivity of processes defined on the basis of methods material MM SM EVM 019-78 "Evaluation of productivity of processors of SM EVM according to mixed characteristics".

Control principle	Microprogramming	Microprogramming
Number of universal registers	5	8
Interrupt system	Multi-level	Multi-level
Interface system**	2K	Common bus
Rate of data exchange under monopole conditions, 1000 words/sec.	Up to 270	Up to 1300

**Description of type 2K and common bus interfaces cited in methods materials on standardization of SM EVM: MM SM EVM 005-76, respectively.

Operating Memories

The SM-3100 ferrite operating memory (Fig. 3) mounts in a standard rack and was developed in the USSR; the SM-3101 ferrite operating memory (Fig. 4) was developed in Poland.



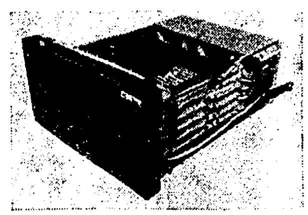


Fig. 3. SM-3100 operating memory   Fig. 4. SM-3101 operating memory

Technical Specifications

Capacity, K words	32
Word capacity, bits	16 + 2 monitor
Cycle time, microsec.	1.2
Sampling time, microsec.	0.6

Magnetic Disks

The magnetic disk cassette memory type IZOT-1370, its code SM-5400, is mounted in a standard rack (Fig. 5). The magnetic disk cassette memory type MERA-9425 (Fig. 6) has the code SM-5401.

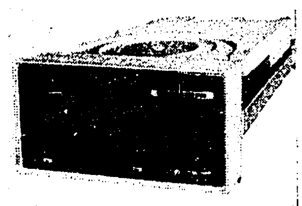


Fig. 5. SM-5400 magnetic disk memory

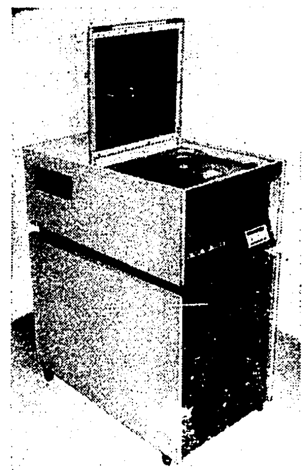


Fig. 6. SM-5401 magnetic disk memory

Control devices (controller) of magnetic disk memories SM-5400 and SM-5401 have the code SM-5105 (Fig. 7). It mounts in the standard rack and can service up to four SM-5400 and SM-5401 memories in the SM-3 and SM-4 complexes.

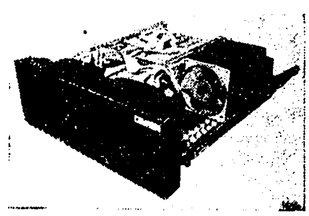


Fig. 7. SM-5105 magnetic disk memory control

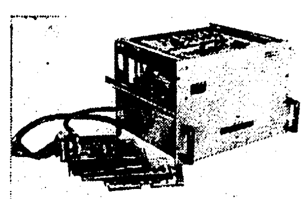


Fig. 8. SM-5500 magnetic disk memory with fixed head

Technical Specification of Memories

Code	SM-5400	SM-5401
Developer	Bulgaria	Poland
Number of data carriers	2	2
Capacity, M bits:		
Variable cassettee	25	25
Permanent disk	25	25
Rate of data exchange, M bit/sec.	2.5	2.5
Average retrieval time, milliseconds	45	40

The external mag disk memory control device SM-5501 includes a controller and mag disk with the type MD fixed heads which have the code number SM-5500. The controller can serve two SM-5500 memories in the complexes SM-1 and SM-2. The overall view of the SM-5500 memory mounted on the standard rack is shown in Fig. 8.

Technical Specifications of SM-5500 Memory

Developer	Hungary
Memory capacity, K byte, in modifications:	
SM-5500	860
SM-5500-01	1720
SM-5500-02	512
SM-5500-03	1024
Rate of data exchange, M bit/sec.	1.35
Average retrieval time, millisec.	10

Video Terminal

The overall appearance of the alphanumeric video terminal type VT-47100 is shown in Fig. 9.

Technical Specifications

Code	SM-7206
Developer	Hungary
Rate of data exchange using parallel interface, symbols/sec.	1000
Number of symbols in set	96
Screen size, millimeters	200 × 140
Number of lines	16
Number of symbols per line	80
Number of symbols on the screen	Up to 1280

Under off-line conditions it has the ability for text editing.

Tape Puncher/Reader

The combined I/O tape puncher type MPR-51/301 (Fig. 10) mounts in a standard rack.

Fig. 9. SM-7206 video terminal

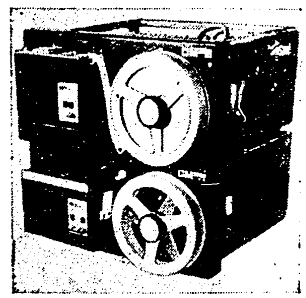


Fig. 10. SM-6200 punched tape I/O device

Technical Specifications

Code	SM-6200
Country	Hungary
Rate of input, lines/sec	Up to 500
Rate of output, lines/sec	Up to 50
Number of tracks on tape	5 or 8
Coding of data	According to GOST 13052-74

Printer

The alphanumeric mosaic printer type DARO-1156 (Fig. 11) has the code number SM-6301; the alphanumeric mosaic printer type DZM-180 (Fig. 12)--code SM-6302; the parallel printing alphanumeric printer VT-24112 (Fig. 13)--code SM-6316; parallel printing alphanumeric printer VT-25150 (Fig. 14)--code SM-6321.

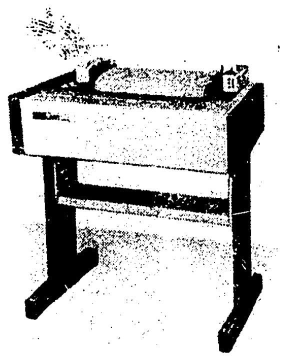


Fig. 11. SM-6301 printer

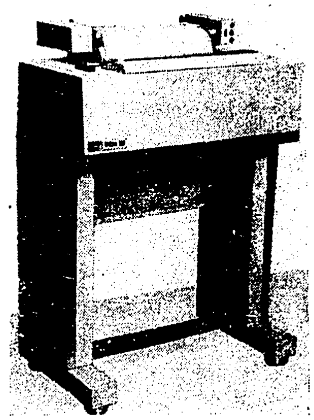


Fig. 12. SM-6302 printer

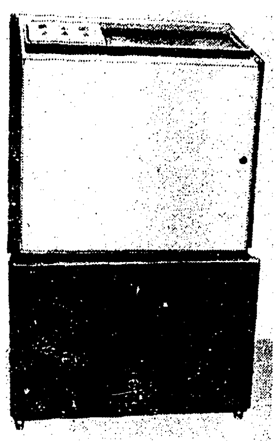


Fig. 13. SM-6316 printer

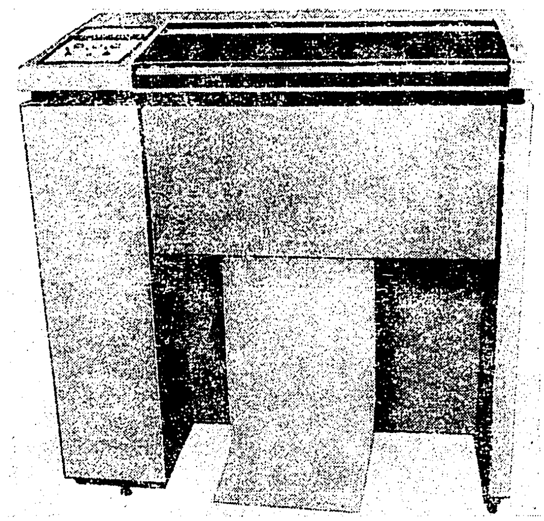


Fig. 14. SM-6321 printer

Technical Specification of Sequential Printers

Code	SM-6301	SM-6302
Country	E. Germany	Poland
Printing speed, sign/sec	100	180
Number of symbols/sec	96	128
Number of symbols/line	Up to 132	Up to 132
Number of copies	Up to 4	Up to 5

Technical Specification of Parallel Printers

Code	SM-6316	SM-6321
Country	Hungary	Hungary
Printing speed, line/min	365	650
Number of symbols in set	96	96
Number of symbols/line	Up to 80	Up to 132
Number of copies	Up to 6	Up to 6

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POLISH MAGNETIC TAPE MEMORIES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 154-157

[Article by M. Vaytsen, Poland]

[Text] The YES-5019 magnetic tape memory (Fig. 1) is designed for recording data used for input and storage in Unified System computers.

The memory enters and reproduces information on magnetic tape 12.7 mm wide according to ISO standard. In entry, the NRZ-1 method is used (remagnetization without return to zero, change of direction corresponds to unity, lack of magnetization designates zero).

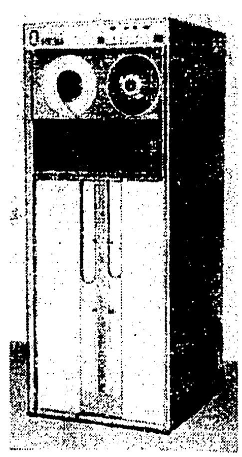

Fig. 1. YES-5019 mag tape memory (plant code RT-3)

At the front part of the memory is placed organic glass which is moved aside to replace the magnetic tape reels. The glass has an auto-lock. Above the glass is the operator control console. Indicators signal to the operator the actual status of magnetic tape memory.

The basic units of the magnetic tape memory are as follows: tape advance and drive, recording and playback heads. In the YES-5019 memory is used a modern single-roller drive with vacuum compensating posts. The arrangement of tape on the posts is determined by a photoelectric sensor which controls movement of the reels. The drive roller is placed on the axle of a quick-response motor. The record and playback unit has a type GPT magnetic head made of solid ferrite. Because of the use of silicon IC, the reliability of the automated circuits is greatly increased.

Technical Specifications

Tape width, mm	12.7
Tape length, m	732
Number of tracks	9
Rate of tape motion, m/sec	3
Rate of data transmission (8-bit sign), sign/sec	96,000 or 24,000
Rated distance between sectors, mm	15.2
Recording density, lines/mm	32 and 8
Reading of stored data	In both directions
Start (stop) time, msec	3.5
Rate of tape rewind, msec	~5
Power supply	3 × 220 VAC, 50 Hz
Consumed power, kW	1.5
Size, mm	670 × 700 × 1700
Weight, kg	~350

The magnetic tape memory YES-5112-02 (plant code RT-5). The basic design of the memory consists of a rack frame, movable frame with mechanisms, side and rear casing, ventilation unit, magnetic heads, with cassette unit removal device, and operator console.

Technical Specifications

Tape width, mm	12.7
Number of tracks	9
Density and method of recording, lines/mm:	32 (NRZ-1 method) 63 (FK method)
Maximum rate of data transmission, K byte	100 (NRZ-1) 200 (FK)
Average working speed, m/s	3.17 ± 1%
Total reel rewind speed, sec	60 (for 10 1/2" reel)
Start (stop) time, msec	3
Rated distance between sectors, mm	15.2

Number of tape passes in contact with magnetic head	100,000 (with retention of the number of errors specified in the technical conditions)
Tape loading	Automatic, from reel with or without threader ring
Maximum automatic loading time, sec	30

The number of playback errors in memory operation without correction of playback information of no more than one zone with an error (bit) per 1.1×10^5 correctly reproduced the zones (10^9 correctly reproduced bits). Constant errors are not permitted. This parameter is observed for both recording densities with an average zone length of 1024 lines.

The magnetic tape memory YES-5002-02 provides for exchange of data recorded on the tape with data on other devices satisfying the same requirements with respect to method and arrangement of recorded information.

The cassette type magnetic tape memory YES-5091 (Fig. 2) is designed for storage of data in ADP systems. The memory enters and plays back information on magnetic tape 3.81 mm wide. The magnetic tape is in a standard type "Compact" cassette and moves over the magnetic head which enters, reads and erases data according to ISO standard. Recording is done by the FK method.

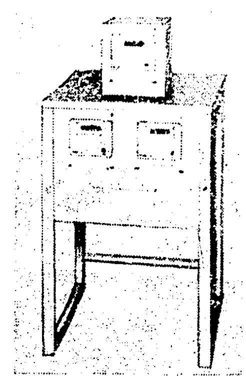

Fig. 2. YES-5091 mag tape memory (plant code RK-1)

The cassette type magnetic tape memory has a modular structure and consists of three modules: drive, electronics and automation, and grid power supply. This design permits easy change of modules and creation of cassette memory systems. The device determines the arrangement of the cassette, start and end of tape, enables recording of data.

The cassette is automatically locked after applying and sampling given memory. The cassette is removed by pressing a button. The electronic circuits are built on semiconductor elements and ICs. Recording and reading on magnetic tape is done by a ferrite single-track dual-gap magnetic head.

Technical Specifications

Cassette type	COMPACT
Tape width, mm	3.81
Tape length, m	90
Number of tracks	2
Rate of tape travel, m/s	0.127 ± 3%
Maximum rate of data transmission, bit/s	4,000
Rated distance between sectors, mm	20
Recording density, bit/mm	32
Readout of recorded information	In two directions
Start (stop) time, ms	40
Rate of tape rewind, m/s	2
Power supply	+15 V ± 3%, 1 A -15 V ± 3%, 1 A + 5 V ± 3%, 1 A
Weight (without grid power pack), kg	3
Dimensions (without grid power pack), mm	180 × 180 × 200

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PROGRAMMING SYSTEMS FOR THE YES-1030 COMPUTER

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian
No. 5, 1979 signed to press 4 Apr 79 pp 157-162

[Excerpt from article by St. Lepetov, Poland]

[Excerpt]

The YES-1030 electronic computer produced in Poland is a highly efficient computer of medium productivity with operating memory up to 1 megabyte and diversified set of peripheral devices.

In the article is described the system of programs permitting most efficient use of the YES-1030 computer:

Large management systems;
Information retrieval systems;
System for scientific and technical calculations;
Engineering systems;
Programming language converters.

[207-8617]

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PROGRAMS FOR REALIZING MATHEMATICAL METHODS IN THE OPERATING SYSTEM OS YES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 162-174

[Excerpt from article by Kh. Verner, East Germany]

[Excerpts]

In the framework of Unified System of Computers, high productivity computers primarily use the operating system OS YES. Experience shows that with an increase in computer productivity there is also a rise in expenditures for preparing it for use. Preparation for use and application of the computer may be facilitated, however, by using ready programming software.

Below is cited a list of programming systems (SP) and program packages (PP) elaborated by the scientific and industrial combine "Robotron" for the operating system OS YES.

Notation	Purpose
PS OPSI	Linear, separable optimization and fractional linear optimization, including single parameter expansions, vectorial optimization
PP DISKO	Optimization "0-1", mixed integer optimization, optimization of transport
PP STATISTIK	Mathematical and economic statistics
PS SIMDIS	Simulation of processes based on discrete models
PP NETZPLANTECNIK	Planning and monitoring periods, summation and balance of resources
PP NUMERISCHE MATHEMATIK	Matrix calculation, linear systems of equations, integration, differentiation, polynomials, etc.
PP YEDO OS YES	Unified organization of data bases for PP and SP of mathematical methods

Information on Applied Programs which Have Passed Compatibility Tests

Applied Program Package "Planning of Capacity" (PPP-PM)

Developer: Bulgaria, USSR
Date of joint tests: 2 Dec 75
Operating system: DOS YES, Version 2.1
Minimum volume of operating memories: 64 Kbytes
Programming language: PL/1

Field of Application

At enterprises with discrete type of production for computing load of industrial capacities.

Brief Description

The basic purpose of PPP-PM package is to establish a correlation of throughput of work sites with the industrial plan of the enterprise. The package can be used in planning the load of industrial capacities for a selected period of current planning and in determining the industrial program for the following year.

PPP-PM consists of a set of programs which analyze the course and sequence of execution of the program, create a systems operation base, create entries of work sites in the systems operation base, compile date tables, select working parameter values, set up matrices of transport time, create load bases, and compute the load of work sites according to the planned periods.

All programs of the package consist of modules and are generated according to the parameters of the macro-instruction CP[illegible]ST, selected by the user.

Minimum Configuration of Computer Under Control of DOS YES

Magnetic disk memories	2
Magnetic tape memories	1
Alphanumeric printer	1
Punched card reader	1
Card punch	1
Operator console	1

Compatibility tests were carried out on the YES-1020 computer.

Applied Program Package "Shop Management" (PPP-UTs)

Developer: USSR, Bulgaria
Date of compatibility tests: 30 Nov 76
Operating system: DOS YES, Version 2.1
Minimum main memory: 64 Kbytes
Programming language: PL/1

Field of Application

The applied program package "Shop management" (PPP-UTs) is a component part of the information system of production management. It is designed for use in the ASU of machine and instrument construction enterprises with discrete production and a complex end product.

Brief Description

PPP-UTs program packages provide shop managers with information on the initiation of orders and their transit through production. This permits the management of orders in the entire industrial cycle. To bring about this, the PPP-UTs realizes the following functions: presentation of orders to production, processing of information on open (presented to production) orders, retrieval and presentation of operational information on the status of open orders, compilation of industrial assignments for incomplete operations in the planned period.

It is possible to include user programs intended for processing report information during production and updating information base on the basis of this information.

Minimum Configuration of Computer
Operating Under Control of DOS YES

Magnetic disk memory (for programs and data)	2
Magnetic tape memory	1
Alphanumeric printer	1
Punched card reader	1
Card puncher	1

Compatibility tests were run on the YES-1020 computer.

Applied Program Packages for Systems of Monitoring, Conversion and Correction (PPP KKO)

Developer: Czechoslovakia
Date of compatibility tests: Sep 76
Operating system: MOS YES
Minimum memory: 64 Kbytes
Programming language: Assembler

Field of Application

In all fields of the national economy for processing data bases on punched cards.

Brief Description

The KKO monitoring system transfers data bases from punched cards to magnetic disk, and the following monitoring and correction functions are performed:

Monitoring of data within a single entry;
Monitoring of logical relations between data entries and catalogue entries stored on magnetic disks. Catalogues may be entered sequentially or in indexed sequence;
Monitoring of completeness of data bases by the method of monitoring of sums;
Correction of bases in which an error is detected.

Minimum Configuration of Computer Operating Under Control of MOS YES

NMD	1
Punched card reader	1
ATsPU	1
Operator console	1

Compatibility tests were run on the YES-1020 computer.

<u>Applied Program Package "Operational Planning of Production" (PPP-OPP)</u>

Developer: Czechoslovakia
Date of compatibility tests: 18 Jun 77
Operating system: DOS YES, Version 1.3
Programming language: Assembler

Field of Application

In an industrial enterprise with serial type of production with the possibility of operational planning in natural and financial expressions, planning of industrial capacity and work site load.

Brief Description

The program of this version PPP-OPP makes it possible to break up the pre-set plan of production into separate components, to draw up a requirements graph for separate components and separate stages of the plan and thereby balance the need for specific components in industrial capacities.

The plan can be drawn up with or without consideration of the dynamics of production with calculation of industrial advances.

The program permits continuous comparison with the actual status of production and response to specific situations making the necessary corrections in the pre-set plan. Furthermore, PPP-OPP executes independent functions of industrial calculations with the entire spectrum of articles produced at the enterprise. PPP-OPP has a subsystem of automated management system MARS is linked with other subsystems, chiefly PPP-TPP.

The subsystem PPP-OPP consists of three modules: DISPO, Compilation of Material plan, and Creation of Industrial Capacity plans.

Minimum Configuration of Computer
Operating Under Control of DOS YES

Mag disk memory	4
Mag tape memory	2
Alphanumeric printer	1
Punched card reader	1
Operator console	1

Compatibility tests were run on the YES-1030 computer.

Applied Program Package "Labor and Wages Management" (PPP-UTZ)

Developer: Czechoslovakia
Data of compatibility tests: 16 Dec 77
Operating system: DOS YES, Version 1.3
Programming language: Assembler

Field of Application

In any sectors of the national economy to form basic information funds on persons participating in the labor process.

Brief Description

A system of programs PPP-UTZ designed for sequential creation of basic information on every worker participating in the labor process. The information fund contains information necessary for computing wages (salaries) and basic information for the personnel department and the planning and economics department. Furthermore, PPP-UTZ fulfills functions of monitoring of pre-set indicators of unified accounting of workers.

The subsystem UTZ consists of three modules: creation and servicing of the information fund, advance wages, differential piece rates, and calculation of wages--total and with deductions.

Minimum Configuration of Computer
Operating Under Control of DOS YES

Mag disk memory	3
Mag tape memory	4
Alphanumeric printer	1
Punched card reader	1
Operator console	1

Compatibility tests were run on the YES-1030 computer.

System MM--Set of Applied Programs for Tackling Jobs in ASU Data Processing

The principle of development of the system MM (developer, Hungary) consists in the fact that most programs in data processing in ASU may be related to standard program classes (verification of correctness of primary data, opening of tables, updating of basic data bases, retrieval of entries in the base, etc.).

System MM provides so-called standard programs for tackling specific types of jobs. The standard program realizes an algorithm which is typical for a given class of jobs. In tackling specific jobs it is necessary to supplement the skeletal algorithms with parameters of the given job (description of entry structure, structure of tabulograms, branching conditions in the course of execution of algorithms, etc.). For indication of parameters is used a special language AP (adapting parameters) and a translator from this language.

System MM is designed for the YES-1010 computer and for middle models of YES computers operating under control of the DOS YES operating system.

The first set of standard programs successfully passed the International Compatibility Tests after which a second set of programs with greatly expanded resources was elaborated.

[207-8617]

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ANNOTATIONS FROM "COMPUTER TECHNOLOGY OF SOCIALIST COUNTRIES"

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No. 5, 1979 signed to press 4 Apr 79 pp 180-182

[Excerpt from Annotations from the Journal]

[Excerpt] Kryukov, Ye. V.; Shokhin, N. N. Elaboration of the main module of BD SIOD oriented towards expanded data base.

Three methods are presented for generating the main programming module in the SIOD data base, requirements are cited for labor expenditures. Recommendations are made on the use of each method.

Blinov, V. P., Bazov, A. N., Shibanov, G. V. File archive in DOS YES.

A programming package is described "Organization and management of a file archive" whose basic purpose is to provide the user with means of automatic file management on magnetic tape. Shown are its functional resources, composition of catalogues and working with it, realization of functions of the user access to the archive.

Yermolayev, B. I. Questions of reliability of programming software of computing systems during its development.

The extent of error tolerance, a prediction of their occurrence, the balance of labor expenditures to eliminate them can be determined based on the theory of reliability considered in several aspects in the article as compared with the theory of reliability of hardware. Shown is the application of this theory to tackle the job of obtaining balanced reliability of programming software.

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