JPRS L/9826

6 July 1981

USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 16/81)

Excerpts from the Journal 'COMPUTER TECHNOLOGY OF THE SOCIALIST COUNTRIES'

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APPROVED FOR RELEASE: 2007/02/09: CIA-RDP82-00850R000400030007-7

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APPROVED FOR RELEASE: 2007/02/09: CIA-RDP82-00850R000400030007-7

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EXCERPTS FROM THE JOURNAL 'COMPUTER TECHNOLOGY OF THE SOCIALIST COUNTRIES'

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian
No 8, 1980

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APPROVED FOR RELEASE: 2007/02/09: CIA-RDP82-00850R000400030007-7

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COMPUTER TECHNOLOGY OF THE SOCIALIST COUNTRIES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 2-4

[Annotation and preface from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] This international collection deals with the problems of research, development, application and operating experience of computer hardware and software developed under the agreement on cooperation in computer technology between the socialist countries: the NRB [People's Republic of Bulgaria], the VNR [Hungarian People's Republic], the GDR [German Democratic Republic], the PNR [Polish People's Republic], the Republic of Cuba, the SRR [Socialist Republic of Romania], the ChSSR [Czechoslovak Socialist Republic] and the USSR.

Treated in this collection of articles are general development problems of the small computer system (SM EVM), specific hardware and systems for the SM EVM, software for the SM EVM and problems of application of SM EVM facilities in hierarchic multimachine complexes, computer networks and ASU's.

The collection is intended for specialists engaged in developing and using facilities of the YeS [unified system] and SM computers.

Preface

The level of automation of processes in the various spheres of social production is largely determined by the presence of mini and micro computers which thanks to microelectronic technology, advanced software, simplicity of maintenance and low cost are gaining more and more fields of application and becoming the most widespread class of computers.

Characteristics of the small computer system (SM EVM), developed in the socialist countries, were determined primarily by the needs of the countries for creating automated control systems (ASU), automating scientific experiments, automating design, and using computers in the nonindustrial sphere. The SM computer development program presupposes simultaneous development of hardware and software in the form of problem oriented complexes that will encompass the various fields of application.

Considering the large number of developments in the socialist countries, the experience of applying small computers in various fields and the great interest in this class of machines, this, the eighth issue of the collection "Computer Technology of the Socialist Countries," is devoted to this theme.

This collection includes both articles dealing with general problems of SM computer development in the socialist countries, and articles on specific SM computer hardware and systems (SM computer complexes, SM computer power supplies, floppy disks in SM computers and others) and software. Articles in the collection show the application of SM computers in hierarchic multimachine complexes, computer networks, automated control systems and for automation of design. The collection also includes articles on the SM-50/50-2, SM-50/10-1 and SM-50/40-1 microcomputer systems.

Without question, even a topical collection on small computers does not cover fully all the tasks and efforts underway in the cooperation of development of mini and micro computers, but from time to time we hope to return to this topic and publish articles on the most varied aspects of development and application of small computers and on the problems of their standardization, operation and maintenance.

The Editors

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DEVELOPMENT STAGES OF THE SMALL COMPUTER SYSTEM

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 5-10

[Article by B. N. Naumov, corresponding member of the USSR Academy of Sciences (USSR), from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The small computer system (SM EVM) is a modular complex of hardware and software intended primarily for use in real-time systems and organically tied to the requirements that the user dictates. Therefore, the selection of characteristics and determination of the nomenclature of the modules of control computer complexes (UVK) involves profound and broad analysis of user requirements.

The small computer system is being developed in several stages. The first phase of the small computer hardware development plan specified development of a functionally complete set of hardware during the period from 1976 through 1980 for configuration of various automated systems. This task was essentially completed in 1979. Within the small computer system, about a hundred different devices representing a functionally complete set have been developed, tested and are in production; this set enables building automated systems of varying complexity.

Four models of processors with different throughput, the SM-1P, SM-2P, SM-3P and the SM-4P (Poland, Cuba, Romania, USSR and CSSR), and a series of main memories and devices for systems complexing (Bulgaria, Hungary, Poland, USSR and CSSR) have been developed under the first phase of the program; these devices enable building systems with a variable configuration and wide range of characteristics. The small computer system includes a large set of peripherals: external storage on fixed and removable magnetic disks and on floppy disks, input and output devices operating with perforated tape and cards, serial and parallel printers, alphanumeric and graphic displays, equipment for transmitting data over telephone and telegraph channels, data preparation devices and devices for communication with an object.

The following table shows the number of devices by individual groups of equipment that successfully passed joint tests in the period 1977 to 1979 (second-phase devices that were tested in 1979 are also included in the table):

Equipment Groups	BU	HU	GDR	Cuba	PO	RO	USSR	CSSR	Total
Processors	-	-	2	1	1	1	4	2	11
Main Memories	1	-	-	-	1	-	2	3	7
External Storage Devices and Controllers for Them	7	4	-	-	5	-	2	3	21
Input-Output Devices and Controllers for Them	1	6	5	-	6	2	2	8	30
Terminals and Terminal Stations	-	5	1	1	1	-	1	1	10
Devices and Terminals for Communication with an Object	-	-	-	-	-	-	2	2	4
Data Transmission Devices	-	3	-	-	-	-	2	4	9
Data Preparation Devices	1	-	2	-	-	-	-	1	4
Inter- and Intrasystem Communication Devices	-	-	-	-	-	-	-	3	3
Other Devices	-	-	-	1	-	-	-	1	2
Totals by Country	10	18	10	3	14	3	15	28	101

Also tested in 1977-1979 were 28 software components--operating systems and application program packages.

The traditional sequence of developing software after completion of hardware development often leads to obsolescence of a system even before it is put into operation. The small computer system development plans specify simultaneous development of hardware and software, as well as control systems based on them in the form of problem-oriented complexes (POK). In the process, the technical level of control systems based on the small computer system is being raised considerably through the organization of distributed data processing in control systems using several compatible small computers. This raises system reliability and viability considerably, and in addition, by bringing out and localizing autonomous control loops, makes it possible to simplify and accelerate program writing and debugging which results in reducing the time needed to put a system into operation.

A large number of systems for various users based on one or several, if necessary, problem-oriented complexes are developed by varying the structure of hardware and software and elaborating the software with specific applied tasks. The most labor-intensive tasks of tying the hardware needed to the basic software under the concrete modes and conditions of operation are handled by the skilled specialists of the leading systems organizations and organizations-developers of the hardware when the problem-oriented complex is created.

Development of the first phase of the small computer system has led to a significant improvement in the technical level of the small computers produced by the industry of the socialist countries. The physical sizes of complexes have been sharply reduced (to about one-fifth of the previous size), cost has been reduced considerably (to about one-half of the previous cost), and reliability indicators

have improved (about twofold). This was achieved by shifting to microprogram control in processors, using microcircuits with a higher degree of integration and improved connecting pins, using small power sources and compact peripherals and by raising the manufacturability of the designs.

In 1977, the "Concept for Development of the Small Computer System (Second Phase)" was adopted; the basic directions for development were formulated in it. And in 1978, the "Preliminary Design, Plans and Specifications for the Second Phase of the Small Computer System" was accepted. Elaboration of the "Development Program for the Second Phase of the Small Computer System" is nearing completion. The concept, design and program set several goals. The major goals are:

fuller satisfaction of national economic demand for, and elimination of the shortage of, small computer hardware to build automated systems in various sectors and to perform autonomous design operations;

creation of the prerequisites for mass introduction of this class of hardware into the national economy;

improvement of the technical and economic indicators for the hardware, expansion of its functional capabilities and enhancement of flexibility, bringing the technical level of the small computer system closer to the level of the best modern small computers; and

raising the economic effectiveness of utilization of computer equipment.

Proceeding from these goals, the concept, design and program for developing the second phase of the small computer system envision a substantial expansion of the computer nomenclature with regard to specialization in the hierarchy of hardware, including in teleprocessing network systems.

The element base for this phase of computers will consist of three microprocessor series (sets) of large-scale integrated circuits distinguished for speed of response and power consumption. The sets are standardized in design and will have the necessary elements for matching of signal levels.

First phase models of the small computer system using second phase microprocessors will basically have the appearance of systems with processors-expanders. In these systems, the new system processors will be compatible with those of the first phase computers, the capability of realizing certain software functions by hardware will be provided, the central processor will be unloaded by having the processors-expanders perform a number of functions (input-output processors, file management processors, communications processors in multimachine systems, specialized processors, for example for Fourier transformations, and others). Using specialized processors in control and computer complexes will make it possible to increase average throughput in certain classes of problems by an order of one-two.

A substantial portion of the nomenclature of control devices--controllers for the peripherals will also be realized on the basis of microprocessors. In the process, the same functional modules may be used for operation with different peripherals. To perform specific prescribed functions, these modules will be programmed at the level of microinstructions or conventional instructions of microprocessors. This will make it possible to standardize hardware, reduce hardware outlays for realization of devices with fixed logic, increase flexibility during system design and implementation and raise reliability considerably.

In the second phase of the small computer system, it is planned to develop superior models that have considerably higher throughput (several millions of operations per second with a main memory capacity up to 1-2M bytes) than first phase models, with advantageous economic indicators. These models are intended for use in the upper levels of control systems operating in real time, where it is necessary to provide for acquisition and processing of large information streams or solving complex problems for which the throughput of conventional small computers is insufficient and the application of large computers is inefficient. These are, for example, systems for complex scientific research, systems for monitoring and testing complex objects and systems for control of fast-flowing processes.

The superior models will have a flexible architecture, ensuring program compatibility from the bottom up. Their architecture is also oriented to efficient realization of high-level programming languages to sharply reduce labor and machine-time outlays for development and debugging of complex application programs, to a rational combination of junior and superior models of the small computer system (as well as of the unified system computers) in multimachine complexes, and to the development of the principles of building multiprocessor complexes with specified reliability, viability and throughput.

Based on these prerequisites, five new classes of models are planned in the program for the second phase of the system of small computers.

The first class of models of second-phase small computers are the microcomputers built with microprocessor sets (models of the SM-50 class). This class is intended for mass application in systems for numeric program control, for building into complex scientific and measuring instruments, intelligent terminals and terminal stations for office work. Based on the SM-50 class of microcomputers, general-purpose controllers are being developed that will enable raising considerably system throughput by transferring some operating system functions to hardware.

The second class are the system compatible small computers of the SM-51 class that ensure continuity of the software and entire series of peripherals with first-phase models. The technical and economic characteristics of these models (speed of response, size, power consumption, storage capacity, etc.) must be substantially (two- to fourfold) improved compared to first-phase models by shifting to a new element base and more progressive technological design solutions.

The third class are models of the SM-52 class which have greater throughput, memory capacity and structural reconfiguration capabilities in the small computer system. Multiprocessor versions of the models are possible. SM-50 and SM-51 class computers may be used as input-output channels in these models. Being intermediates between small computers and unified system machines in their capabilities, these models are suitable for small problem-oriented networks in hierarchic integrated control systems.

Models in the SM-53 class are actually multiprocessor and multimachine complexes built with modules of the other classes, hardware for intermachine and interprocessor communication and integrated software which ensures a rational distribution of the computing process over the system facilities.

SM-54 class models are specialized processors that realize individual algorithms (such as fast Fourier transformation, matrix operations, etc.) by hardware and make it possible to obtain with these algorithms a very high throughput, exceeding that of large high-speed computers by an order of one-two. Using these processors in combination with models of other second-phase small computer system classes will make it possible to build efficient systems for data processing in the real-time mode in applications such as analysis and synthesis of speech, analysis of aerial photography, analysis of seismic prospecting results and others in which the application of today's computers is limited because of their low speed of response.

In addition to the new classes of models in the second-phase small computer system, plans call for development of a large number of new peripherals with rather high quality. Especially worth noting is that the second-phase small computer system will have a broad range of various types of terminal stations that, on the one hand, will be capable of autonomous data processing at the work station, and on the other, will provide user access to a higher-ranking computer network when needed.

In addition to the directions associated with development of hardware and computer complexes, a broad program of software development is planned. In the software development, consideration is being given to the specific nature of small machines, which does not permit giving the programmer a large choice of hardware as is done with large machines. On the other hand, the necessity of ensuring operation of the small computers in systems and in the required modes (real-time, burst, data acquisition, interactive, time-sharing) determines the expediency of developing a set of operating systems, each fo which efficiently realizes some one of these modes. Such systems are considerably simpler than the general-purpose systems of large computers.

To facilitate programming of various application tasks, development is underway on programming systems that would require the user to specify only the functions needed, relieving him of concern for how this will be performed. Efforts are also in progress to develop more efficient problem-oriented programming languages and the corresponding translators.

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SM-52/10 SMALL COMPUTER

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 10-13

[Article by Ya. Gantner, engineer, Hungarian People's republic. from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The experience gained while successfully developing the first phase of the system of small computers (SM EVM) and the effective use of these computers in various sectors of the national economy have determined the need for developing high-throughput small computers suitable for systems of hierarchic control and automation. Developing high-throughput small computers is a major task of the program for the small computer system.

Modern electronic elements, new technology, more efficient software and the experience of international cooperation on the YeS [unified system] and small system of computers have made it possible to begin developing the SM-52/10 model at the VIDEOTON plant (VNR [Hungarian People's Republic]).

The SM-52/10 has a flexible architecture which makes it possible to easily change the configuration of a system to match the problem to be solved. This computer can use the applications programs developed earlier for the small computer system, and at the same time, for more complicated applications, it has the capabilities offered by flexible architecture and programming.

In designing this model, the "3M principle" was realized: modularity (of hardware and software), microprogramming and a monobus system.

The main principles realized in developing the architecture of this model are:

optimal distribution of tasks between hardware and software;

support of a multifunctional mode by hardware and microprograms;

mutual protection of applications and systems programs while maintaining good communication between them;

capability of using software developed earlier; and

realization of advanced "self-diagnostics."

Realization of the design principles makes it possible to simultaneously solve different types of problems on one and the same (logical) computer while providing practically absolute protection of them from each other.* Division of the functions of the central processor is afforded by the technology of ESL- [emitter-coupled logic = ECL] (which up to now has practically not been used in small computers), TTL [transistor-transistor logic = TTL] and MOP-BIS [metal-oxide-semiconductor = MOS large-scale integrated = LSI circuits]. Floating-point or decimal operations are performed in supplementary units, and, for example, separate functions of file processing are supported by a microprogram memory realized in interface units (in some cases with a capacity up to 10 Kbytes).

The models have no traditional complicated control console; the method of remote loading of programs and the method of remote diagnostics have been developed and realized. The latter method affects the qualitative variation in hardware maintenance. To satisfy requirements primarily for management of small data bases, the model SM-52/10 has a main memory with a capacity up to 1M byte and auxiliary storage on disks with a capacity up to 200 Mbytes. The speed of the processor is maintained by buffer cache** memory by matching the transmission rate between the memory and other system elements. Terminal control and connection to networks is effected through synchronous and asynchronous lines.

The model SM-52/10 has a multilevel (64) system of interrupts. Instructions have the format of a word (16 bits) and data may have the format of a halfword (byte), a word (16 bits) or a double-word (32 bits) with floating decimal. The microprogram memory is made in the form of RAM [random-access memory] on-line memory. Part of the memory is reserved for user needs, for example for expanding the system of instructions. An integral part of the central processor is the microdiagnostics which test the processor and cache memory and operate with each switch-on, but may also operate upon command from the operator's console.

The central processor consists of the following standard modules: interface, cache memory, arithmetic-logic unit and clock.

Besides the bus for memory and peripherals, the processor has a synchronous bus for rapid internal communication between processor modules and between the processor and special operating units.

The cache memory, in essence, is a "rate interface" between the relatively slow main memory and the fast arithmetic-logic unit built with ECL processor sets. The capacity of the cache memory is 8K words and each element in it is organized in the form of a pair of words: a word with an even address and a word with an odd address. Access to it during any reference to memory is effected by the low order bits of the even address. If the word sought is in the cache memory, then communication with the main memory is not required, as a result of which execution of operations with reference to memory is accelerated considerably (approximately 90 to 95 percent of the operations using memory are executed with the cycle time of the cache memory, i.e., about 250 ns).

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* Up to now, this property had been the exclusive privilege of only large computers.

** A cache is a fast semiconductor memory.--Editor's note.

The arithmetic-logic unit is made with high-speed microprocessor sets of the bit slice type; it contains the arithmetic module and the control fields for the microprogram memory. Addressing of microinstructions, decoding of the instructions and checking memory segmentation is performed by the control module. The microprogram memory may be loaded, and the microprocessor updates it. The control microprocessor reads the main microprograms from the read-only memory [ROM] to establish the initial states, and other microprograms are read from main memory.

The operational units are used to raise the efficiency of the operations of FORTRAN (with floating point) and COBOL (decimal); the units provide for hardware execution of instructions oriented to high-level languages. The efficiency of various translating programs may be significantly enhanced by incorporating such special units.

The second processor, created from basic modules with microprogram memory, is used for emulation. It is possible to use a large number of such processors to realize other systems of instructions. Thanks to the high level of technology, the time for execution of instructions typical for emulated architectures is no worse than with the source modules.

The microprocessor interface units used for very high throughput peripherals unload the processor to a considerable extent. In essence, they are a processor, transformed into a functional exchange control unit and a unit for direct access to memory. These processors perform organization of data flow and control typical for a peripheral in an autonomous mode. In accordance with the modular principle, exchange processors differ from each other usually only in content of microprogram memory. More "intelligent" interface units provide for execution of many new functions for control of data transmission using interfaces created for various data transmission networks (for example, synchronous and asynchronous interface, X-interface according to ISO [International Organization for Standardization] standards and others).

The model contains integrated and high-throughput units for control of peripherals; in addition, there is the capability of connecting peripherals to a simple standard bus system. Used as peripherals (with regard to standardization) are the peripherals for the YeS and SM computers in accordance with requirements of throughput and economy. For man-machine communication, the most efficient and convenient ATsPU [alphanumeric printers] and displays with microprocessor control are used. Controls and indicators on this equipment have been designed with maximal regard for human engineering requirements.

The decentralized functions embedded in the hardware promote optimal selection of software and ensure balance within the bounds of "cost versus productivity" and "outlays for production versus cost of utilization."

The concept of the SM-52/10 computer and the schedule for implementation allow considering it as one of the first models of the second-phase system of small computers. It may be used extensively to solve the more complicated class of problems that impose special requirements on a computing system.

The author considers extremely important giving prompt assistance to users to train them to operate this high-throughput computer, since experience shows that use of the capabilities embedded in individual models depends on the degree of user training. The design of this model will make it possible to relieve the user of a number of routine maintenance tasks.

These efforts are being made in close international cooperation with users and scientific institutions with respect to critical evaluation of the operating experience of previous models.

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CSO: 1863/157

MODULAR CONCEPT IN DEVELOPMENTS OF GDR DATA PREPARATION UNITS AND TERMINALS FOR YES AND SM COMPUTERS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 13-19

[Article by G. Merkel, engineer, GDR, and H. G. Jungnickel, engineer, GDR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The decade of cooperation between the socialist countries in computer technology is part of the socialist economic integration. The Robotron Combine's contribution to this integration has been the YeS-1040 and YeS-1055 computers which are operating successfully in various countries, and the 10 devices in the system of small computers (among which are two second-phase microcomputers) developed and put into production (before 1979).

Robotron produces not only central processors for the YeS computers; it is a major producer of serial printers and peripherals, particularly data preparation units, data teleprocessing devices and various special-purpose terminals, displays, magnetic tape cassette storage units and optical readers. Mass production os such small computers as the Cellatron 8205 and the Robotron 4000/4201 have made it possible to acquire experience for participation in developing the SM computers.

In accordance with the specialization in YeS and SM computers, the tasks of the collective are:

to expand production of the YeS-1055 computers. The modernized version of this model will be equipped with a matrix module that will make it possible to solve the expression a + bc with a high speed and thereby increase 10 to 50-fold the speed of execution of this class of problems. The matrix module, made as an individual special processor supplementing the standard processing unit, will allow direct transmission between the matrix module and storage. Efforts continue to further modernize the YeS-1055 computer. For example, it is planned to increase the capacity of the main memory to 8 Mbytes, using semiconductor highly integrated memory circuits;

to participate in developing operating systems and application program packages for the second series of YeS computers. The program package developed in the GDR provides the capability of using Unified System Computers on the virtual machine principle, which will allow achieving high efficiency in developing user programs. The shift to using new efficient operating systems is being facilitated;

to make full use of the expertise and technical and economic potential in developing small computers, peripherals and storage units for the YeS and SM computers and data preparation devices. In the process, it should be oriented to the areas in which the equipment developed by the combine has been used with success for many years now. These are banks, financial agencies, trade organizations, agricultural enterprises, statistical adminsitrations, railroad administrations and the entire area of economic calculations in industry, construction and other social areas.

Basic Hardware Requirements. The hardware under development to meet user demands is used more and more in various fields of science and technology. In connection with this, new requirements for them are also emerging. Studies and analyses were made of user requirements for hardware in which man is allocated the role of operator-executor. Based on these trends in computer application, an analysis was made of those fields of application in which

a clear shift has been noted from autonomous small-scale data processing to complex data processing (among which are teleprocessing systems with central computers of the YeS and (or) SM systems);

data preparation requires new engineering solutions, primarily in problem-oriented intelligent terminals directly in the workplace; and

use of terminals with broad problem orientation in teleprocessing systems will make it possible to substantially raise the efficiency of control processes (in the field of mass servicing and production, in financial institutions, etc.).

In these fields, the hardware is used under conditions differing from those, for example, in automating an industrial process. To obtain a solution effective for computer users, both general and specific requirements must be considered.

General Requirements Imposed by Users on Hardware.

1. Clarity, i.e. the operation of people with a system must look simple, despite the complex processes occurring in the system.

2. Capability of system expansion. Usually for the user, the fundamental requirements are:

capability of simple forms of expanding the configuration, for example by peripherals and additional memory (as a rule, this requirement is being met);

capability of system expandions: expansion of the capacity for addressing, the list of instructions, connection of compatible units of devices for proportional increase in the overall throughput of the equipment (for example, connection of large external storage devices without overloading the channels);

capability of using efficient compatible programs, programming languages, data bases or files, and operating systems;

capability of simple adaptation of the system to new user requirements, i.e. flexibility, for example, by replacing microprograms.

3. Unity of principles of solution. This requirement significantly raises system operation efficiency:

common engineering solutions allow the user to reduce the quantity of spare parts and time for training maintenance personnel, and to reduce downtime and repair time;

common logical and functional principles make it possible to better track system operation within a device and between different devices, make it easier for users to develop program packages for various fields of applications, reduce outlays for operation with devices and simplify maintenance of the different system units.

4. Adaptation of hardware and software to human habits. The most abundant requirements are dictated by human engineering: location and layout of the keyboard, location of the display and text on a screen, referencing various devices and data media (for example, changing magnetic tape cassettes). Other human engineering criteria are adaptation of shape and color to the environment, and consideration of human habits in organizing machine operation. For example, the custom of letting the operator see immediately the symbol input by him through a keyboard on a screen or printer. Waiting in the course of a second makes him unsure and lowers productivity. However, if the computer response appears immediately on the screen during interactive mode operation while solving complex problems, an operator tends to feel that he is being "urged on" and he tires quickly. A waiting time of 1 to 2 sec. in solving such problems may be considered a fast response. But if an operator has to wait more than 5 sec. in solving simple problems, his work rhythm is disrupted. In this sense, adaptation calls for extensive system analysis.

5. High system reliability. For example, terminal reliability must be more than 98 percent for the commercial user. However, high reliability must not be achieved through high economic outlays.

6. Small outlays for teaching programming and maintenance of the various system devices.

These requirements are equally legitimate for YeS and SM computer users. Development of standardization and modularity of this equipment has determined the task of developing a common technology for analogous directions of application of YeS and SM computers with regard to reasonable compromises with respect to interfaces, control procedures, etc.

Specific User Requirements. Specific requirements for hardware to be developed are defined by the working process of users. These requirements include various data media adequately equivalent for the user, various logging equipment, use of various programming languages, etc. For example, it is natural for a user used to working with magnetic cards to want attachments for processing these cards on new accounting and office machines, and for the user who has not worked with magnetic cards to want floppy disks. Terminals used in banks and those used to make reservations are almost the same in the interactive procedure. Both terminals are elements of a multiaccess system controlled by a computer and require response time on the order of a second, etc. But there are specific differences: the technique of printing tickets and reserved seat tickets differs completely from issuing bank documents or making entries in savings-bank books.

These legitimate specific requirements limit the selection of hardware for maintaining a dialogue and presenting the results (parameters, entries, data) to the user.

These facts were used in developing the new concept: the modular concept for the units was compiled in accordance with general system requirements. Specifications of the YeS and SM computers were considered as general conditions.

General system concept of autonomous devices, complexes and subsystems. The basis of the sets of data preparation units, devices for communication with a computer, and microcomputers developed at the Robotron Combine were the features of application discussed, general specifications, and the general and system provisions of the YeS and SM computer systems. Development proceeded according to the following basic rules.

1. Problem-oriented complexes and individual devices, as items to be marketed, are developed on the basis of standard units and devices, unified operating systems and software components, as well as problem-oriented special units and problem-oriented software components.

2. The set of unified units and individual devices is restricted; they are developed as general-purpose as possible and are subject to strict standardization. Used, for example, are:

the two main trends of unified units of microcomputers of the SM-5040-2 type as the 8-bit version and the SM-5050/5110 as the 16-bit version, compatible with the architecture of the system of small computers;

two types of serial printers, compatible design and system engineering wise, with a rate of 30-400 characters per second;

three main types of video monitor units;

two basic types of keyboards; and

a unified series of power modules and a whole assortment of other peripherals in accordance with the design specifications for the system of small computers, including a considerable number of purchased units from the nomenclature of the YeS and SM computer systems.

3. Items are developed within the bounds of a common basic design in various forms of execution based on CEMA standard No 834-77. This common basic construction allows common design realization of seats, console devices and table devices. Production is carried out by common industrial methods. These design solutions realize the basic provisions of the system of small computers, are efficient for advanced devices of the unified system of computers and meet the requirements for application of modern microelectronics.

4. The individual devices and complexes for application, used as a remote terminal or subscriber's station within data teleprocessing systems, presuppose efficient adaptation to the various control procedures and transmission algorithms which have already been adopted or must be adopted in the YeS and SM computer systems. In addition, facilities are offered for efficient adaptation to specified operating systems.

5. For rational development of problem-oriented programs outside the bounds of the proposed extensive standard assortment, efficient technology exists, including appropriate aids for programming and complexes for developments, which may be offerred also to major users and thereby will make it possible to reduce the continuously increasing outlays for programming.

6. The set of unified assemblies and units, software components and special components is an open system, i.e. it is continuously supplemented within the bounds of the specified principles.

A series of devices and problem-oriented complexes within the YeS and SM computer systems has been and is being developed on this basis. The first of these devices and some basic modules were shown at Moscow at the Second Joint Exhibit of the Computer Technology of the Socialist Countries (1979):

the Robotron MFG 20--a general-purpose programmable terminal made in the form of an individual work station;

the Robotron DEG 20--a programmable device for data preparation with properties of a terminal (desk-top device);

the Robotron PRT 20--a programmable complex device for reservations, also with properties of a terminal;

the Robotron MRES 20--a system for development of programs for all items based on the 8-bit SM-5040-2;

the SM-5040-2 microcomputer;

the Robotron 1152 serial printer; and

the Robotron K 5251--a device with cassette magnetic tape conforming to the ISO standard TC 97/2-35.

System diversity of devices may be achieved based on the unified core of a control computer and strict unification of other main components. This approach made it possible to focus efforts in software development on the more important problems and to combine the principle of modularity with high throughput of operating systems.

The Robotron Scientific Production Combine is also working on 16-bit microcomputers with varying capacity, and these are used as the basis for developing efficient problem-oriented complexes and devices to control data teleprocessing. These complexes and control devices are, for example:

complete minicomputers for scientific, technical and economic problems in all spheres of the economy. GDR efforts in minicomputers enter fully into the program for development of the system of small computers. These machines may be used both autonomously and in direct communication with a computer as a terminal or subscriber station for a YeS computer. Their configuration has a large set of peripherals of the system of small computers, multiplexors and general-purpose terminals. Offered as operating systems are primarily the SM computer operating systems for computing centers oriented to disk storage, the SM computer operating system for application in real time and software for the base computer, especially for a YeS computer;

general-purpose systems for data preparation for autonomous preparation of mass information at enterprises, combines, research institutes and other institutions or for direct communication with computers. Here too the system control unit of the SM computer serves as a central core, to which along with the most varied peripherals are also connected multiplexors and terminals (primarily problem-oriented). In addition to general-purpose operating systems, special software components are needed. Subscriber stations of the YeS-8505 or YeS-8506 type will be developed further by connecting other special devices for preparation of production data and production control;

a series of multiplexors and concentrators. Modular structure will allow realization by common concept of several versions of data teleprocessing control units with regard to the latest requirements. These devices are intended for use in YeS computer networks and may as a multiplexor have a YeS computer channel adapter or process YeS computer control procedures as a concentrator; they may also be used for similar functions in the system of small computers. In addition to data transmission control through various interfaces, these devices are used to monitor control and teleprocessing of information, and to realize such problems of data teleprocessing as code conversion, buffer storage of messages, message processing, adaptation of procedures, addressing of channels, message distribution, etc.

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DEVELOPMENT OF SMALL COMPUTERS IN CUBA

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 19-23

[Article by L. H. Karrasko, engineer, Republic of Cuba, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The development of small computers, begun in the Republic of Cuba in 1969, for automated systems for real-time control and monitoring of the sugar harvest is being continuously improved. Subsequently, the program of research and concrete developments received an additional orientation to new objects where these systems could be applied with great effectiveness. In particular, the research program was aimed primarily at implementing a system for planning and management of the national economy, as well as technical, scientific, social activity and others. A major task was developing hardware for export.

The small computer development program in the republic includes not only designs, plans and specifications for the short term, but is also part of a long-term program for computer hardware development in the Republic of Cuba to 1990. A major characteristic of the effort on development of computer hardware (SVT) is that it is determined by the problems, methods and forms of international cooperation that are specifically expressed in the Agreement on Multilateral International Specialization in Developing and Producing Computer Hardware, adopted by the MPK po VT [Intergovmental Commission on Cooperation between the Socialist Countries in Computers].

Specialization by the Republic of Cuba has special importance for successful development of computer technology in the country, since it will allow applying high throughput machines and progressive technology, building enterprises with optimal scales of production ensuring their high profitability, and conducting an effective export policy. On this basis, cooperation between the Republic of Cuba and the countries participating in the MPK po VT is being improved and expanded.

The participation of Cuban specialists in the work of the MPK po VT has made it possible to exchange information on the status and evolution of this complex technology, to cooperate in scientific research and design, to forecast and implement scientific and technical analysis and exchange technical documentation. Cuba's participation in the agreement on specialization and cooperation in computer production guarantees the country high economic effectiveness in the production, export and import of this equipment and at the same time allows achieving a high technical level and quality in production.

The SID-201 Series of Small Computers. The first group of models of SID-201 small computers were developed over the period from 1969 through 1977. It includes four type models: the SID-201, SID-201A, SID-201B (basic) and the SID-201B (expanded). These models were not compatible with the unified models developed in the other socialist countries. The SID-201 series of small computers is not a family; it is a development of a set in which the technical structure or architecture has one common line (set of instructions, memory word size, system of addressing and others). The early models of this group were the components for the later ones.

The first system, designed and built in 1969-1970, was the model SID-201. It confirmed the capability of producing it in Cuba, despite the great difficulties in providing for the technology of production. The system SID-201 was used in sugar plants, particularly for organization and monitoring of rail transportation for the sugar industry. It was noted that with generalization of some characteristics and connection of a minimal number of peripherals, this system could be used not only in the sugar plants, but in any other sector of the national economy. To this end, the system SID-201A with expanded software capabilities was developed.

The model SID-201A was the first computer put into series production in 1970-1972. The series was comprised of 20 units; in the process, more modern technology of production was achieved, and system reliability and economy was raised. System throughput is 25,000 to 50,000 operations per second; the main memory with a capacity of 4K words with 12 bits each is organized into pages of 128 words each; there are four forms of addressing memory. This system furnished classroom and on-the-job training for specialists in this technology.

The model SID-201B (basic) was developed in 1972 and its production was begun in 1973. This model had greater capabilities than the SID-201A; the experience gained in designing and producing the previous models was taken into consideration in the development. The main memory was organized on a modular basis which made it possible to increase the capacity from 4 to 32K words. The instruction set was expanded 1.5-fold, and a system of interrupts from peripherals was provided. Software was improved and the number of programs increased. According to assessments by Cuban specialists, there was about a 10-fold increase in power and operating capabilities with the SID-201B (basic) system compared to the SID-201A.

This model underwent further development in an expanded configuration, where the central processor in general features was the same as that in the SID-201B (basic); interface units and a direct-access channel were added, which significantly increased the system's technical capabilities, having provided the capability of connecting a large number of peripherals. Development began in 1975 in connection with the need of introducing a new system for managing and planning the economy in the country. The system has fundamentally new characteristics compared to previous one: input of standard perforated cards at a rate of 320 cards per minute and an interface of peripherals through slow and high-speed channels make it possible to transmit data at a high rate without delay.

The model SM-2302 small computer (SID-300) is one of the first results of the unified direction of developments and production of computer equipment by the countries participating in the agreement adopted in 1975. Development of this computer began in 1976. Three pilot models were developed which successfully passed joint international tests in the USSR in 1978. This computer was included in the

family of the system of small computers with the designation of SM-2303. The SM-2303 is now being put into series production.

In its element base, architecture and software, the SM-2303 is among the advanced models produced in the socialist countries. The element base (developments of the socialist countries) has a medium and high degree of integration. Thanks to the standard interface, a number of different peripherals may be connected to it, beginning with electromechanical and ending with magnetic with large capacity. The instruction system is more powerful than in the small computers of previous models. Twelve forms of addressing allow increasing the efficient rate of computation and facilitate using the computer. The system of interrupts has four levels of priority which considerably increases the power of the machine and also facilitates operating it.

The model SM-50/40-1 microcomputer (SID-400) was developed completely on the basis of large-scale integrated circuits (BIS) and microprocessor sets developed in the socialist countries. This model has perforated tape input and output and additional storage on floppy disks. The system is useful wherever automation of engineering and adminsitrative activity is being delayed because of the high cost of small computers, and also because of the requirements for their operating conditions; this is primarily the small enterprise or specialized department of economic activity. Up to now in Cuba, this problem had been solved partially through import of calculating machines, which besides their high cost had other shortcomings too, such as relatively low productivity, limited application, much space occupied, etc. Development of a family of SM-50/40-1 machines will make it possible to avoid these shortcomings.

The microcomputers will also be used as elements of the SM-2303 system of small computers (modular construction) and in computer networks.

The SM-7203 Video Terminals (SID-702). Development of peripherals has been proceeding along with development of the small computer system. The first result is the SM-7203 (SID-702) alphanumeric video terminal. Three pilot models were developed which successfully passed joint international tests in 1978.

The SM-7203 has a set of 64 different ASCII [American Standard Code for Information Interchange] characters; 20 lines of 72 characters per line may be displayed on the screen. There is also a standard alphanumeric keyboard. The terminal operates in two modes: standalone and with a computer. Among the capabilities this unit offers users are:

blinking or normal cursor indicating position of next character;

insertion or deletion of characters or line of text;

cursor movement in any direction, position by position or continuous;

adjustable margins for text being transmitted; and

scrolling.

The terminal has an audio signal to indicate line or screen margin.

Future developments. Under development now is a more powerful computer (the SID-300/20), compatible with the SM-2303 as well as with other models of the system of small computers. This new model will have a higher degree of integration and a larger main memory.

In the development of microcomputers, research and development is underway on new, more powerful machines (the SID-400/20); and solutions are being sought to expand their application in the national economy.

Development is also proceeding on several models of video terminals, based on components of larger-scale integration, including a microprocessor.

Unity in the engineering policy for development ensures assimilation of new models without special additional efforts (particularly in training specialists to operate them), as well as the capability of development of application and the compatibility of systems.

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PRINCIPLES OF BUILDING MULTILEVEL AUTOMATED CONTROL SYSTEMS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 23-29

[Article by R. S. Sedegov, doctor of economic science (USSR), V. A. Bashko, candidate of economic science (USSR) and A. M. Shipulin, engineer (USSR), from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The shift to development of complex systems with automation of control at all of its levels has become a real necessity and characterizes the new stage in the development of ASU [automated control systems = ACS]--multilevel automated control systems.

The lack of a unified concept for building systems to control production (associations, combines, enterprises) causes the emergence of various, often contradictory, requirements for the organization and technology of developing and implementing the systems, and makes it impossible to establish general norms, rules and standards, and prescribed procedures for the development, implementation and functioning of the systems. Therefore, it is becoming especially urgent to develop a systems methodology for building multilevel ASU's that ensure coordinated control of the various production and industrial objects, integration of control procedures and methods, and integration of the processes for design of the controlled objects and control systems, as well as their assimilation and functioning.

A multilevel automated control system is a complex man-machine system based on a computer and teleprocessing hardware, intended to obtain needed data and to control an association and its structural units. It realizes control of an association, the enterprises and industrial processes, coordinated in goals, criteria and procedures for data processing. A multilevel ACS includes these levels: the upper level--an ACS for a production association (ASUPO), the middle level--an ACS for an enterprise, branch, shop or section (ASUP), and the bottom level--an ACS for industrial processes (ASU TP).

A multilevel ACS must ensure output of a product with the least physical, manpower and cost inputs. The use, parallel with traditional control methods, of uncoordinated systems for control of individual industrial and organizational processes does not, in the majority of cases, yield the necessary efficiency of control. The determining role in the development of a multilevel ACS is played by the mutual coordination of the purposes of control at all levels and the well-grounded selection of

the criteria of efficiency in strict accordance with the established purposes of control, participation of administrative personnel in development of the systems, and organizational, hardware, software and data compatibility. In a multilevel structure of an integrated system for control of an association and an enterprise, each control unit must perform the tasks of the senior unit and in turn establish the target tasks, limitations and criteria for the control units subordinate to it.

A multilevel ACS is a complex control system with a trilevel structure that realizes the following directions of integration:

functional-purposeful (unity of purpose and a system of coordinated criteria);

organizational (rational combination of administrative activity of personnel and the ACS);

software (combined and interrelated complex of models, algorithms and programs);

informational (unity of sources and files of data); and

hardware (unification of the hardware complex to raise the throughput and reliability of the computer data network).

A multilevel ACS must perform the selected functions of control of specified objects on the basis of

coordination of goals and the problems that are to handled by the system and its individual subsystems (components);

formulation of a rational structure of the control system;

interlevel exchange of information;

coordinated solution of control problems of the different levels; and

organization of interrelation between automated systems for planning, accounting and monitoring and systems of industrial automation.

Development of a multilevel ACS is a complex problem, for the realization of which the countries of the socialist community have been enlisted within the framework of the Council on Application of Computer Technology. In developing a multilevel ACS, the following principles must be realized:

systems approach under the conditions of limitations on resources;

compatibility of all types of support (organizational, informational, hardware and software);

rational combination of centralized and peripheral hardware for data processing;

integration of levels by purposes, criteria and procedures of data processing;

maximal utilization of NIR [research] conducted by the socialist countries in accordance with the plans of the Intergovernmental Commission on Computer Technology; and

the capability of ACS functional evolution as experience is gained and new structures and industrial objects are connected.

The hardware complex (KTS) of a multilevel integrated ACS (IASU) is a complex system, consisting of interacting hardware complexes of the ACS's of all three levels, including facilities for acquisition, storage, processing, presentation and transmission of information, as well as the hardware to interface them, which result in solving the complex of problems of all classes of the multilevel ACS.

The intricate system of the hardware complex stems from the need of using various structures of hardware and methods of realizing the goals set (the problems). The hardware complex of multilevel ACS's must meet the following requirements:

capability of building hierarchic and multiprocessor computer complexes;

use of data transmission networks and teleprocessing facilities;

use of small computers for preparation and decentralized processing of data, and for control of industrial processes and equipment;

capability of acquiring valid data under the conditions of production interferences and personnel errors;

reliable operation of individual hardware complexes in an aggressive environment;

hardware, data and software compatibility;

validity of problem solving;

minimal outlays for hardware maintenance; and

short payoff period and high economic effect from introduction of the multilevel ACS.

As base equipment for the system's top level, third-generation medium and large computers--YeS and SM EVM [unified system and system of small computers]--must be used. The SM-1, SM-2 and SM-3 series of small computers must be used extensively at the bottom level of a multilevel ACS as machine-dispatchers, for preliminary data processing and for controlling industrial processes.

As network terminal equipment at the bottom level of an integrated ACS, subscriber stations and terminals that support data input and storage and output of results must be used. Two types of terminals are used: simple with hardware control and input-output equipment, and terminals with input-output equipment and a small computer for program control and preliminary data processing. Terminals operating in real time may obtain data from sensors, metering instruments, etc. The terminals developed may accept and put data into a computer and edit data. The most widely used terminals for a data teleprocessing system within the unified system are the subscriber stations. A subscriber station is one or several unified system peripherals with a special control device performing various functions.

A subscriber station collects, prepares and accumulates data for transmission to a computer, and inputs-outputs and displays data.

Software (PO) for a multilevel ACS must meet the following requirements:

use of a multiprogram real-time operating system for organization of data acquisition and processing;

availability of data bases for use on-line;

reliability of functioning;

restoration of status of data at a specific moment of time; and

maintenance of communications with the software at the different levels, both functional and informational.

These requirements, as well as a large number of problems in the multilevel ACS's, and the increase in communication and dependence between software components shape the development of the software in two directions: general systems and problem.

In addition to type procedures (input, sorting, etc.), the functions of general systems software include:

organization of system operation in the specified modes;

distribution of computing operations in accordance with their dynamic priorities;

monitoring the execution of computing operations;

timely preparation and input of data bases needed;

differentiated access to information in a data base;

monitoring the operation of terminals and small computers;

initiation of operation and control of a teleprocessing system; and

communication with the system operator and terminal operators.

Problem software functions are:

loading and management of the information base of normative-reference information;

loading and management of real-time informational bases for all levels of the ACS;

solving the problems of control automation; and

capability of restoring the status of the data.

These software requirements and functions determine the selection of the main components of the general systems software, namely: the operating system, the data base management system (SUBD) and the teleprocessing system.

In selecting an operating system, it is very important to take into consideration the capability of using application program packages developed earlier. Simultaneous operation of different operating systems in an integrated ACS is not ruled out. In selecting a teleprocessing system, the tasks of the multilevel ACS, the requirements for data processing from the user aspect and hardware capabilities must be considered. The determining factors in selecting a teleprocessing system are the type of base operating system selected and the data base management system.

The information base of multilevel ACS's is the aggregate of the unified system of classification and coding of technical and economic information and the unified systems of documentation and files of information used in all levels of the hierarchy. The components of the information base for multilevel ACS's are the data bases for the automated production association control system, the automated enterprise control system, the automated system for control of industrial processes and the data base management system.

Information compatibility of the functional systems means developing coordinated sets of classifiers and codifiers that ensure smooth exchange of information in the links of man-machine and machine-machine at all three levels (production association, enterprise, work place or industrial process).

One-time input of information for repeated use of it and centralized data processing must be provided for in the system. A centralized data base (TsBD) must be developed for collective use at all levels. Centralization of the information base within the framework of the centralized data base will make it possible to a considerable extent

to tie the ACS's of the different levels and the individual users together with respect to information;

to reduce duplication of data during storage of it;

to increase the identity of information thanks to one-time input and centralized management of it; and

to separate the processes of creating and managing the centralized data base from problem programs.

A centralized data base for a multilevel ACS must meet the following requirements:

concentration of information used at the different levels of the ACS and transmitted between them;

capability of partitioning for the different levels of the ACS as a function of priorities and user access restrictions;

simplicity and convenience of creating and managing;

validity of data without discrepancies;

efficient use of machine resources; and

capability of changing the composition and structure as the system evolves.

Also charged with information support of the ACS, besides the centralized data base, are the local data bases oriented to groups of users and even the individual users. Thus, the information base for a multilevel ACS is the aggregate of the centralized and the distributed data bases.

Under these conditions, it is important to properly select the criteria for building the information base and the methods for realizing it.

Problems of organization of development. Full preparation has to be made first of all in sectors of industry where multilevel ACS's are planned. It should be considered that multilevel ACS's will be created under conditions of change in structure and organization of industrial control and introduction of new general schemes for development and siting of production.

In preparing to develop a multilevel ACS in enterprises, there has to be modernization of the industrial equipment largely influencing the parameters of the entire production process.

This preparation, carried out with the use of modern facilities for control of equipment, will make it possible to create the conditions, with the lead time needed, for the overall technical and economic substantiation (TEO) for evolving the list of multilevel ACS's being developed.

Solving the problem of developing a unfied system of hardware to operate multilevel ACS's is of major importance. The solution must be based on integration of the programs to develop the various means of automation.

The intricacy and complex nature of multilevel ACS's require solving a broad range of scientific and methodological problems, efficient organization of production control, selection of methods of coordination and ensuring interaction of ACS components, and organization of the man-machine control systems. The most immediate problems should include: the systems approach, decomposition of the object of control, coordination of aims, inter- and intralevel integration, compatibility of system components and individual types of support, formulation of the target complex of tasks, adaptation, automation of design of integrated ACS's, coordination of components of integrated ACS's by preciseness, reliability and throughput, establishing rules for interaction and organization of communication between integrated ACS components, and methodological support for the integrated ACS's.

Let us examine, as an example, the problem of methodological support. It must be handled by the sectors charged with the responsibility for engineering policy in developing automated control systems. The methodological problem of developing a multilevel ACS should be solved within the framework of the scientific and technical program, "Development of a Unified System of Methodological Support for Development and Implementation of Multilevel Automated Control Systems." The senior level of this program must define the order of developments and implementation, and the composition and content of work on developing the multilevel ACS's. The second level of the program must prescribe the rules for development of the methodological materials defining the order of development, and the rules and norms for developing the different types of components for a multilevel ACS (an automated system for control of industrial processes, a system for automation of projection and designs, elaboration of organizational projects). The third level is the specific techniques for performing the individual efforts to develop the multilevel ACS and its components. The ultimate aim of realization of the program msut be a fund of methodological material for development of a multilevel ACS.

The distribution of developments of the functional systems--the parts of a multilevel ACS being carried out by the countries within the framework of multilateral cooperation is shown in the table:

ACS Level	System Code	Functional Systems	Developer Country
Top	101	Management of technical preparation of production	USSR
(ACS for production association)	102	Management of basic resources	Hungary
	105	Management of product cost	Poland
	106	Real-time control of basic production	USSR
	107	Technical and economic planning	USSR
	108	Management of product marketing	USSR
	109	Management of labor and wages	CSSR
	112	Management of R&D	Poland
Middle	201	Management of technical preparation of production	Poland
(ACS for enterprise)	202	Management of basic resources	Hungary
	205	Management of product cost	Poland
	206	Real-time control of basic production	USSR
	207	Technical and economic planning	USSR
	208	Management of product marketing	USSR
	209	Management of labor and wages	CSSR
	214	Product quality control	Romania
Bottom	301	Assembly process control	USSR
(ACS for industrial processes)	302	Control of mechanical processing lines	USSR
	305	Control of complex-automatic sections	Bulgaria
	306	Control of mechanized warehouses	Bulgaria, Hungary
	307	Control of test processes	Romania

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SM-1 AND SM-2 CONTROL COMPUTER COMPLEXES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 30-38

[Article by V. M. Kostelyanskiy, candidate of engineering science, USSR, and V. V. Rezanov, candidate of engineering science, USSR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] Two architectural lines have been adopted for the SM EVM [system of small computers]: a complex formed from the SM-1 and SM-2, and the other formed from the SM-3 and SM-4. The architectural lines differ only in the core of the computer complexes: processors, main storage, system peripheral controllers and system devices such as direct memory access channels, system interface branching devices, etc. Thanks to the effort to standardize interfaces, made within the framework of the system of small computers, the entire range of peripherals and a considerable part of the controllers for them do not depend on the processor architecture and consequently are common to both architectural lines.

The SM-1 and SM-2 control computer complexes (UVK) are intended for use in automated systems that control industrial processes and production, in experimental research complexes, for initial processing of test results, geologic reconnaissance data, medical and biological studies, and in information retrieval systems.

The SM-1 and SM-2 control computer complexes are built with the SM-1P and SM-2P processors according to client specifications from aggregate modules of the system of small computers using peripherals, when necessary, from the nomenclature of the system M-6000 (M-7000) ASVT-M [modular system of microelectronic computer equipment]. The SM-1 and SM-2 have full program compatibility with the M-7000 system and one-way compatibility with the M-6000 at the level of relocatable programs, as well as full compatibility with these systems on input-output interface. Based on the SM-2P processors, multiprocessor computer systems can be built with a common storage area and common or separate peripherals. In technical parameters and structural capabilities, the SM-1 and SM-2 complexes fully replace the M-6000 and M-7000 complexes, respectively.

A new method of design arrangement is used in the SM-1 and SM-2. Any aggregate module is made either in the form of an autonomous unit, structurally complete, with autonomous power and a built-in ventilation system, or in the form of incomplete construction (unit of elements realized on a printed circuit board, or a plug-in unit in part), installed in an autonomous unit (another aggregate module), where

space, power and ventilation have been provided for it. Thanks to the use of medium-scale integrated microcircuits, the overall dimensions of the complexes have been substantially reduced. Characteristics of the SM-1 and SM-2 are:

high throughput;

high operational characteristics (advanced capabilities for monitoring and diagnostics, automation of system restart when malfunctions occur, automation of initial program loading and system startup); and

problem orientation of architecture (capability of expanding the system of instructions as standard sets of supplementary instructions as well as special user instructions).

Local and territorially distributed multimachine complexes may be built with the SM-1 and SM-2. Information in distributed complexes, as well as between complexes and terminals is sent over telephone, telegraph and special communication lines. Interface is supported with the YeS EVM [unified system of computers], the KAMAK [expansion unknown] system, the domestic modular systems ASET [modular system of electrical measuring equipment], ASKR [automated monitoring and regulating system], ASPI [automated system for initial processing of information], and with instruments that have an outlet for the international interface for the IIS-2 measuring instruments.

The SM-1 and SM-2 models differ in systems capabilities, and capabilities of problem orientation and ensuring systems viability in concrete ASU's. The SM-1 is a traditional minicomputer meeting the requirements of relatively simple control systems and allowing development of multimachine configurations, while the SM-2 has structural and architectural capabilities allowing development of multiprocessor configurations of control computer complexes with a common storage area up to 256K bytes and common peripherals. This allows development of full standby powerful control systems of practically any complexity, with mean time between complete failures in the range of several tens of thousands of hours, i.e., within the bounds of the industrial operating time of equipment.

It is natural that these capabilities may be realized only by using the specially developed system software. The extensive system capabilities are supplemented by the capabilities of problem-directed expansion of the instruction set in the processing device and the capabilities of using programs of computers with similar architecture if such a need arises

Maintaining the input-output interface during development of the line of the modular system of microelectronic computer equipment and the system of small computers makes it possible to update and improve peripheral equipment parameters by evolution without violating the principles and methods of complexing throughout the entire life of the system. The specific configurations of the control computer systems are made up of peripherals from a set of over a hundred devices which can be grouped basically as follows.

1. External storage and input-output devices handling standard media: devices for external storage on magnetic tape or on fixed or removable magnetic disks meeting ISO [International Organization for Standardization] standards.

Input-output devices, traditional equipment for handling perforated papertape, as well as equipment for operating with magnetic media (minicassettes and floppy disks).

2. Facilities for "operator-system" communication--video terminals. There are two types of alphanumeric black and white displays (with 512 and 2,000 characters), equipped with the necessary editing facilities, and a graphic display with control that allows portrayal of a graphic panel by computer program. The capability is provided of configuring the workplace for the process engineer-operator in accordance with the functional requirements for the engineering workplace and with regard to system topography.

3. Facilities for communication with the object--a set of aggregate modules (analog-digital and digital-analog converters, commutators, normalizers, portable commutators and group converters, modules for code control and acquisition of code information) that acquire and output data in objects equipped with sensors, systems of local automation and actuators of the state system of instruments (GSP).

The structure and design of the SM-1 and SM-2 system are such that to fit each specific case, both a centralized and a distributed, by object of control, information network of a control computer complex may be configured. In the process, each individual station for acquisition and reception of information is made up from an arbitrary set of devices for communication with the object in accordance with the requirements for types of signals and the precision and rate of their acquisition and transmission. A program system has been developed that makes it possible to control the acquisition and initial processing of information of a control computer complex at the logic level.

4. Facilities for intra- and extrasystem communication (modules for interprocessor communication, modules for rapid transmission of data through special communication lines, modules for matching the internal input-output interface with the standard junction for data transmission equipment and others) that allow development of territorially distributed ASU's for various purposes both within the bounds of an enterprise and within the bounds of a large region. The capability of operating the SM-1 and SM-2 with complexes of the state system of instruments is supported.

The SM-1 and SM-2 complexes have well-developed software. The basic software delivered with the SM-1 and SM-2 complexes is designed to the needed configuration of hardware and required modes of operation from program modules of the modular software system (ASPO). The ASPO includes: a package of program modules for assembly of operating systems; problem-oriented packages of program modules; libraries of programs; a system for preparing programs; service and checking-diagnostic programs.

Software is delivered according to user specification in the form of generated program systems or a set of program modules from which the user himself assembles the program system required.

The operating system performs the set of functions, specified during its generation, on controlling the execution of tasks, input-output control, management of files, communication with the system operator, as well as on changing the complex configuration during abnormal situations (equipment failures) and on eliminating them.

In a single-task operating system, all operating programs are designed to one task and executed in the prescribed sequence, without interrupting each other. In the process, the time for execution of a task and one or more input-output operations coincides.

In a multitask single-processor operating system, operating programs are designed for several tasks. The processor at each moment of time executes the task highest in priority among those ready for execution. The remaining tasks in the ready status receive control when higher priority tasks are in the status of waiting for some event (end of an input-output operation, expiration of a time interval, change in status of a module that inputs initiative signals and others). With the onset of this event, execution of the lower priority task is interrupted. The maximal amount of storage occupiable by one task is 32K words. Tasks may be combined into groups (partitions), wherein the total storage occupiable by the system and all partitions must not exceed 128K words.

A multitask dual-processor operating system differs from the multitask single-processor system in that two tasks senior in priority may be executed simultaneously in the two processors. Tasks, just as the operating system, are stored in the common main memory for the complex in a single copy and are in no way tied in advance to the processors. If a task in one of the processors goes into the status of waiting for some external event, the processor is switched to execution of a less important task. If there are no tasks ready for execution for it, it goes into a status of a dynamic halt. Upon the opposite change in status of some task (transition from status of waiting to the status of ready for execution), the task is executed by a processor in the dynamic halt status or one executing a lower priority task. A switch to a new task does not occur if both processors are executing more important tasks when the new task goes into the ready status.

In the SM-1 and SM-2 complexes, there is a capability of specifying, during system generation, another mode for distributing tasks between the processors, wherein besides task priorities, location of tasks in main memory modules is considered. In this mode, two senior tasks located in different main memory modules are executed at any given time. Thanks to this, higher system throughput on the whole is achieved since delays associated with the simultaneous reference of the two processors to the same memory module are eliminated.

In the non-disk versions of the operating systems, all programs for the operating system an all operating programs are permanently located in the main memory for the complex. In disk operating systems, both system and operating programs are divided into two types: resident which are always in main memory during system operation, and disk-resident, which are stored on disk and called into main memory only when needed for execution. This allows saving system main memory at the cost of additional delay for calls of a disk-resident program (average time for loading and starting a disk-resident task is 100 ms, while the average time for switching of main-memory-resident tasks is about 1 ms) and impossibility of simultaneous execution of two programs set for the same area of memory. Therefore, programs that are rarely executed and insensitive to delays should be allocated to the disk-resident class.

In disk operating systems, a logical method of access to files on disks and other data media is provided. The file management system performs automatic distribution

of disk storage, and stores, saves, fetches and modifies files. Operating systems also offer capabilities associated with time readings (obtaining by program the value of the current time, waiting for a given time or expiration of a specified interval) and with control of system operation. The required instruction set for the system operator (associated with start, halt and change in task priority, logical connection and disconnection of peripherals and changing their logical numbers, obtaining data on system operation, etc.) is defined by the user and taken into account when the operating system is generated.

Execution of non-real-time tasks (such as translation, editing, debugging and assembling of user programs, execution of various calculations) may be done in the interactive or batched mode. Any of thse modes may exist in the system autonomously or as background for real-time tasks. Interactive processing may be performed in the background of batched. Each user operating in the interactive mode calls for execution the programs needed into a main memory section (partition), allocated to him, using operator instructions put into the system from a console (printer with keyboard, alphanumeric display). All system messages pertaining to operation of his programs are put out on the same device. There may be several operator consoles in the system which several users may operate independently of each other.

In the batched processing mode, periods of waiting for new instructions on system operation are reduced to the minimum. In this mode, user instructions on system operation together with the data and programs, if necessary, are prepared beforehand on perforated media and processed by a special system programm--the batched processing dispatcher. When necessary, batched processing of several input streams of tasks may be done simultaneously in the system in several partitions. As a function of operating mode, functions performed and peripheral set, the operating system takes up from 2 to 12K words or more of main memory.

For application of the SM-1 and SM-2 control computer complexes in systems that control industrial processes, within the modular software system there is a package of application programs allowing configuration of a system to acquire, analyze and process industrial data. The set of macrodefinitions in the package allows the ASU developer to describe sources and receivers of analog and discrete data and to specify processing for each point or group of points in a language understandable to him. For analog sensors, one can specify calculation of real values, linearization, smoothing, introduction of corrections for temperature and pressure, required monitoring of parameters of the industrial process, etc. A message on disturbances in the industrial process is put out to the process engineer-operator and the higher level of the control system.

The package of program modules for operation with data bases (PPM BD) is used to develop and operate large interrelated files of information on direct-access external storage devices. The package may serve as a good base for developing various queuing systems, information retrieval systems and others.

The package of programs for generation of interactive, multitask, real-time systems (DMSRV) is used to make use of the SM-1 and SM-2 complexes in systems that control a scientific experiemnt as well as in experimental systems that control industrial processes. This package supports in the interpretation mode execution of real-time tasks prepared in the interactive mode in the BASIC-RV [real-time] language which is an expanded version of the BASIC language.

The package of program modules for assembly of distributed operating systems for multimachine complexes (PPM OSMK) is a set of adjustable program modules used to develop operating systems for each SM-1 and SM-2 computer forming a local or territorially distributed multimachine complex. The distributed operating system provides for functioning of user programs written with orientation to single-machine operating systems and offers these additional capabilities:

data exchange between tasks being executed in the various computers in the multimachine complex;

execution of input-output operations with remote (parts of another computer) peripherals;

data exchange with files on direct access devices of another computer;

control of a multimachine complex using operator instructions entered from one or more central operator consoles; and

centralized loading and startup of a multimachine complex.

To reduce labor input for programming of tasks in the main areas of application of the SM-1 and SM-2 control computer complexes, the following are supplied to users:

a basic library of subroutines, including programs for calaculation of elementary functions, input-output subroutines, service subroutines for translators, interface subroutines for operating in FORTRAN in accordance with the standard and others;

a library of programs for real-time operation, including input-output subroutines and subroutines for processing analog and discrete process data;

a library of subroutines for graphic display, including administrative programs, programs to generate the basic graphic elements, programs for scaling and display of graphs, programs for interaction with man and others;

a library of subroutines for plotting to draw the basic geometric figures, legends and graphs in various coordinate systems;

a library of programs for numerical analysis containing programs for solving systems of differential equations, matrix computations, etc.;

a library of programs for processing statistical data; and

a library of programs to sort and merge data files.

The following programming languages are available to the user: mnemonic code, macro language, FORTRAN II, FORTRAN IV, and a dialect of ALGOL-60. BASIC may be used to solve problems in the interactive mode. Besides translators and interpretors, the service programs include: a symbolic data editor, assembler, debugger, programs to copy from one medium to another and others.

In addition to the systems described above, users of the SM-1 and SM-2 control computer complexes are supplied (upon request) M-6000 operating systems adapted for single-processor configurations of the SM-1 and SM-2 complexes with a main memory capacity of no more than 32K words. These systems include:

a basic control system (OUS) that supports the single-task mode of operation;

a real-time supervisor (SRV) that operates with the basic control system and allows execution of up to 28 real-time tasks without one task interrupting another;

a modified real-time supervisor (SRV-M) that operates with the basic control system and allows execution of up to 98 real-time tasks belonging to two groups (tasks in the first group interrupt those in the second);

a disk operating system (DOS) that supports preparation, debugging and execution of user programs both in the batched and interactive modes;

a real-time disk operating system (DOS RV) that supports simultaneous operation of a computer complex in the real-time multitask mode and in the modes of interactive and batched processing;

a file management system (SUF) that functions within the real-time DOS and offers the user additional capabilities for efficient processing with data organized in the form of files on disk and other standard input-output devices; and

the BASIC interpreting system designed to solve mathematical and engineering problems in the interactive high-level BASIC language.

Thus, the SM-1 and SM-2 constitute a system of hardware, well-developed in structure and architecture, as well as in nomenclature of peripherals, open to development, and designed especially for building industrial process control systems and other ASU's with similar functions. The experience of development, introduction into series production and assimilation by users of the first lots of the SM-1 and SM-2 has confirmed the correctness of the initial premises and fruitfulness of this direction. In throughput, the SM-1 and SM-2 complexes outperform by twofold on the average the M-6000 and M-7000 complexes previously developed and distributed within the CEMA countries for similar purposes. The method of delivering complexes specified according to individual order, that had been introduced for the M-6000, continues in practice based on the SM-1 and SM-2.

The primary aims and directions of further development of the architectural line of the SM-1 (SM-2) have been defined:

further improvement of the effective throughput of the processors, throughput of the channels, and the capacity of the main memory, both the total in the complex as well as the memory accessible to a task;

introduction into the nomenclature of specialized processors supporting high throughput when solving special problems;

expansion of the set of signals received from and sent to the object, and improvement in the rate and metrological characteristics of the USO [device for communication with the object];

expansion of the forms and methods for intercourse between the computer and operating personnel, and improvement in human engineering characteristics;

development of means and methods for improving reliability;

development of capabilities for configuration of territorially distributed complexes and networks of computers;

development of means of communication with the unified system of computers, KAMAK, etc.

An effective means of achieving the goals set is to use microprocessors and microprogrammable controllers for building intelligent terminals, decentralizing data processing, organizing data transmission, controlling the operation of a computer complex, etc. Within the framework of the program of efforts on the small system of computers, these goals will be realized in the SM-53/50 multiprocessor complexes which continue the architectural line of the SM-1 and SM-2.

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TERMINAL INTERFACE MACHINE BASED ON THE SM-3 COMPUTER

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 38-42

[Article by E. T. Beyner, engineer, USSR; P. P. Treys, engineer, USSR; and E. A. Yakubaytis, academician of the Latvian SSR Academy of Sciences, USSR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The emergence of electronic computer networks (EVS) has not only opened broad prospects for new methods of data processing, but has also raised a number of problems for researchers. One of them is the necessity of using in the networks the subscriber stations (AP) that were developed previously for tree-like systems of teleprocessing with a central computer. The main obstacle to direct connection of existing subscriber stations (terminals) to a computer network with switching of packets is the incompatibility of the data exchange protocols by which the network and subscriber stations operate. To eliminate this obstacle, a terminal interface machine (TIM) is installed between the network and the station (fig. 1); the TIM links the entire hierarchy of protocols used [1]. In addition to this, user capabilities have to be expanded, for example, to support operation with system programs of the unified system of computers of the type KAMA, DUVZ and KROS [expansions unknown]. Thus, the terminal interface machine is designed to connect terminals and subscriber stations operating by synschronous and asynchronous methods of character-by-character or block-by-block data transmission to central machines through a packet switching network.

The terminal interface machine was developed on the base of a standard configuration of the SM-3 computer, supplemented by a set of remote data transmission equipment. Operation through the TIM allows subscribers to:

conduct the initial dialog with the TIM for presentation of the addressee with whom the subscriber will be exchanging data during the communication session;

operate in the mode of remote input-output of tasks;

operate in the interactive mode with system application programs of the unified system of computers; and

conduct the concluding dialog with the TIM.

The following features are considered in developing the TIM:

in the experimental network to which the TIM is connected, data exchange proceeds through previously allocated logical channels; therefore, the TIM does not have to solve the problems associated with setting and releasing logical channels (see fig. 1);

it is assumed that the number of logical channels allocated (third level of X25) matches the number of processes at the application level in the TIM which makes multiplexing at the higher levels unnecessary. However, the TIM software is designed for future evolution through replacement of individual modules, for example, for realization of the full set of functions of the third level of the X25 protocol.* The capability of replacing the LAPB [expansion unknown] driver by a program that supports a microprocessor controller that realizes the LAPB protocol by hardware has been taken into account.

The logical structure of the TIM is shown in fig. 2. The logical structure is designed to use subscriber stations operating by synchronous and asynchronous (start-stop) data transmission methods. Used for this are two types of linear adapters, the SLA [synchronous linear adapter] and the ADS [asynchronous adapter for remote communication], connected to the common bus [OSh] of the SM-3. The sets of program modules of virtual terminals, operating with various types of subscriber stations, contain various modules to support these adapters as well as various program interfaces for the subscriber stations. The interfaces between the virtual terminals, the VTA [virtual terminal, asynchronous], the VTS [virtual terminal, synchronous], and the units PP1, PP2, ..., are identical. The interfaces between the units for communication with the application processes and the transport stations, as well as between the stations and the X25 terminators have also been standardized. The units PP1, PP2, PP3, ... are problem-oriented, i.e., designed to operate with specific system programs of the unified system of computers (for example, KROS, DUVZ, KAMA). The number and set of these units depend on user requirements and the number of subscriber stations.

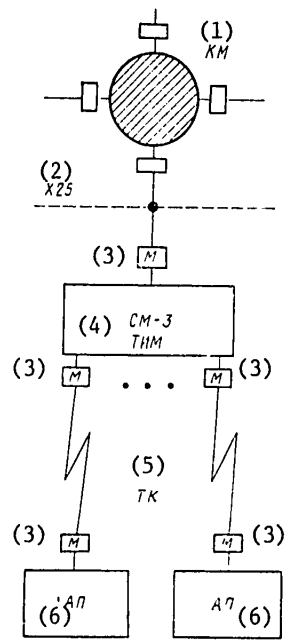

Fig. 1. Structure of Subscriber Station Interaction with an Electronic Computer Network

Key:
1. KM--communication machine
2. X25--network interface
3. M--modem
4. SM-3 TIM
5. TK--telephone channels
6. AP--subscriber stations

* The X25 is the protocol (algorithm for data transmission and exchange) recommended by the International Telephone and Telegraph Consultative Committee (MKKTT). It has a multilevel structure.--Editor's note.

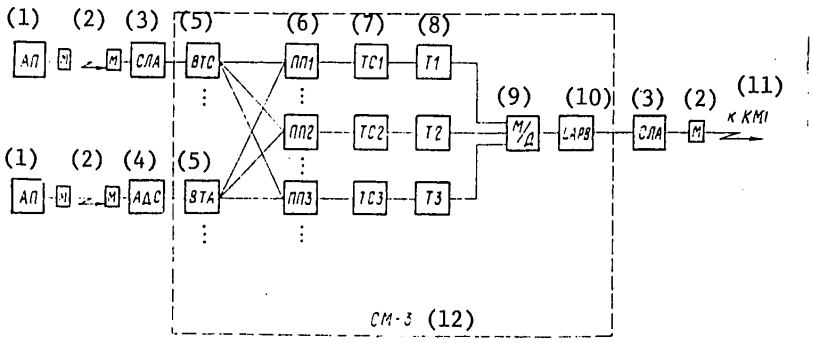

Fig. 2. Logical Structure of the Terminal Interface Machine (TIM)

Key:

1. AP -- subscriber station
2. M -- modem
3. SLA - synchronous linear adapter
4. ADS - asynchronous adapter for remote communication
5. VTS, VTA - complexes of program units of virtual terminals for operation with synchronous and asynchronous adapters, respectively
6. PP1, PP2, PP3 - program units for communication with application processes in the unified system of computers
7. TS1, TS2, TS3 - transport stations
8. T1, T2, T3 - X25 terminators
9. M/D - multiplexor-demultiplexor
10. LAPB - driver that realizes the LAPB channel protocol
11. to the communication machine
12. SM-3

Let us examine the functions of the individual functional units of the TIM. The VTS and VTA virtual terminal program unit complexes contain programs to support the linear adapters and to supply the protocols for synchronous or asynchronous data transmission. These units respond to the calls from the subscriber stations and set up the links. After linkage, the virtual terminal supports the initial dialog with the subscriber stations in which the called process and parameters for linkage are defined. When the resource is available (unit for communication with the application process), the virtual terminal is linked to the application process. When no resource is available, a message is sent to the subscriber station and the link is terminated. If a link with a process is established, the virtual terminal goes into the text mode and begins operation. In the process, the subscriber station may break the text mode, conduct a concluding dialog with the virtual terminal and free the resource. If a malfunction occurs in the line between the subscriber station and the virtual terminal, link restoration is possible. If this does not occur in the prescribed time interval, the link to the process is terminated in the malfunction mode.

Each unit for communication with the application process (PP1, PP2, ...) supports interactive communication with one specific process in the central machine (unified system of computers). For the process in the central machine, the corresponding PP [application process] in the TIM is a process of the same level. The number of types of application process units equals the number of processes in the network that are accessible through the TIM. The number of units of each type is determined by the number of subscriber stations operating simultaneously with each process in the network. Each unit for communication with an application process is assigned a transport station. The unit that controls the application process is thus supplied with the necessary facilities for operation with the process in the network. On the other hand, these units serve as resources and are distributed among the virtual terminals.

Between the application process operating by messages and the X25 terminator, there is a trsnport station that receives data packets from the terminator and forms messages from them, and conversely, breaks up messages and forms packets sent to the terminator. The data received from the terminator is checked by the transport station to see if it belongs to the specific "process-process" communication and is sent to the application process or canceled.

Each logical channel registered in the TIM corresponds to one X25 terminator [2] which is always in an active status. The X25 terminator sends to and receives from the transport station data packets and packets of interrupts. The main task of the terminator is to support the X25 protocol. The terminator sends to the multiplexor-demultiplexor data and service packets and accepts correctly received packets from it. An X25 terminator may be engaged or free. The initiative for entry into linkage in the TIM belongs to the subscriber station, and data exchange through the TIM is possible only if a request for TIM services arrives from the subscriber station. All X25 terminators used by the subscriber stations are in an engaged status and transmit data in both directions. The free X25 terminators have no correspondent from the subscriber station and do not have to transmit data. The multiplexor-demultiplexor links the LAPB driver with the set of X25 terminators. It transmits correctly received packets to the terminators by logical channel number in the packet heading or cancels the packet is the logical channel number is not registered in the TIM. A reference to the multiplexor-demultiplexor occurs when each data frame is received and when transmission of each data frame to the line is completed. The multiplexor-demultiplexor puts the X25 packets received from the terminators into a queue for transmission.

The LAPB driver supports a balanced protocol in the "point-point" mode through the half-duplex communication channels. Data is transmitted in bytes. The hardware of the SLA adapter sets bits to provide "transparency," identifies flags and exceptions and calculates the check sum. Since communication between the packet switching network and the TIM must be maintained throughout operation of the TIM, the LAPB driver sets up links at the start of operation, maintains the links and restores them in event of malfunctions and disconnects the TIM upon completion of work. The LAPB driver sends to the multiplexor-demultiplexor the data fields of frames--packets received without errors and receives packets from it for transmission.

Using the SM-3 as a terminal interface machine supports the interaction of up to 16 standard character (non-packet) terminals in the unified system of computers with the information computing resources of a packet switching network. The data transmission rate through the communication lines depends on the type of modems and terminals used. The SLA and ADS adapters support operation at a rate of up to 9600 baud.

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CSO: 1863/157

MICROCOMPUTER APPLICATION IN LABORATORY GAS CHROMATOGRAPHY

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 42-49

[Article by W. Felre, engineer, GDR, and M. Kummer, engineer, GDR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] Laboratory gas chromatography is a widespread analytic method in studies in chemistry, the environment and others. However, this method requires high inputs for adjusting and supporting the needed levels of analysis and even higher inputs to output results from the given measurements. Therefore, attempts are being made to automate laboratory gas chromatography, especially processing of chromatograms. As a rule, small computers have been used for this purpose, but their high cost has limited their application. The development of substantially cheaper microcomputers has made it possible to automate these processes.

In using the gas chromatographic method, a mixture of the components of a gas or evaporated sample is separated into its component parts in a fractionating column based on physical principles. The qualitative and quantitative determination of these components is the aim of the analysis. Using a detector, the physical result is converted into an analog electrical signal which represents the gas chromatogram (fig. 1), but yields (graphically) only the approximate results of the analysis. Determining the time of emergence of maximum peaks and areas of peaks will allow deriving the qualitative and quantitative result of analysis of the components desired.

As a rule, recording of an entire gas chromatogram, requiring more than a hour, is necessary to derive analysis results. A chromatogram may be recorded graphically (on paper or magnetic tape) or in the form of digits (print out of numbers or storage in main magnetic memory). Special equipment is needed for each type of recording. If automation is performed by computer equipment, then the digital form of recording is preferred. To precisely record the dynamics of the chromatogram, a scan frequency of at least 10 Hz is required, which corresponds to the main memory capacity needed to store the results of about 40,000 measurements. Stemming from the need to economize on memory, signal processing begins even before the computer (integration), and considerable data is reduced parallel with scanning of the chromatogram in real-time. Such processing of the chromatogram makes it possible to influence subsequent analysis, using intermediate results, during current analysis. Subsequent analysis is done by microcomputers connected to each laboratory gas

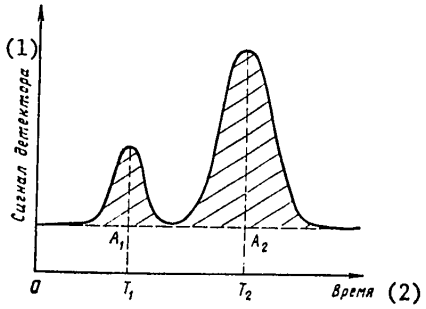
Fig. 1. Gas Chromatogram (Diagram):

A -- area of peak;

T -- time of retentions.

Key:

1. signal of detector
2. time



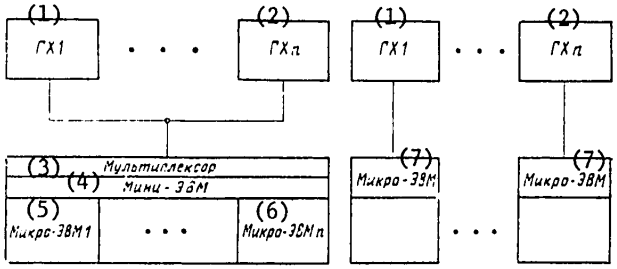


Fig. 2. Diagrams of Application of Mini- or Microcomputers for Laboratory Gas Chromatographs: GC1, ..., GCn are the laboratory gas chromatographs; microcomputer 1, ..., microcomputer n are part of the minicomputer for automation of GC1, ..., GCn

Key:

1. GC1
2. GCn
3. Multiplexor
4. Minicomputer
5. Microcomputer 1
6. Microcomputer n
7. Microcomputer

chromatograph (fig. 2). Before, each small computer used served from 4 to 20 chromatographs, which made the software for them very complicated. Program processing of a chromatogram in a microcomputer is the same as in small computers.

The programs must include operations such as identification of peaks, processing of superimposed peaks and supplementary peaks, adjustment of base lines, etc. They may be supplemented by other operations on peaks (suppression and summing of peaks, change in sensitivity of identification of peaks, etc.).

Chromatograms are always evaluated in the batched processing mode, after completion of analysis or acquisition of the chromatograms. Applying microcomputers for this case is no different from using small computers.

Using microcomputers to process chromatograms allows significant improvement in operator (user) communication with the complex. The operator receives data on the status, alignment and results of system operation. In addition, microcomputers allow reducing the number of special operations to service the gas chromatograph. The complex contains a problem-oriented keyboard for the user to align and service the complex.

The operator obtains data on system operating status by using:

a digital display for checking the numeric input and output of physical parameters (for example, temperatures of the fractionating column) measured by the microcomputers;

facilities for indication (for example, light-emitting diodes) of the status of operation and analysis; and

printers for recording operator actions and events in the process of analysis (for example, a message on errors) and recording the result (logging). In addition, a graphic analog image of the chromatograms is required.

Depending on the problem being solved, "operator-computer" dialog is conducted using the appropriate device (for example, printer) to obtain the needed information from the operator. The operator responds through the keyboard to queries as they appear and receives answers himself on the display or printout.

Using microcomputers for control significantly improves the operation of a laboratory gas chromatograph.

Thus, in the case of automating control by conventional electronics (provided the process can be measured and regulated), all signals, as a rule, are acquired and processed separately; multiple use of signals needed for processing is not possible in the majority of cases. Only the most necessary functions are automated due to high costs. Adjustment is possible within very narrow limits.

In using microcomputers, signals are acquired by central modules. The central processor allows solving laborious signal processing problems with great flexibility of the algorithms to fit specific conditions.

The most varied problems are solved by using microprocessor control, for example:

realization of general temperature conditions (monitoring and control of temperature, changing temperature conditions as a specified function of time);

automatic feed of samples (control of sequence of sample feed, automatic dosing, automatic identification of samples);

control of recorder (switch on and off, setting of markers); and

connection of individual system parts (for example, connection of the column).

It is possible to make use of microcomputer hardware in stages as the level of automation increases (fig. 3).

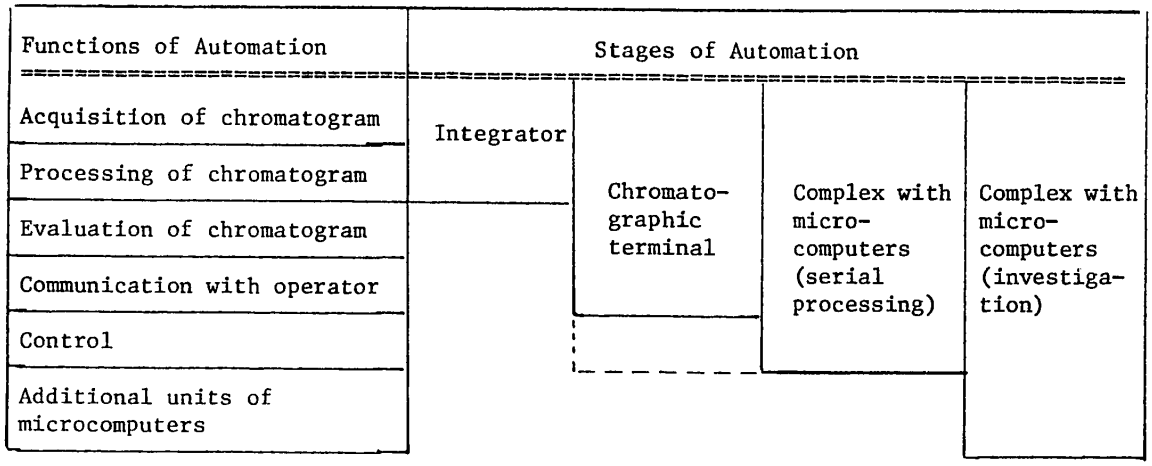


Fig. 3. Stages of Automation with Application of Microcomputers in Laboratory Gas Chromatograph

Let us consider the chromatographic terminal realized by using the SM-50/10-1 microcomputer system. This eight-bit computer for limited tasks of computations, monitoring and control is also used in monitoring and laboratory instruments and devices for an operate to communicate with a process or with a computer.

The modular structure of the SM-50/10-1 allows easy variation of the configuration, which facilitates substantially including it in complexes and systems at moderate cost. It consists of the following functional parts: central processor, semiconductor main memory, peripheral control device, indication and display control device, semipermanent memory unit (PPZU), program debugging stand, accumulator module for holding data and a timer.

The SM-50/10-1 microcomputer system configuration for a chromatograph is shown in fig. 4. Units for preventive maintenance and program debugging are not shown in the diagram.

The complex uses a real-time operating system (OSRV) that controls the central interrupt register (fig. 5). If no branch 1-4 is being processed, then the system is in a wait cycle (dynamic halt) until processing of the next interrupt. Interrupt 0 (INT0) has the highest priority, INT7--the lowest. An interrupt from the network occurs with switch-on or malfunction of the network. The timer generates interrupts with equal time intervals. Messages on malfunctions and keyboard entry occur irregularly.

The start-restart program ensures a correct start after the computer is connected to the network and a correct continuation (restart) with connection of the network after a malfunction. Restart sets the major parameters of the system and specific statuses of the input-output units and the system of programs. Then the program goes into a dynamic halt (wait cycle).

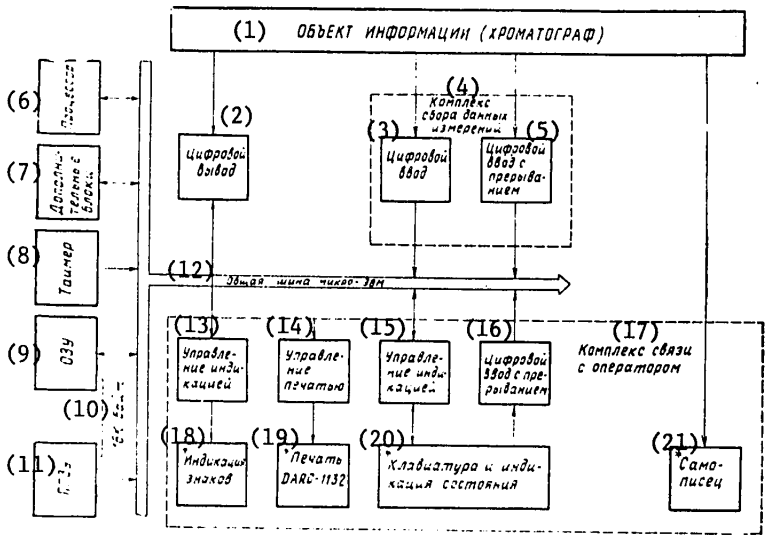


Fig. 4. SM-50/10-1 Microcomputer System Configuration for Chromatograph (components marked with an * are not part of the SM-50/10-1)

Key:

1. Object of information (chromatograph)
2. Digital output
3. Digital input
4. Complex for acquisition of measurement data
5. Digital input with interrupt
6. Processor
7. Supplementary units
8. Timer
9. Main memory
10. 16K bytes
11. Semipermanent memory unit
12. Common bus of microcomputer
13. Display control
14. Printer control
15. Display control
16. Digital input with interrupt
17. Complex for communication with operator
18. *Character display
19. *DARO-1132 printer
20. *Keyboard and status display
21. *Recorder

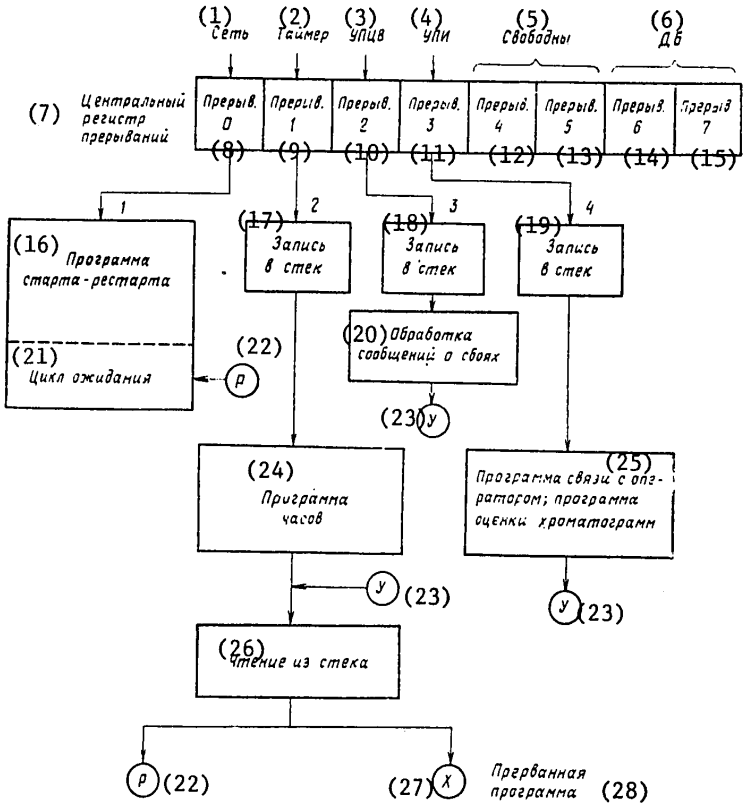


Fig. 5. Monitor Program of the Real-Time Operating System (OSRV)

Key:

1. Network
2. Timer
3. UPTsV -- Digital input control
4. UPI -- Display control
5. Open
6. DB -- Supplementary units of microcomputers
7. Central interrupt register
8. Interrupt 0
9. Interrupt 1
10. Interrupt 2
11. Interrupt 3
12. Interrupt 4
13. Interrupt 5
14. Interrupt 6
15. Interrupt 7
16. Start-restart program
17. Write in stack
18. Write in stack
19. Write in stack
20. Malfunction message processing
21. Wait cycle
22. R
23. U
24. Clock program
25. Operator communication program; chromatogram evaluation program
26. Read from stack
27. Kh
28. Interrupted program

The clock program realizes the entire real-time portion of the real-time operating system, including control of the programs for acquisition and processing of chromatograms.

The operator communication program processes signals from the keys.

The real-time operating system was developed in the following stages:

assembly of the complete microcomputer documentation, including detailed description of instructions to familiarize developers with the machine (documentation on operating the SM-50/10-1);

description of tasks taking microcomputer capabilities into account and optimal division of tasks between hardware and software (close cooperation between client and developer is advisable);

determination of microcomputer system configuration for development of the real-time operating system taking cost of final version into account, which requires optimal utilization of the common bus; and

preparation of needed devices and software: microcomputer, computer for program development, computer software, debugging programs for microcomputer components such as the processor, main memory and input-output control. Precise debugging instructions (documentation) are also necessary.

The real-time operating system structure was developed in the following stages:

development of basic flowcharts for the total system;

estimate of relative duration of operation of individual branches of the program;

selection of critical branches for operation in real-time;

determination of priorities for operation of program branches (leads to monitor program); and

determination of points at which interrupt of individual program branches is possible.

It is advisable to have one person (the lead programmer) perform the procedures of these stages provided he has previous experience as a developer of program systems.

After distribution of tasks by developers, depending on individual capabilities and skills, the detailed flowchart can be worked out or the instruction sequence written immediately. The written instruction sequence is punched on peforated tape, translated using the Assembler (in the process, a listing is produced in addition to the perforated tape in machine code) and debugged. When there are syntactic and (or) logic errors, the process is repeated until the program is error-free.

Development of the real-time operating system should begin with the program branch used most often, for example, with the operator communication program which realizes the digital display, input of parameters, etc., and offers diverse capabilities for debugging. Experience shows that the following sequence is advisable in developing the real-time operating system.

Program to be developed	Computer for debugging
Peripheral programs: data acquisition program, data output program, digital display program	Microcomputer
Service subroutines: clearing program (clearing regions of main memory), loading programs	Microcomputer or main computer
Arithmetic subroutines: basic arithmetic operations, comparison operations for various wordlengths	Main computer
Development of parts of a branchprogram using subroutines	Main computer or microcomputer
Writing of a program branch under real conditions of interrupts (including storage in stack)	Microcomputer
Gradual addition of remaining branches of the program to the total system	Microcomputer
Recording the real-time operating system into the semipermanent memory unit with verification	Microcomputer

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ORGANIZATION OF MULTIPROCESSOR OPERATION BASED ON SM-50/40-1 MICROCOMPUTER MODULES

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 49-53

[Article by V. D. Gus'kov, engineer, USSR; N. D. Kabanov, engineer, USSR; V. S. Kravchenko, candidate of engineering science, USSR; and A. N. Shkamarda, engineer, USSR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The model SM-50/40-1 is an eight-bit modular microcomputer made with n-channel MOP-BIS [metal oxide semiconductor large-scale integrated circuits]; it is designed to be used as a controller for active devices for communication with an object (USO), terminals and data transmission equipment to build distributed systems that control industrial processes, automated systems for laboratory and production measurements, and automation of scientific experiments and the processes of data preparation, programming and training.

The SM-50/40-1 consists of functionally complete modules made in the form of individual boards and leading to a unified parallel interface (I41). SM-50/40-1 modules may be divided into these groups: processor modules, memory modules, peripheral communication modules, object communication modules, intermachine exchange modules and auxiliary modules.

The I41 unified parallel interface establishes common principles for data exchange between the SM-50/40-1 microcomputer modules. The structure of the I41 interface supports addressing of the memory units using the entire address field of the interface (64K bytes); in the process, addressing the registers of the input-output [IO] devices (UVV) is also supported--256 addresses for input and 256 addresses for output of data. Data may be sent in the direct-access mode from one IO device to the others, from an IO device to memory or from memory to an IO device, bypassing the processor. IO devices may issue requests to interrupt the processor program, which are serviced in accordance with the system of priorities for the IO devices. The majority of lines of the I41 interface trunk are used for two-way transmission of signals. All modules, including the microprocessor, are connected to these lines in parallel. The procedure for interaction between devices and the I41 interface is such that in any exchange operation, there are always two devices associated between themselves as a controller (control device) and an executor (controlled device). The controller controls the operation of the interface during data exchange with the executor. Only one controller may operate at a time in the

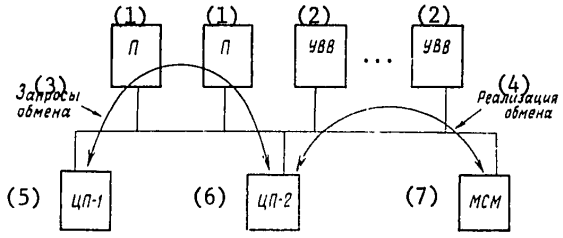
interface. There are four types of operations for transmitting data through the I41 interface--read from memory, read from an IO device, write to memory and write to an IO device.

From certain methods of organizing parallel operation in the SM-50/40-1, multimachine complexes and multimicroprocessor systems are realized.

Multimachine complexes are several computers joined by intermachine exchange modules. From the viewpoint of data exchange, multimachine complexes are poorly linked systems due to the limited transmission rate and rather lengthy delay in transmitting data packets. Intermachine exchange may be realized by using an interface module with a modem, a communications device with "Common Bus" interface (links an SM-50/40-1 to an SM-3 or SM-4) and a communications device with an I41 interface (links two SM-50/40-1's).

In organizing an Intermachine exchange using an interface with a modem, the basic difficulty lies in realizing the standard exchange protocols (HDLC [expansion unknown], SDLC [synchronous data link control] and others) and preliminary processing of packets. The SM-50/40-1 hardware does not support these functions; therefore, they are realized by software. In single-processor configurations, a substantial amount of time is spent on these routine functions. The capability of parallel operation of several processors with the I41 trunk allows data exchange operations to be performed in the second central processor (fig. 1).

Fig. 1. Dual-processor System Using SM-50/40-1 Modules for Data Exchange Operations



Key:
1. P -- memory
2. UVV -- IO device
3. exchange requests
4. exchange realization
5. TsP-1 -- main processor
6. TsP-2 -- auxiliary processor
7. MSM -- interface module with modem

Systems with better linkage are multimachine complexes using communication devices with a "Common Bus" or the I41 for exchange. These devices support read-write operations for files of data with a length of up to 256 two-byte words through direct memory access; simultaneous execution of operations actuated in different directions is also possible. The software for these multimachine complexes must include procedures that realize sending of data packets, obtaining confirmations, and facilities for synchronization of user problems executed in the different computers. For multimachine complexes, realization of a unified operating system is also possible, which enhances the viability of the entire system as a whole.

Multimicroprocessor systems differ from multimachine complexes primarily by the availability of common memory and IO devices. SM-50/40-1 central processors also have their own memory and access to it does not require the processors to "seize" the entire I41 trunk. The size of this memory determines the overall throughput of a multimicroprocessor system.

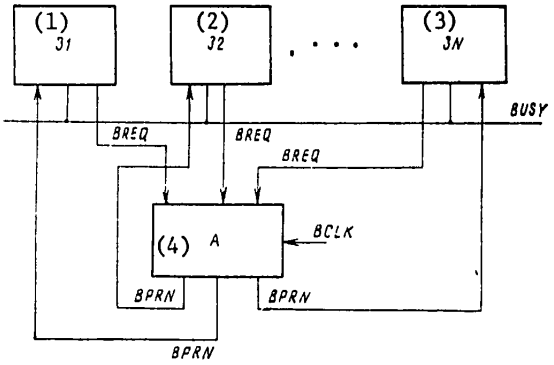


Fig. 2. Flowchart of Parallel Arbitration

Key:
1. Z1 -- controller 1
2. Z2 -- controller 2
3. ZN -- controller N
4. A -- arbitrator

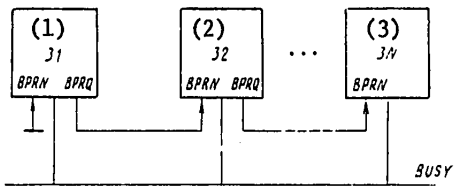


Fig. 3. Flowchart of Serial Arbitration

Key:
1. Z1 -- controller 1
2. Z2 -- controller 2
3. ZN -- controller N

For multimicroprocessor systems, the method used by the processors to "seize" the I41 trunk for access to the common memory and IO devices. As a function of the priority organization, three methods of "seizure" are possible: parallel, serial and cyclic.

In the parallel method, each controller in the system has its own line for the BREQ signal to request the trunk, which is emitted by the controller through a negative front of the synchronization line BCLK and goes to the arbitrator (fig. 2). The arbitrator analyzes the requests and for each of the negative fronts of the BCLK emits a BPRN permission signal to the controller having the higher priority; each controller has its own line for the permission signal. The controller that received the BPRN signal when there is no bus BUSY signal, by a negative front of the BCLK puts out a BUSY signal and removes the BREQ. The bus remains busy until the controller completes the reference and removes the BUSY signal by a negative front of the BCLK.

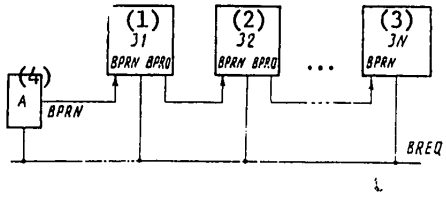


Fig. 4. Flowchart of Cyclic Arbitration

Key:
1. Z1 -- controller 1
2. Z2 -- controller 2
3. ZN -- controller N
4. A -- arbitrator

In the serial method (fig. 3), the BPRN signal indicates to a controller that there is no higher priority bus request in the system. A BPRQ signal is emitted by a controller that received a BPRN signal, but is not requesting the bus, and is sent to the BPRN inlet of the next controller having a lower priority. The BUSY signal, also controlled by the controller, is used for analysis of the bus busy status.

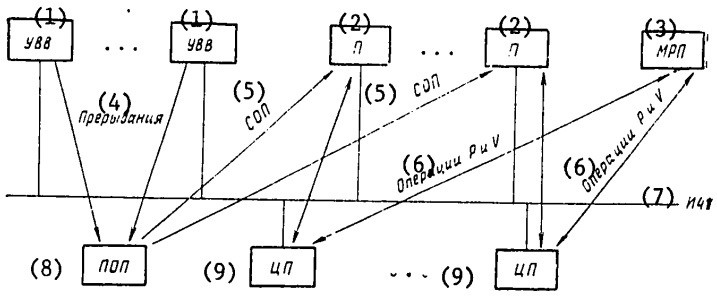


Fig. 5. Structure of a Real-Time Multimicroprocessor System

Key:

1. UVV -- IO devices
2. P -- memory
3. MRP -- module for realization of primitives P and V
4. interrupt
5. SOP -- messages to echangers of interrupts
6. operations P and V
7. I41
8. POP -- interrupt processing processor
9. TsP -- central processor

The cyclic method (fig. 4) is characterized by emission of requests by a chain of controllers to one BREQ line. The arbitrator, receiving the BREQ signal, emits a BPRN signal to the chain. One of the controllers that has the highest priority of those that issued a request receives the BPRN signal, interrupts its further passage and begins the reference through the bus. If at this time a bus request emerges from a controller having a higher priority and the BPRN signal has already gone through, then it does not put out a BREQ signal.

After completion of the references, control passes to the controller that issued a request with a lower priority. After completion of the reference, the controller removes the BREQ signal from the line. When there are no requests on this line, all the controllers simultaneously remove the BPRQ signal from their outlets, and the arbitrator removes the BPRN signal.

The structure of a real-time system supporting multimicroprocessor operation is shown in fig. 5.

User tasks and procedures for the nucleus of the operating system are reenterable and may be executed in the various central processors. Blocking of the nucleus data structures, including lists of tasks and lists of regions of data exchange (exchangers), is maintained by using a special module that realizes the primitives* P and V. In parallel organization of the I41 interface, interrupt buses may

* A primitive is an elementary operation. A V operation increases the argument A (integral) by 1. A P operation decreases A by 1 (in the region A 0). They are used to synchronize operations in computer systems (for more details, see for example: "Yazyki programmirovaniya" [Programming Languages], edited by Or. Zhenyui, Moscow, Mir, 1972).--Editor's Note.

initiate several processors simultaneously; therefore, (to improve time characteristics) it is advisable that an individual processor--the interrupt processing processor--be charged with responding to the interrupt, which consists in sending a special message to the exchanger of interrupts.

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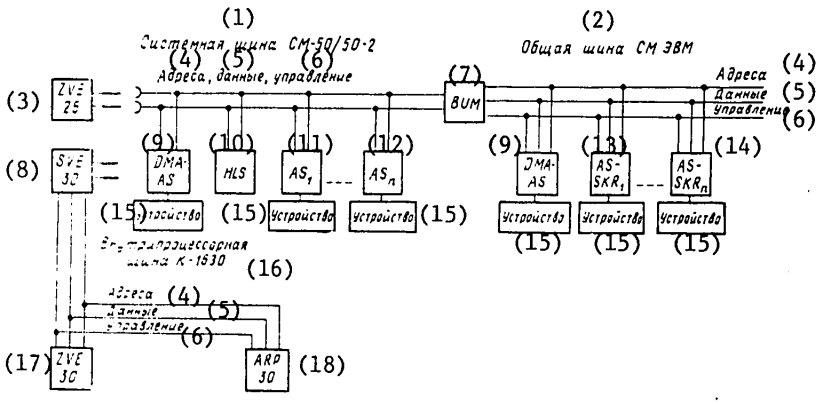
SM-50/20-2 MICROCOMPUTER

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 54-62

[Article by H. Giebler, engineer, GDR, and M. Lauermann, engineer, GDR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text]



SM-50/50-2 System Architecture

[latin characters, except DMA, are German abbreviations]

Key:

1. SM-50/50-2 system bus
2. SM EVM [system of small computers] common bus
3. ZVE 25 -- processor
4. addresses
5. data
6. control
7. BUM -- interface converter for buses
8. SVE 30 -- memory control unit
9. DMA-AS -- direct memory access controller
10. HLS -- semiconductor memory
11. AS_1 -- controllers on SM-50/50-2
12. AS_n system bus
13. $AS\text{-}SKR_1$ -- controllers on SM EVM
14. $AS\text{-}SKR_n$ common bus
15. device
16. internal processor bus K-1630
17. ZVE 30 -- processor
18. ARP 30 -- arithmetic processor

In developing the SM-50/50-2, it was necessary to ensure compatibility with the SM EVM [system of small computers] and increase the scale of integration of the element base. To solve this problem, a completely new approach was adopted: parallel development of the computer itself and the system-defining microcircuits in a continual process of optimization. The aim was to develop highly integrated circuits defining the main system properties of the SM-50/50-2 and sufficiently general-purpose to use them in other electronic devices or computers. It was decided to use metal oxide semiconductor [MOS] technology which is more effective for creating large-scale integrated [LSI] circuits with the throughput needed. As a result, a modular system was developed that consists of concrete configurations of the K-1620 and K-1630 computers and is designated the SM-50/50-2 in the system of small computers.

The general system architecture of the SM-50/50-2 microcomputer provides for having all system components, such as the central processor, memory modules, controllers and matching modules, connected by a common trunk--the SM-50/50-2 system bus (see the drawing). In the SM-50/50-2, there are three systems of buses, coordinated with each other and guaranteeing flexibility and configuration properties of the SM-50/50-2 system: the K-1630 internal processor bus, the SM-50/50-2 system bus and the SM EVM common bus.

Through the K-1630 internal processor bus, it is possible to also equip the K-1630 microcomputer with an arithmetic processor for fast processing of numbers with floating and fixed points. Communication through the SM-50/50-2 system bus is the same for all devices connected and is effected by the "master-slave" principle in both the programmed mode of the processor and the mode of direct memory access.

The SM-50/50-2 system bus operates asynchronously relative to the length of the lines and data transmission, but synchronously for addressing. The organization of addressing, direct memory access and interrupts has not been changed fundamentally so that when both trunks are available, communication with all system parts is possible at the level of full program compatibility. The bus allows parallel word-by-word transmission of data and addresses (16 bits) through the same bidirectional lines and thereby permits connecting memory modules up to the maximum size of the memory of 128K words. The region of the upper 4K words of the total capacity for addressing has been allotted for addresses of input-output [IO] devices. Two more functional units belong to the system bus: an expander and a cap.

The system bus has been designed in the form of a two-layer printed circuit board.

The SM EVM common bus corresponds precisely to the methodological material MM SM EVM 003-76. Connection of peripherals and controllers to the interface for the SM EVM common bus is supported by the bus converter (BUM). The K-1620 and K-1630 microcomputers are serviced by using a communications device installed separately from the processor and linked to it through a controller. The peripherals connectable to the SM-50/50-2 system (table 1) have a number of features: functional and design completeness, capability of connection to the SM EVM common bus and autonomous design (movable unit or individual device).

Devices 1-15 (see table 1) operate in the programmed mode. For compatible operation with the 25 and 30 central processors, the controllers have buffer data registers for input-output of data as well as status registers to indicate the current

Table 1. Peripherals for the Model SM-50/50-2

No.	Device type	Model designation by developer-country, SM EVM model	Basic technical data	Device interface	Controller type	Processor interface
1	card reader	VT 42111 (HU), SM-6101	600 cards/min, desk unit	IRPR	ASP	SM-50/50-2 system bus
2	card reader	K-6100 (GDR)	160 cards/min, desk unit	"	"	"
3	perforated tape IO unit	K-6200 (GDR)	200 char/sec input; 50 char/sec output; slide-in unit	"	"	"
4	perforated tape input unit	Robotron 1210 (GDR)	200 char/sec, desk unit	SIF 1000	ASI	"
5	tape perforator	Robotron 1215 (GDR)	50 char/sec, desk unit	"	"	"
6	perforated tape IO unit	SPTP-3 (PO), SM-6204	1000 char/sec input; 50 char/sec output; slide-in unit	IRPR	ASP	"
7	perforated tape input unit	FS1503 (CSSR)	1500 char/sec, desk unit	IRPR	ASP	"
8	magnetic tape cassette IO unit	K-5261 (GDR)	two magnetic tape transports, slide-in unit	IRPS	ASD	"
9	alphameric serial printer	Robotron 1152 (GDR)	30 char/sec, 132 char/line, desk unit, external unit	"	"	"
10	alphameric serial printer	Robotron 1157 (GDR)	200-400 char/sec with 132 char/line, desk unit, external unit	"	"	"
11	alphameric parallel printer	VT 27060 (HU)	600 lines/min with 64 char/line, external unit	IRPR	ASP	"
12	operator console	K-7160 (GDR)	screen with 31 cm-diagonal, 24 lines with 80 char., alphameric keyboard, desk unit	IRPS	ASD	"
13	teletype	FSM T51, T63 (GDR)	50 bits/sec, desk unit	S1	ASD	"

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14	IO unit	K-7260 (GDR)	screen with 31 cm-diameter, 24 lines with 80 char., alphameric keyboard, desk unit	S2	ASD		SM-50/50-2 system bus
15	process communication unit	Ursadat 5010 (GDR)	set of assemblies to configure an automated industrial process control system; analog IO, digital IO, pulse input, incremental output; in a rack	ISO	ATP		"
16	magnetic tape storage unit	IZOT 5004 (BU), SM-5300	10 kbytes/sec; 32 bits/mm; slide-in unit	INML	AMB		SM EVM common bus
17	magnetic tape storage unit	IZOT 5006 (BU), SM-5303	36 kbytes/sec; 32 bits/mm; slide-in unit	INML	AMB	SM-5001	SM EVM common bus
18	magnetic disk cartridge storage unit	IZOT 1370 (BU), SM-5400	one permanent disk, one cartridge disk, 25 Mbits each, 2.5 MHz, 60 ms, slide-in unit	IKMD	AKP		SM-50/50-2 system bus
19	magnetic disk cartridge storage unit	MEPA 9125 (PO), SM-5401	one permanent disk, one cartridge disk, 25 Mbits each, 2.5 MHz, 60 ms, slide-in unit external unit	IKMD	AKP		"
20	floppy disk storage unit	BHP (GDR)	two MF-3200 mechanisms, slide-in unit	GNI	AFS		"
21	floppy mini-disk storage unit	K-5561 (GDR)	two K-5660 floppy minidisk mechanisms, slide-in unit	"	"		"
22	fixed magnetic disk storage unit	GDR	two-four fixed disks, 15, 25, 35 Mbytes, 40 ms, slide-in unit	--	AFK		"

Following designations are used in table 1:

IRPR -- interface for radial connection of devices with parallel exchange of data (MM SM 004-76);
IRPS -- interface for radial connection of devices with serial exchange of data (NM MPK po VT 010-78);
INML -- interface for small magnetic tape storage units (NM MPK po VT 019-78);
IKMD -- interface for magnetic disk cartridge storage units (MM SM EVM 007-76);
SIF 1000 -- interface for radial connection of devices with parallel exchange of data (ASKI);
ISO -- interface for linear connection of USO [process communication unit] with serial data exchange;
GNI -- instrument interface for floppy disks;
ASP -- controller for IRPR interface;
ASI -- controller for SIF 1000 interface;
ASD -- controller for IRPS interface;
ATP -- controller for ISO interface;
AMB -- controller for INML interface;
AKB -- controller for IKMD interface;
AFS -- controller for GNI interface;
AFK -- controller for fixed magnetic disk storage unit.

status of the controller and peripheral. For peripherals 16-22, peripherals access memory in the direct access mode (DMA). Except for the SVE 30 memory control unit, the DMA mode is possible only through the SM-50/50-2 system bus or the SM EVM common bus.

The SM-50/50-2 microcomputer system is built on the modular principle and may be optimally matched in throughput and configuration to the application conditions. The following microcomputer configurations are possible using the system modules:

the K-1620 microcomputer in the form of a built-in computer with medium throughput;

the K-1620 microcomputer in the form of a computer complex with medium throughput (autonomous); and

the K-1630 microcomputer in the form of a computer complex with high throughput.

The computer throughput parameters are shown in table 2. Thanks to the program and interface compatibility with the SM EVM, it is possible to make use of the wide range of SM EVM software and peripherals. The system concept provides for future expansion of the spectrum of modules.

The K-1620 microcomputer is a medium throughput model. A built-in K-1620 computer is intended to operate as a problem-oriented computer included in a hardware composition. An autonomous K-1620 computer is intended as a stand-alone computer for solving general-purpose problems of control and data processing; it is built on the modular principle and may be optimally matched to the conditions of application by selection of the modules needed.

The 25 processor (ZVE 25) is the nucleus of the K-1620 microcomputer. It is built on a base of the U 830 LSI processing circuit and contains a control unit based on TTL [transistor-transistor logic]. The system architecture of the K-1620

microcomputer provides for connection of all system components through a common trunk--the SM-50/50-2 system bus.

The SM-50/50-2 processor-controlled system bus is a bidirectional interface through which addresses and data are transmitted multiplexed in time and in parallel. Data is exchanged synchronously for addresses, but asynchronously for data. The 25 processor realizes the basic SM EVM instruction set and is compatible through interface with the SM EVM through the BUM [interface converter for buses] and the SM-50/50-2 system bus.

The processor operates with microprogram control on the asynchronous principle of control. The K-1620 microcomputer is serviced by using a communications device connected to the SM-50/50-2 system bus through a serial interface (IRPS) and controller. There are also minor capabilities for service and display by using the front panel of the processor. In addition, the front panel has a display for fan malfunctions and the fill level of the support accumulators for holding data.

The K-1630 microcomputer has the highest throughput in the SM-50/50-2 system. It is intended for more comprehensive systems of small computers with higher throughput; it may be used for computations in real-time and multiprogramming systems and in multisubscriber systems. The K-1630 computer is built on the modular principle and may be optimally matched to application conditions thanks to available system components. The nucleus of the computer is the high-throughput 30 processor (ZVE 30), built on a base of LSI elements. The memory control unit (SVE 30) allows expansion of the range of addressing for the processor to 256K bytes and also realizes memory protection. The model K-1630 may also be equipped with an arithmetic processor (ARP 30) that allows fast processing of 32-64-bit numbers with floating point and 16-32-bit numbers with fixed point. The K-1630 microcomputer system architecture provides for connecting all system components through the SM-50/50-2 system bus and the ZVE 30 processor realizes the SM EVM instruction set.

The K-1630 microcomputer is designed as a slide-in unit in which the processor, memory and controllers are placed. Depending on the type, the peripherals are built-in, attached or desk units. Servicing of the K-1630 microcomputer is similar to that for the K-1620.

The ARP 30 arithmetic processor supplements the K-1630 microcomputer and cannot operate without the ZVE 30 processor. It is built on the base of the U 832 LSI arithmetic expander and also contains a number of registers and a control unit based on TTL. It operates with microprogram control. Aside from the basic arithmetic operations (addition, subtraction, multiplication, division and conversion operations), the ARP 30 executes a number of additional instructions in the format of numbers with floating and fixed point. The ARP 30 is linked to the ZVE 30 processor through the SM-50/50-2 system bus and direct links. The processor performs all address computations for the ARP 30, assigns data for operations and receives results after execution of operations. Data is exchanged asynchronously between the ARP 30 and the ZVE 30 and within the ARP 30.

System-defining integrated circuits. LSI circuits that have no prototype are used in the SM-50/50-2 computer. MOS technology was used to design these LSI circuits. They were developed especially for the SM-50/50-2, but are also so versatile that they may be used in other computers and electronic devices too. The following

Table 2. Computer Throughput Parameters

Parameter	K-1620	K-1630	ARP-30
Word length	16 bits. Parallel processing of words and bytes	similar to K-1620	with fixed point: 16 and 32 bits; with floating point: 32 and 64 bits
Number representation	with fixed point, radix complement	same	
Number of instructions	about 400 (including modification	same	30 basic instructions
Instruction system	SM EVM instruction set	same	--
Control principle	asynchronous microprogram control, horizontal microprogramming	same	similar to K-1630
Number of types of addressing	12	12	8
Number of general-purpose registers	8	8 + 8	9, of which 4 are accessible to the programmer
Range of addressing	32K words (memory -- 28K words, IO registers -- 4K words or 64K bytes)	128K words (of which 4K words are IO registers) or 256K bytes	
Interrupt system	vector organization of interrupt processing, 5 levels of interrupt, of them 1 level for DMA	similar to K-1620	
Levels of signals	TTL	TTL	
Preservation of data when power fails	available	available	
Automatic RESTART	available	available	
Real-time clock	clock cycle is 20 ms; serviced by software	similar to K-1620	
IO organization	software and direct access	similar to K-1620	
Organization of interrupt queue (stack)	available	available	

Continuation of table 2.

Parameter	K-1620	K-1630	ARP-30	
Operator communication	through remote console and front panel			
Execution of instructions: .ADD/SUB	microprogram	microprogram	with floating point of 32 bits, 5-12 μs	with fixed point of 16 bits, 1-5 μs
.MUL	by program	by program	7-15 μs	2.5-10 μs
.DIV	by program	by program	15-30 μs	7.5-30 μs

types of LSI circuits have been developed: U 830 -- LSI processing circuit, U 831 -- LSI control circuit, U 832 -- LSI arithmetic expansion circuit and U 834 -- LSI trunk adapter circuit.

All the LSI circuits have the dual in-line package (DIP) with 48 leads.

The U 830 LSI circuit is a cascade-connected processing circuit with eight bits for creating the computing circuits with microprogram control. Joining two or four of these LSI circuits increases the processing word length to 16 and 32 binary bits, respectively. Processing of one microinstruction takes about 1 microsecond.

The U 831 LSI circuit is a microinstruction memory circuit with asynchronous generation of signals. It requires no external clock. The microinstruction memory circuit is built in the form of a programmable logic matrix (PLM) with 140 terms (number of DNF). The PLM is programmed by masking. Information input to the PLM has 20 bits of input data and 8 bits of internal address for tracing. Thus, each input information may cause 2^8=256 read cycles, i.e. the maximum length of a microprogram is 256 microinstructions. Branching (up to 16 directions) is possible at any point in the microprogram. This LSI circuit is used either separately, or jointly with the U 831 LSI circuit in computer control devices, for control in controllers and peripherals or control devices without a computer. The content of the PLM may be optimized using the optimization program that operates with the YeS EVM [unified system of computers]. The U 831 LSI circuit in the SM-50/50-2 is used to control peripherals.

The U 832 LSI circuit is a cascade-connected circuit for building fast microprogram controlled arithmetic processors with a high number of bits. In addition to simple operations, multiplication and division of numbers with a fixed and floating point, as well as conversion of numbers from the fixed-point format to floating-point and vice versa may be performed.

The LSI circuit processes a 16-bit word. By connecting up to four U 832 circuits in parallel, processing may be expanded to 64 bits in stages of 16 bits each.

The U 834 LSI circuit, as a significant component in controllers, links the SM-50/50-2 system bus with any peripheral. This circuit may be used in the modes of programmed operation or DMA (direct access). Its basic functions are storing data on the current status of the device and controlling all IO operations performed by the controller. IO operations with the time of a bus cycle from 1.0 to 1.6 microsecond are possible, i.e. in the DMA mode, a data transmission rate of up to 10^6 bytes/second is possible.

8545
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FLOPPY DISK STORAGE UNITS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8 1980 (signed to press 17 Nov 80) pp 63-68

[Article by A. Pieszko, master, PNR [Polish People's Republic] and B. Gwizdala, engineer, PNR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] Floppy disk storage units were put into production on a series basis in 1977 (under license from the French firm Logabax). The Krakow Measuring Equipment PLant became the prime producer of these storage devices in the socialist countries.

The floppy magnetic disk storage units, with the national designation PLx45 DE, were tested in 1978 while operating in the SM-3 system and designated the SM-5602 in the unified system of small computers. Assimilation of series production of the SM-5602 by "MERA-KFAP" enterprises served as the basis for an extensive program of efforts to develop this licensed item. As a result, production was established and mastered for magnetic floppy disk storage units with the working designation of SP 45DE, intended for the "MERA" minicomputer systems produced in Poland.

However, the main purpose of the research was development of floppy disk units for the system of small computers (SM EVM). The storage unit (SP 55DE) intended for operation in the SM-3 system and the data preparation and processing unit (PSPD90) (fig. 1) [see below] have now been developed and made ready for series production.

These units underwent international tests and were included in the SM EVM nomenclature in 1979; series production of them began at the start of 1980.

The SM-5602 floppy disk storage unit contains a mechanism to drive the movement and set the heads of two floppies and a printed board with control circuits and channels for serial recording and reading of data. The flowchart for the SM-5602 and the signals by which the unit is linked to the selector guiding its operation are shown in fig. 2. The SM-5602 is assembled on a cast base. Each of the disks is inserted in a cartridge. The disks are placed on self-centering hubs driven by a synchronous motor. Each disk has a marker hole to synchronize the joint operation of the storage unit and the external devices and to determine the side in use at a given time with the help of photoelectric sensors (in the infrared range).

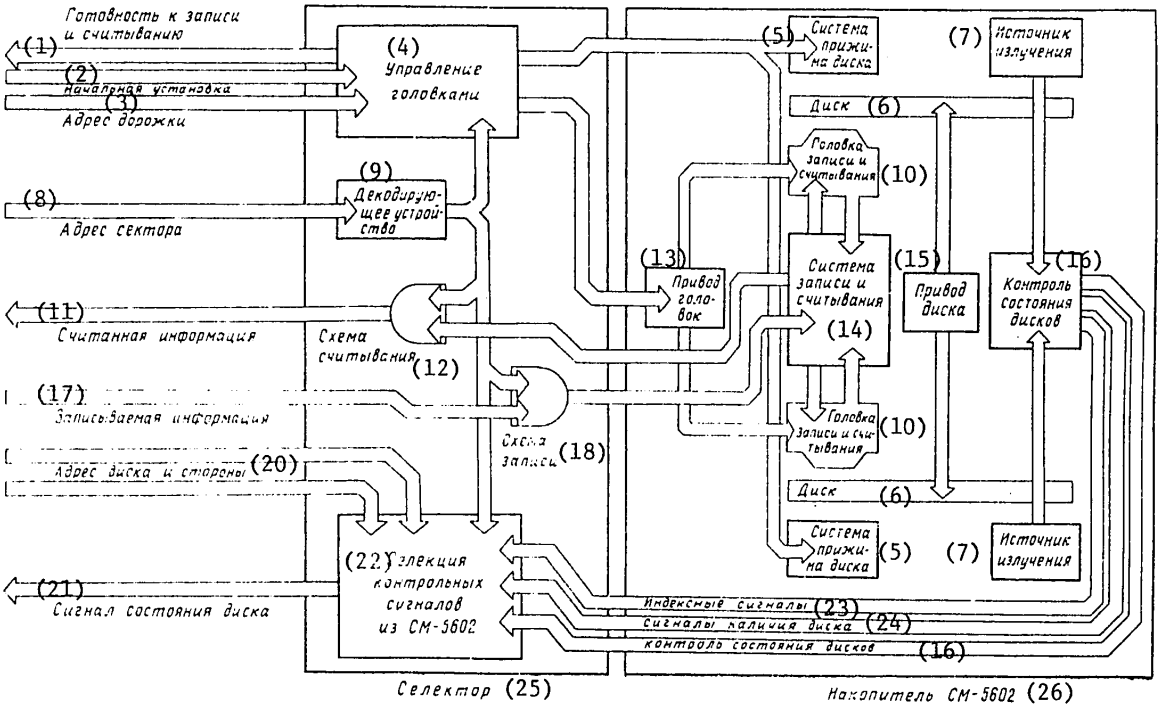


Fig. 2. Block diagram of the SM-5602 magnetic disk storage unit with the SP 55DE storage unit selector

Key:

1. readiness to write and read
2. initial setting
3. track address
4. head control
5. disk pressure system
6. disk
7. radiator
8. sector address
9. decoder
10. read-write head
11. data read-out
12. read-out circuit
13. head drive
14. read-write system
15. disk drive
16. disk status monitor
17. data being written
18. write circuit
20. disk and side address
21. disk status signal
22. selection of monitor signals from the SM-5602
23. index signals
24. disk availability signals
25. selector
26. SM-5602 storage unit

The disk heads are linked by a setting mechanism with a drive from the step motor. Each motor step shifts the head one track. Disk contact with the head for writing and reading is maintained by the disk pressure system--an electromagnet that drives the contact faces. Operation of only one head is possible.

The motor control circuit has a protective relay that ensures data is preserved when the power is inadvertently disconnected. The disk stops automatically when the cartridge covers are opened.

The SM-5602 has the following specifications:

Number of disks	2
Disk type	conforms to No. 149 ISO 97/11
Recording technology used	FM (DF NRZ)
Number of tracks on a disk	77
Total capacity of a disk, Mbits	3.2
Total capacity of a storage unit, Mbits	6.4
Usable capacity of a storage unit, Mbits	4.1
Average data access time, ms	205
Recording synchronization frequency, kHz	250
Disk rotation rate, rev/min	360 $\pm$2.5%
Voltage, V:	
for synchronous motor (50 VA, 50/60 $\pm$1 Hz)	$220^{+10\%}_{-15\%}$ or $115^{+10\%}_{-16\%}$
for step motor	48 $\pm$3%
for printed circuit board	+5 $\pm$3% (current to 2A)
	-6 $\pm$5% or -12 $\pm$10% (100 mA)

Environment parameters:

temperature range during operation, °C	+5 - +45
temperature range for storage without disks, °C	-40 - +55
humidity, %	20 - 80

The SP 55DE floppy magnetic disk storage unit is used to expand internal storage and organize rapid input-output of data in systems operating with the "Common Bus" interface (the SM-3, for example). Especially effective is the use of the storage unit as supplementary storage in real-time systems and as the main storage in office systems. The entire device is mounted in one panel and contains: the SM-5602 floppy magnetic disk storage units; the controller board that includes the formatter and selector (see the left part of fig. 2 for the block diagram); and the power supply.

The unit also includes a separate SM-3 interface adapter board made according to the norms OST 25 795-78 "Interface. Common Bus."

Unit parameters meet the requirements of the methodological materials MM SM EVM 002-76 and 003-76, and the design conforms to the "General Requirements for Equipment Esthetics and Human Engineering" of the NM MPK po VT [Standards of the Intergovernmental Commission on Socialist Countries' Cooperation in Computer Technology].

The main technical data for the unit are:

Number of accessible disks	2
Capacity of useful data, Mbits	4.1
Average data access time, ms	205
Mean time to failure, hours	1000
Validity, bits	10^9
Power	220V $^{+10\%}_{-15\%}$, 50 $\pm$1 Hz, 500-A
Power for interface adapter board	-5V, 2A

The structure and principle of operation of the controller can be traced by analyzing the flowchart of the formatter and selector. The formatter, assembled on three boards, realizes the dialog with the microprocessor, selection of the disk, side, track and sector, preparation of the data for recording on the disk, read-out of data and setting of the head on the threshold track.

These actions are determined by the microinstructions contained in the read-only memory (ROM). The microinstructions are grouped into microprograms that realize specific operations. A microinstruction determines the type of operation and the address of the arguments. ROM addressing is determined by the status of the control logic. This address may be the status of the address counter, a microinstruction, content of the main register or address in event of interrupts. Interrupt signals start subroutines to process them while the main program is delayed.

The wait register allows synchronizing the program run with an external asynchronous signal. The arithmetic-logic unit processes information in accordance with the instruction in the input registers or in the buffer main memory of the RAM [random-access memory] type.

The device performs the operation of data processing by using the main register. The result of the operation is placed in either the output registers of the buffer memory or in the main register. Buffer memory is used to increase the data transmission rate in a small computer. Data from the small computer is accumulated in buffer memory, then output to disk. Data read from a disk is put into buffer memory at the rate of 250 kbits/sec, but output to a small computer at the rate of 500 kbytes/sec. The data exchange between the small computer and the buffer memory is monitored by the arithmetic-logic unit.

Data to be written on a floppy magnetic disk passes through a cyclic monitoring circuit. A check character, determined by this circuit, is written to the data. When the data is read, the check character allows the monitor circuit to find errors made in writing or reading the data from the disk.

The selector, realized on one board, performs two basic functions: it classifies the data sent from the formatter, directing it to the corresponding disk as a function of the specified address, and generates signals to control the operation of the SM-5602 storage unit.

The PSPD 90 device for data preparation and processing substantially extends the capabilities of using a computer. It allows accumulation and systematization of data on floppies. Unit maintenance is simple. The operator guides the operation by calling a series of instructions from the keyboard. The instructions include:

basic operations (input, confirmation and verification of data);

auxiliary operations (retrieve, read and replace file names, retrieve data in a file, cancel recordings, service programs);

test operations (check the main units in the device and indication of malfunctions);

operations of automatic processing of data that contains possible calculations (addition, subtraction, multiplication and division) on fragments of data, and operations on files that allow creating new multidisk files and updating old ones, as well as printing back-up documents on a matrix printer; and

operations that realize telecommunications with a large computer, direct communications with a small computer, as well as recording of data on magnetic tape.

During execution of all these operations, the device outputs graphic indications and test comments on the monitor screen (video terminal) and light signals on the keyboard.

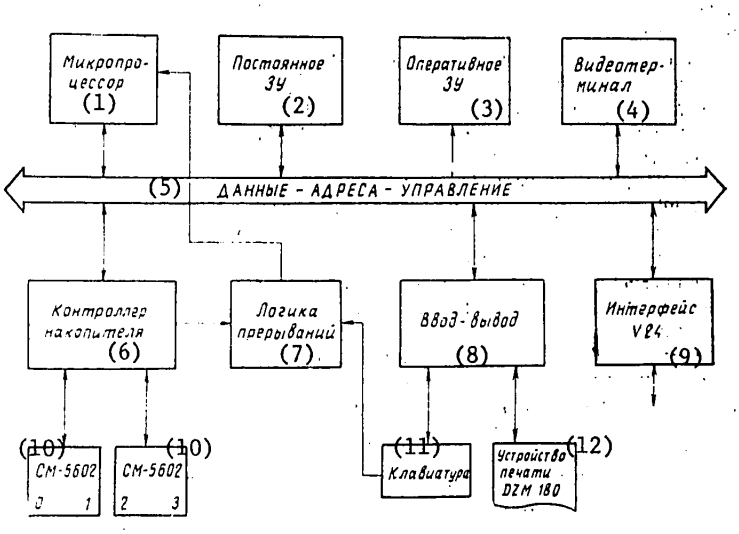


Fig. 3. Block diagram of the PSPD 90 unit for data preparation and processing

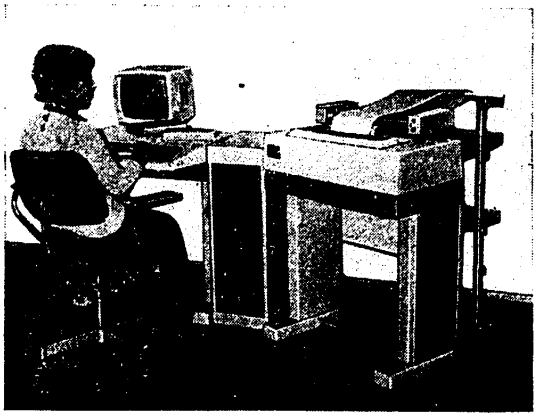
Key:

1. microprocessor
2. ROM
3. main storage
4. video terminal
5. data - addresses - control
6. storage unit controller
7. interrupt logic
8. input-output
9. V24 interface
10. SM-5602
11. keyboard
12. DZM 180 printer

The block diagram for the data preparation and processing unit is shown in fig. 3. This is a typical block diagram of a microcomputer with these peripherals: two SM-5602 floppy magnetic disk storage units, keyboard, screen monitor and DZM 180 matrix printer. The low cost of this arrangement is achieved primarily through the simple design of the screen monitor. The monitor receives from the "Video" board a complex signal containing the image and synchronizing pulses. Screen capacity is 512 characters (16 lines of 32 characters each). Any character may have a direct or reverse image allowing especially important information to stand out. The alphabet can be changed by changing the character generator realized with PROM circuits.

The keyboard is serviced completely by software and the key codes are a function of the table in the microcomputer memory.

Having provided a brief description of the three peripherals introduced into the system of small computers that use floppy magnetic disks as a data medium, the authors are prepared to send more details to those interested. Send your request to: MERA-KFAP, ul. G. Zapol'skoy, 38, 30-126 Krakow, Poland.



PSPD90 programming unit for the collection and processing of data.

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CSO: 1863/157

UNITS FOR COMMUNICATION WITH THE OBJECT OF CONTROL COMPUTER COMPLEXES IN THE SM EVM

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 69-77

[Article by A. Ya. Sokolov, engineer, USSR; L. A. Sopochkin, engineer, USSR; Yu. P. Strashun, candidate of engineering science, USSR; and L. A. Sergeyev, engineer, USSR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] Necessary for the functioning of an automated system to control technological objects are conversions and input into the system of data describing the status of the object, as well as conversion and output of control actions to the actuating mechanisms. In the control computer complexes (UVK) of the system of small computers (SM EVM), this function is performed by units for communication with an object (USO) that support input and output of analog and discrete information.

Developers of the first phase object communication units in the system of small computers were faced with the task of creating a set of functional modules and devices to build process control systems and systems for automation of scientific experiments and laboratory research. This set of USO's allows operating the SM-1, SM-2, SM-3 and SM-4 UVK's in the most varied sectors of industry, including power, machine building, metallurgy, mining, chemical, machine tool manufacture, as well as in a number of fields of scientific experimentation.

Typical of the SM EVM object communication units is:

the use of the design and element base for the system of small computers;

predominance of centralized configurations in development of systems;

use of remote grouped converters and commutators, as well as remote grouped units for normalization of signals from thermocouples and resistance thermometers for data acquisition from dispersed objects (at a radius up to 1 km); and

use of sets of modules with an outlet for unified interfaces and creation of an analog input subsystem that includes the entire measuring path in an autonomous complete unit.

The organization scheme for an object communication system, based on a set of modules of object communication units, is shown in fig. 1. The set contains:

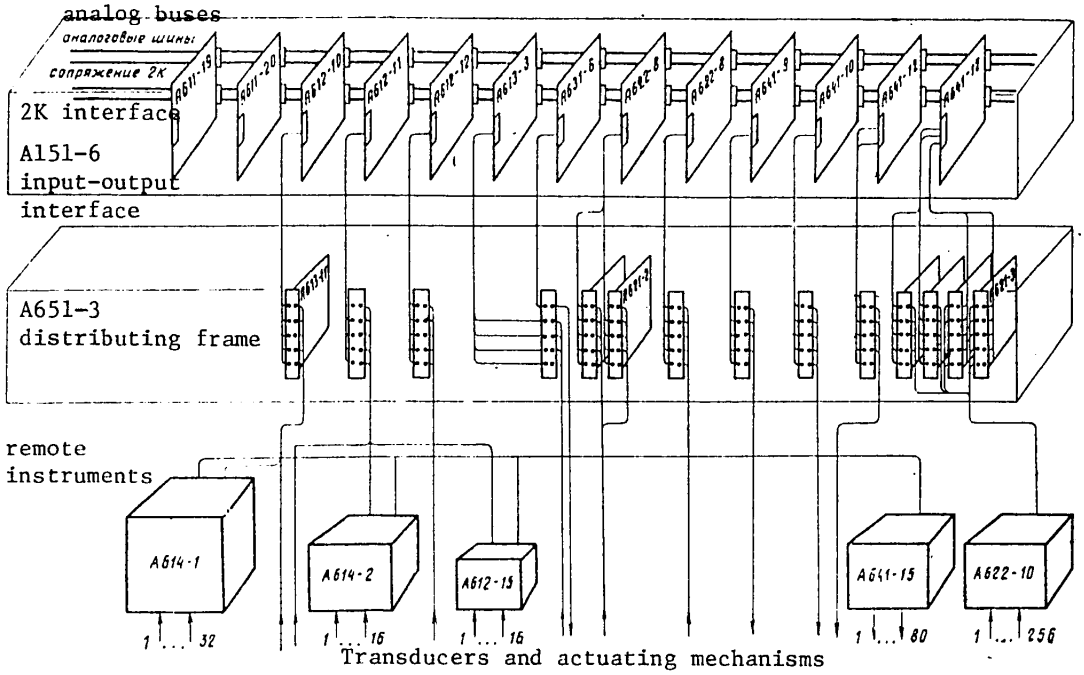

Fig. 1. Diagram of organization of a system, based on a set of USO modules, for communication with an object

modules for input of analog signals: the A611-19 analog-digital converter, the A611-20 analog-digital comparator module, the A612-11 solid-state switch, the A613-3 sampling and storage module, the A612-12 low-level signal switching and normalizing module, and the A613-11 normalizing module;

modules for input of discrete signals: the A622-8 module for input of initiating signals, and the A621-2 and A621-3 modules for normalization and galvanic uncoupling;

modules for output of analog signals: the A631-6 code-current converter module;

modules for output of discrete signals: the A641-9 contactless code control module; the A641-10 pulse signal output module, and the A641-12 discrete signal input-output module;

remote grouped converters and switches: the A614-2 alternating current signal transducer, the A614-1 thermocouple and resistance thermometer signal transducer, the A612-15 remote current and voltage signal switch, the A622-10 discrete signal input switch, and the A614-15 relay signal output switch.

A feature of this set of modules is the high rate of analog-to-digital conversion (time for conversion is 20 microseconds) with an error of 0.1 percent. The provided module for analog-digital comparison allows realizing by software the various conversion algorithms, making a comparison with settings, operating with the specified number of digits and changing the time of conversion. The sampling and storage

module fixes the instantaneous values of one or a group of signals from the transducers and precludes dynamic component errors in conversion. The set allows reception of signals directly from thermocouples and resistance thermometers, as well as from alternating current transducers by using remote grouped converters and switches at a distance of up to 1 km from the computer with transmission of information by analog current signals in the 0 to 5 mA range. The basic error of these converters (as a function of the range of the input signal) is 0.6 to 1.0 percent. The low-level signal switching and mormalizing module provides for signal reception in the ranges of 10, 20, 50 and 100 mV and amplification to the level of 5 V.

Program assignment of the operation mode to the module for input of initiating signals raises the convenience of operation with it, allowing the option of setting the mode either with interrupt signal normalization or with program polling of the status of the transducers.

The relay signal switch together with the modules for output of discrete signals provides the capability of shaping signals with a rating of 24 V X 2.0 A for output of control actions to the actuating mechanisms of direct and alternating current.

The set of modules discussed above has an outlet for the unified 2K interface to the SM-1 and SM-2 complexes and is connected to the SM-3 and SM-4 through a matching device for the 2K-OSh interfaces. At the same time, object communication units have been developed for the SM-3 and SM-4 control computer complexes that allow building a system from autonomous units. The units use the design and configuration solutions adopted in the SM-3 and SM-4 control computer complexes with an outlet for the unified interface "Common Bus" (OSh).

SM-3 and SM-4 object communication units allow:

normalization of resistance thermometer signals of all standard graduations;

automatic compensation for thermo-EDS [emf] of the free ends of the thermoelectric thermometers;

input and conversion into binary codes of low and high level analog signals;

suppression of general and normal types of noise in the measuring path for input of analog signals;

input of discrete and initiating signals;

input (output) of number-pulse signals;

output of discrete and analog signals; and

autonomous search for the address of the initiating channel and data exchange with the SM-3 and SM-4 processors through the OSh interface.

Functional capabilities are realized by three units designed in the form of autonomous complete units: remote normalizing unit (BNV), analog signal input unit (UVA) and the discrete signal input-output unit (UVD).

The remote normalizing unit (BNV) is designed to normalize resistance thermometer signals and automatically compensate for the thermo-emf of the free ends of the thermoelectric thermometers, caused by free end temperature deviation from 0° C. Up to 16 transducers may be connected.

The error in normalizing the signal of the resistance thermoconverters is $\pm$0.25%.

The error in the correction applied to the thermoelectric thermometer readings (°C) is given by the formulas: $\pm$ (1.1 to 6.0) X 10^{-3}t for graduations KhK and KhA; and $\pm$ (1.8 to 6.0) X 10^{-3}t for graduations PP and VR 5/20 (where t is the temperature of the free ends, °C).

Mean time to failure is 50,000 hours. Operating range of temperature for the unit is 5 to 50°C.

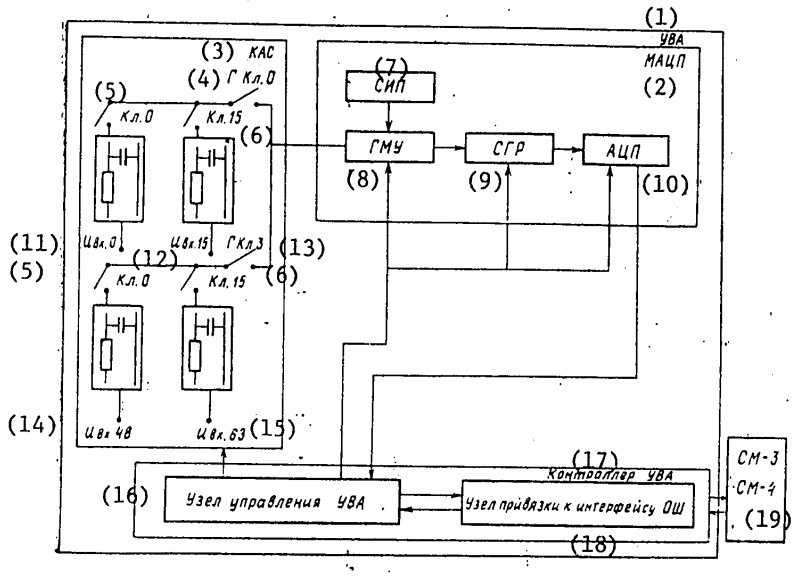

Fig. 2. Structural diagram of the analog signal input unit (UVA)

Key:

1. UVA -- analog signal input unit
2. MATsP -- multirange analog-digital converter
3. KAS -- analog signal switch
4. [expansion unknown]
5. [expansion unknown]
6. [expansion unknown]
7. SIP -- special power supply
8. GMU -- group scaling amplifer
9. SGR -- galvanic separation circuit
10. ATsP -- analog-digital converter
11. [expansion unknown]
12. [expansion unknown]
13. [expansion unknown]
14. [expansion unknown]
15. [expansion unknown]
16. UVA control unit
17. UVA controller
18. unit coupler to common bus interface
19. SM-3, SM-4

Analog signal input unit (UVA). The UVA features are a high rate of scanning channels with a low level of signals (not less than 2000 channels/sec), the capability of operating with a contact switch with general-type noise having an amplitude up to 100 V, and the availability of five ranges of low-level signals, including the ±10 mV range. The structural diagram of the UVA is shown in fig. 2.

The analog signal switch (KAS) that has two modifications--in contact (sealed contact reed relays) and contactless (MOP [metal oxide semiconductor = MOS]) keys--in addition to the keys and key control circuits, includes filters to suppress normal type noise, as well as protection circuits when MOS-keys are used.

The multirange analog-to-digital converter (MATsP) allows achieving fast total time for amplification, galvanic separation and analog-digital conversion (respectively, not more than 140 microseconds in the ±10 mV range, and not more than 100 microseconds in the ±5 V range with a general-type noise suppression factor of 60 to 80 dB at a frequency of 50 Hz as a function of input signal level). The MATsP has seven input voltage ranges from ±10 mV to ± 5 V and the input resistance is not less than 10 megohms.

The group scaling amplifier (GMU) in the UVA may change the structure for input signals of low and high levels. The GMU structure is varied by its control circuits in accordance with the operating program.

The UVA controller allows:

selecting channel and group keys in the analog signal switch;

connecting the amplifer to the switch upon the signal of the unit number decoder;

emitting the signal "Coding Permission" to the input of the analog-digital converter by timing marks for establishing the signal at the switch output or at the scaling amplifier output as a function of the UVA measuring path modification; and

exchanging signals with the common bus interface.

The structural diagram for the input system based on the analog signal input unit is shown in fig. 3. There are six versions of the analog signal input unit allowing a system to be put together from the basic and expanding modifications (in fig. 3, the individual modifications are indicated by the dash lines), each of which in the form of an autonomous unit has 64 channels each for input of analog signals:

UVA-0 and UVA-1 are the basic modifications which include the BKI-AV interface unit; they differ by switch type (contact or solid state);

UVA-2 and UVA-3 are the expanding modifications without an interface unit. They are connected to the UVA-0 and UVA-1. They have an analog-digital converter and serve as the basic element in the supplementary bay designed to increase the number of operating channels. They are distinguished by switch type (contact or solid state);

the UVA-4 and UVA-5 are modifications expanding the number of channels within a bay. they may be connected (up to three units) to the UVA-0 - UVA-3. Up to 16 autonomous units with a total of 1024 channels may be connected to one UVA controller.

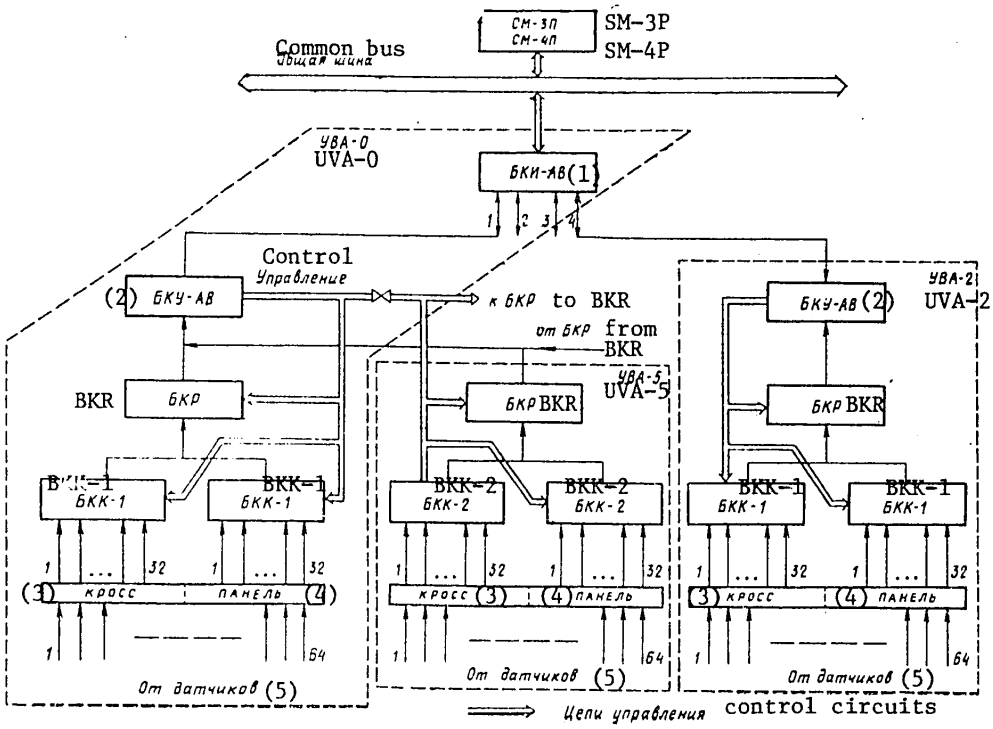

Fig. 3. Structural diagram of input system based on analog input unit (UVA)

Key:

1. BKI-AV -- cassette interface unit
2. BKU-AV -- cassette control unit
   BKR -- cassette amplifier unit
   BKK-1, BKK-2 -- cassette units with contact and solid state switches, respectively
3. distributing frame
4. panel
5. from transducers

Basic specifications of the analog input unit (UVA) are:

number of channels	64
types and ranges of input signals:	
direct current voltage	±10, ±20, ±35, ±50, ±100 mV; ±1, ±5 V
direct current	±5 mA
basic error in measuring voltage and current:	
in the ±10 to 100 mV ranges	±0.6%
in the ranges ±1 V; ±5 V; ±5 mA	±0.25%
frequency of parameter polling, channels/sec:	
solid state version:	
in the ±10 to 100 mV ranges	2000
in the ranges ±1, ±5 V	6000

contact version	200
general-type noise suppresion factor	
at frequency of 50 Hz, dB:	
for low-level signals	80
for high-level signals	60
normal-type noise suppression factor	
at frequency of 50 Hz, dB	60

The discrete signal input-output unit (UVD) is designed to receive the signals of the discrete transducers and emit discrete and analog control actions to the various mechanisms and terminals. The functional capabilities of the UVD are determined by the set of functional input-output modules: discrete and initiative signal input modules, the pulse signal input-output module and the discrete and analog output modules.

Each of these modules when installed in the cassette control unit (BKU) has an outlet to the internal unit interface in the UVD, which supports the serviceability of the arbitrary set of modules in each cassette control unit. An autonomous complete unit may contain up to four cassette control units, each of which has four locations for functional modules and a cassette interface expander unit (BKR).

The structural diagram for the discrete input-output system based on the UVD is shown in fig. 4. As seen from the diagram, up to 12 discrete signal input-output units (UVD) with over 3000 input-output channels may be connected to one BKI-DV interface unit. The maximum number of channels for input-output in one autonomous complete unit is 256. In addition to data exchange through the common bus interface, the UVD controller locates the address of the initiative channel.

UVA and UVD software is supplied with the units and contains the following programs:

UVA "Metrology" which provides by statistical methods an assessment of the metrological characteristics for each measuring channel;

a program to compare measured parameters with settings;

a program for averaging parameter values;

a program for linearization of the nonlinear characteristics of the transducers and scaling;

the UVA driver;

the UVD driver;

the UVD controller test; and

the UVD module test.

In addition, the "Typical User Task" program is supplied, which implements program polling of all channels for analog signal input, linearization of nonlinear characteristics of the transducers, scaling and averaging of parameters and output of parameters to a printer and alphameric displays.

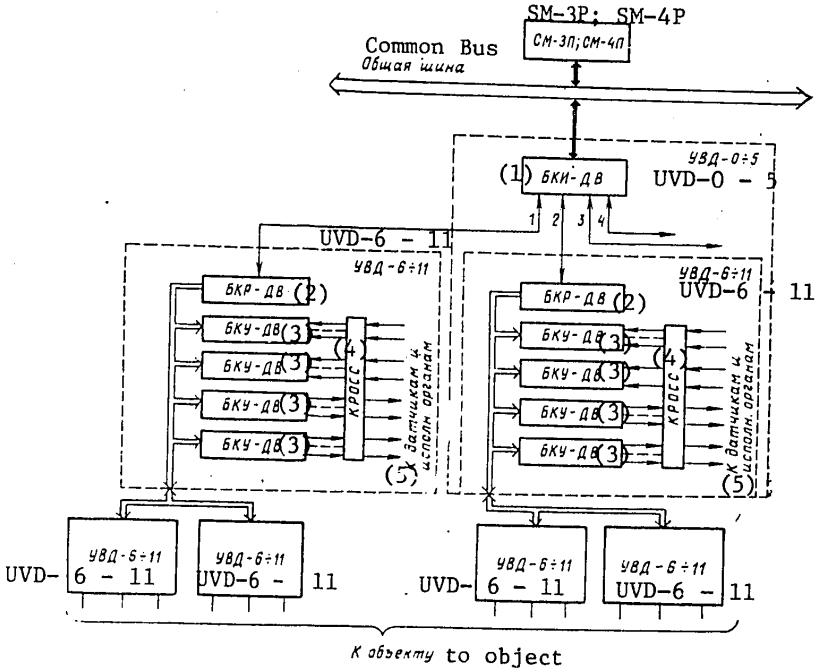

Fig. 4. Structural diagram of the discrete input-output system based on the discrete signal input-output unit (UVD): UVD 0-5 and UVD 6-11 are any of the given six modifications of the UVD

Key:

1. BKI-DV -- interface expansion unit
2. BKR-DV -- interface expander unit
3. BKU-DV -- cassette control unit with four locations for functional modules
4. distributing frame
5. transducers and actuators

The units operate under the control of the PLOS RV or DOS RV real-time operating systems.

As a result of the development of the SM EVM USO, functionally complete object communication hardware complex and software have been developed that give control computer complexes broad capabilities for operation in the most varied applications.

The second phase of the system of small computers envisions extensive use of microprocessor technology in building object communication units. This will allow:

building programmable object communication units in which some functions previously performed by hardware can be implemented by software; and

decentralizing the acquisition of analog and discrete data and reduction of it.

The lack of experience in using microprocessors for these purposes leads to the need of making a number of studies, including:

the effectiveness of programmable object communication units as compared to previous units by the criteria of functions performed, technical characteristics, cost and reliability;

principles of organizing data acquisition in territorially dispersed objects;

methods of enhancing noise immunity of object communication units;

methods of enhancing data systems reliability and viability in dispersed objects and formulating additional requirements for object communication units; and

methods of enhancing central processor response to a change in status of the individual aggregates of a dispersed object.

In addition, the expanding application of computers in the national economy is presenting a number of new problems to the developers of object communication units:

development of small-number-channel and multichannel decentralized object communication units having small dimensions and high reliability on the new design and element base of the system of small computers;

development of object communication units with enhanced precision (resolution of 10 microvolts at a level of 5 V), speed of response (polling frequency up to 250 kHz) and noise immunity of the measuring path;

development of object communication units with high-speed sampling and storage circuits for dynamic analysis of processes;

development of object communication units with multichannel analog output and storage of the analog signal; and

development of object communication units with output of discrete signals increased in strength.

Solving these problems will raise sharply the effectiveness of control systems and ensure high reliability and accuracy in operating them while simultaneously reducing cost, dimensions and weight of the equipment.

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FOBOS OPERATING SYSTEM FOR SMALL COMPUTERS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 87-92

[Article by I. Machacka, engineer, CSSR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The base software for the SM-3 and SM-4 computers is a group of operating systems (OS) that allow satisfying all user requirements--from data reduction to solving computational problems in the batched and interactive modes and problems in real time. The experience of operating the first SM-3 computers has shown that the majority of users prefer at this stage to implement the FOBOS (Background-On-Line Base Operating System) operating system. In the list of OS for the system of small computers (SM EVM), the FOBOS system belongs to the medium-level systems with respect to capabilities and capacity.*

The FOBOS system can be used in small and medium complexes with respect to configuration, but in the process the specific user requirements for the operating system have to be taken into account. Magnetic disk storage, which may be offered by the various types of devices in this class in accordance with the specific configuration, serves as the medium for FOBOS programs.

The OS may operate in the single-program or multiprogram mode, under which simultaneous processing of two user programs is possible.

The FOBOS system can control the following set of hardware:

the SM-3P or SM-4P central processor;

main memory. Minimum size: 8K words when operating in the single-program mode (12K words for batch processing), 16K words when operating in real-time mode with a background task. Memory of the central unit is not restricted. OS uses up to 28K words of memory;

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* See: Prachenko, V. D. and Khristochevskiy, S. A., "A Real-Time Operating System for the System of Small Computers," TRUDY INEUM, issue 66, 1977.

peripherals (minimum composition: console terminal and magnetic disk storage (resident of system))**: perforated tape input unit, perforator, card input unit, typewriter, display, matrix printer, standard magnetic tape unit, magnetic tape cassette, floppy disk, fixed-head disk, plotter and object communication unit.

OS programs are functionally divided into three groups: control programs, translators and utilities. The main part of the control programs is the monitors. The FOBOS system has single-program and multiprogram monitors. One of them is used in operation depending on the operating mode selected.

FOBOS allows processing of programs written in ASSEMBLER, FORTRAN, BASIC and FOKAL. FOBOS translators operate as compilers from ASSEMBLER and FORTRAN. This means that in the process of compilation, a program is obtained in relative addresses (object module). As a result of processing in the next stage, the linkage editor forms a load module--a program ready for operation. The BASIC and FOKAL translators are interpreting programs (interpreters) that allow the user to build and operate programs in the interactive mode.

FOBOS control programs. As noted, each OS operating mode (single-program or multiprogram) has its own control program, the main part of which is the monitor. Its other components are the programs controlling input and output [IO]. The FOBOS monitor has a modular structure so that at each moment in time, the part of the program that is used at a given time is in main memory. The monitor consists of three main modules and in operation is closely tied to the other modules that are IO device control programs.

The part of the monitor permanently in main memory is called the resident module. The other primary modules are the communications module and the file control module which are called into main memory when needed. Control modules of all devices, except the system disk device, are also written from disk into main memory only when needed; after completion of the operation, they can be erased from main memory or overwritten by another program.

Programming language translators. The FOBOS system contains programming language translators. The user chooses the programming language as a function of the type of problem to be solved. A program may be written in FORTRAN IV, BASIC, FOKAL, MACROASSEMBLER or ASSEMBLER. Object modules, obtained from translating FORTRAN source programs, can be linked to modules translated from ASSEMBLER. A COBOL translator will be included in the operating system in the future to process economic problems.

The MACROASSEMBLER is an efficient, multipurpose, basic means of programming. It translates a source program in two stages and requires a minimum of 12K words of main memory (OZU). The macroassembler allows use of the macroinstruction library. The system library of system macroinstructions and a user's own macroinstruction library may be combined by using the linkage editor.

** The console terminal usually is a display with a typewriter or printer. The OS medium may be cartridge disk, floppy or disk with fixed heads.

In connection with the macroassembler needing 12K words of main memory, for user needs there are two programs: MACROPROCESSOR and ASSEMBLER that use 8K words of main memory. The macroprocessor generates the macroexpansion in one pass. At input it traces the group of source macroinstructions and at output issues a program in the form of ASSEMBLER instructions in symbolic form, obtained in the macroexpansion process. Thus, the program obtained serves as a source file to be translated by ASSEMBLER. ASSEMBLER is a two-pass translator, functioning in an 8K-word section of main memory. Thanks to the use of the macroprocessor and the ASSEMBLER, the user has almost all the functions of the macroassembler as his disposal, plus the library of all system and user macroinstructions.

FORTRAN IV is used in the FOBOS system. The FORTRAN compiler processes a source program and performs functions of optimization. Optimization of the source program consists in ordering the machine code so that the program takes up the minimum memory and processing occurs as fast as possible. At output the compiler creates a program in machine codes in the form of an object module without the aid of the assembler. The FORTRAN compiler now operates in the smallest complexes with respect to configuration that have 8K words of main memory.

A program compiled in absolute addresses may be used for smaller configurations too; such a program is put into the machine from a perforated tape input unit. The system library of FORTRAN subroutines may be used in combination with FORTRAN; the library contains a file of functions that expand the capabilities of FORTRAN instructions and allow solving problems in real time.

BASIC for a user is intended for solving problems in the interactive mode. This mode of operation leads to an overall savings in computer resources (storage and processing time) used to solve problems. The BASIC translator is an interpreter. Source language instructions are converted into compact, easily executable code and placed directly in main memory. Upon the instruction RUN, this internal code is interpreted and processed as a program. Using the instructions LIST and SAVE, the internal code is translated into source symbolic form. Sequential processing by instructions is used for debugging and creating programs or for using the computer as a calculator. The source program is executed either by individual instructions, or processed as a whole. The CALL instruction is used to call special functions or those introduced by the user; CALL allows calling a function by its name and sending parameters to it. Users may create functions as subroutines written in ASSEMBLER. There are also functions to process graphic problems that may be called by CALL.

BASIC for several users is an expanded version of BASIC for a user. It allows simultaneous operation by up to eight users in the interactive mode using the monitor for one problem and 24K words of main memory, or by up to four users with 16K words of memory. In the interactive mode with 28K words of memory, four users may operate simultaneously. Users may have their own number and password for their files.

FOKAL belongs to the class of simple languages used in the interactive mode. The FOKAL translator is an intermediary in the FOBOS system that allows the user to operate in the mode of interaction and program execution. FOKAL is similar to BASIC in its semantic and syntactic data. FOKAL may operate with data files with a sequential or virtual structure. Data may be in the form of an integer (with or without a sign) with floating point, with double precision or it may be stored in symbolic form (in bytes).

COBOL. The COBOL translator, now under development, will give the user an efficient means of programming problems in economic data processing. FOBOS system COBOL comes from the language definitions of ANS X3.23 1974. A low-level language kernel and some modules for other functions have been realized in the translator. Functions not supported by the translator, for example sorting and output table generator, will be performed by special utilities that will be delivered with the compiler,

Utilites. Text Editor is an interactive program oriented to symbolic texts that allows scanning of sequences of symbols and textual manipulation. This program is used primarily to process symbolic files representing a program in source form. The program operates in three modes: processing by symbols, execution of instructions on strings and instructions pertinent to the entire field of display.

Linkage Editor processes and links object modules (in relative addresses) and creates the load module that can be directly placed in main memory and starts it. The linkage editor offers the usual capabilities, for example, automatic scanning of the library and creation of overlapping structures (when program segmentation is used).

Library allows the user to create, update, modify, reduce and maintain the library file. The user has at his disposal a set of operations supporting these functions.

Any library is a file having a list of library programs, a catalog of addresses (or table of entry points) and one or more modules. Individual modules in the library file may be programs used repeatedly, and subroutines used in various programs, logically related, and may create a single unit. For example, a typical library file is a set of mathematical functions used in FORTRAN programs.

The Debugging Program (debugger) allows debugging translated programs. Through the console keyboard, a user may interact with the debugging program and the program to be debugged. In the process, he can:

analyze and modify the contents of any memory cell, the contents of registers, the processor status word and the internal registers of the program being debugged;

start the entire or a part of the program being debugged;

obtain a precise description of the so-called points to be debugged (halt points);

retrieve words in the program being debugged by the given binary code;

calculate the shift for address assignment; and

place a specific value in the needed byte or word.

Object Module Editors are used to modify modules (files) output by the ASSEMBLER or FORTRAN translators. The object module editor is used when correcting programs that exist only in .OBJ form (when the source symbolic program is lost). It cannot be used to correct libraries created by the library program, but it can be used to correct object modules from which the library is created.

Load Module Editor is used to modify machine code in a load module file in nonrelocatable form, i.e. in the .SAV form. The load module editor may also be used in the debugging program to find and then change the contents of words and symbols within the file.

The File Housekeeping Routine peforms these functions: copies files individually or in groups, expands, eliminates or renames files, exchanges files between devices, etc. A major program function is the capability of packing copies on external storage and thereby bringing open sectors of memory into one area; in the process, the efficiency of using continuous structure files increases.

File Comparison Routine is used to compare two symbolic files. In the process, the routine prints out detected noncoincidence on a specified peripheral.

File Print Routine prints the contents of a part of or the entire file on the console terminal or printer. Contents may be printed in one of three forms: octal by words, octal by bytes or in the Radix-50 format.

File Converter converts files transferred from other operating systems in the system of small computers to the FOBOS system.

Batch Control Program is used as a means of creating the job stream at system input and supporting batched processing in the FOBOS operating system. The input stream may contain both FOBOS monitor commands and special commands processed by the batch control program. When these commands are used for job control, the input stream may be transferred to other operating systems in the system of small computers that have the batch control program.

System Operating Modes. The FOBOS operating system allows running and solving problems in the interactive or batched mode. User tasks consist in processing data for various scientific, technical, mathematical and economic calculations or operating in real time. Program creation, data processing or numeric calculations are most often done in main memory, in the single-task mode--in-line or background.

In real time, the system operates in either the single-task mode or the two-task mode (one task is handled as in-line, the other as background).

In the multiprogram mode, the real-time task has the higher priority, and as the background task (lower priority), the user may solve a problem in real time, or perform data processing or digital calculations, or using facilities available, translate and debug his own programs.

In the process, system response time to real-time tasks is important, for example to signals from the object of control. Naturally, a background real-time task should not be as critical to response time as the in-line task.

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CSO: 1863/157

IRIS DATA BASE FOR A HIERARCHIC MULTIMACHINE COMPLEX

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 93-96

[Article by V. D. Prachenko, engineer, USSR; Ye. N. Filinov, candidate of engineering science, USSR; and S. A. Khristochevskiy, engineer, USSR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] Sufficient experience has been gained in designing systems to manage data bases (BD) in the CEMA countries. Systems such as the OKA [1] for the YeS EVM [unified system of computers] or the integrated data processing system (SIOD) [2] for the M-4030 UVK [control computer complex] and others have become widespread. These systems feature the capability of being used as the basis for creating centralized data bases with orientation to use in automated production control systems and systems for organizational control.

In our view, the use of centralized data bases in real-time systems, in particular in systems for control of industrial processes and scientific experimentation, etc., is very promising. Hierarchic multimachine complexes, created on the base of small computers and computers with medium and high throughput, may be used for this purpose. At the lower levels of hierarchic complexes, small computers are used for the functions of control proper, data acquisition and reduction, and data transmission to higher level computers fitted with centralized data bases. This is exactly the approach adopted in designing the hierarchic distributed information system (IRIS) intended for operation with data bases in multimachine complexes of the system of small computers (SM EVM) and the M-4030 UVK.

The M-4030 UVK is charged with data base management functions in the IRIS. Special program interfaces link real-time user programs functioning in the system of small computers with the M-4030 data bases. In addition, IRIS includes program facilities allowing use of the small computer as a telecommunications processor. For this purpose, IRIS has a special interactive language allowing interaction with data bases by using terminals connected to the SM EVM common bus through remote communication adapters (ADS). The IRIS structure consists of three interrelated subsystems (fig. 1): the IRIS/BD (data bank), the IRIS/TO (teleprocessing) and the IRIS/KM (complex).

The IRIS/data bank functions in an M-4030 UVK and is an expanded version of the integrated data processing system with the inclusion in it of new functions:

support of direct access to any aspect of the data base through creation of specialized (inverted) lists which reduces retrieval time considerably.

organization of simultaneous operation of the same or different programs with several data bases (multibank mode);

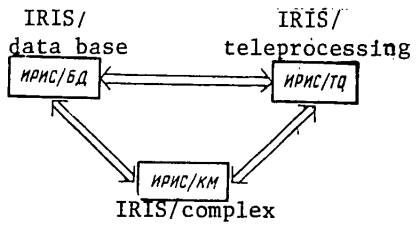

Fig. 1. The IRIS system structure

sanctioning of access to data (i.e. granting right of access as a function of user category) through input of keys-passwords;

capability of system checkpoint and restart;

capability of operating with two-level hierarchic structures of data; and

capability of managing a "temporary" data base, i.e. selection and localization of a subset of data base records in a special data base area for the time of operation with this data.

In the process, all SIOD functions are fully preserved in the IRIS data base which allows converting a SIOD data base to an IRIS data base. Also fully preserved is the program interface with the resident program of the IRIS data base, which allows all application programs developed earlier for the SIOD to be used with the new data base.

The IRIS complex is a set of program interfaces for both the M-4030 and the SM EVM supporting interaction of SM EVM real-time programs with the resident program of the IRIS data base that operates in the M-4030 UVK. Intermachine communication is supported by the use of the USVM (computer communication device).

Program interfaces for the IRIS complex on the SM EVM side function under the control of the background-in-line real-time operating system (FOBOS) which allows the application of IRIS for operating in control systems, automation of scientific research, etc. Program modules for the IRIS complex in the SM EVM include the USVM driver and the communications module.

On the M-4030 side, the USVM is controlled by the data exchange system (SOD) to which the operation of the USVM driver is strictly matched. Interaction of the program components is shown in fig. 2. The communications module in the SM EVM is included within the user programs. It supports sending queries from a program to the data base and receiving answers from it. For this, the user must, by specific rules, fill a special interface section, in which the data base queries are contained and to which the answers are sent.

It should be noted that a user program may function in both the in-line and background partitions of the FOBOS. On the M-4030 side, a similar interface module supports communication with the IRIS data base control program. It receives the previously filled interface section from the SM EVM and after accessing the data base sends it back by using the SOD and the USVM driver to the SM EVM user's application program.

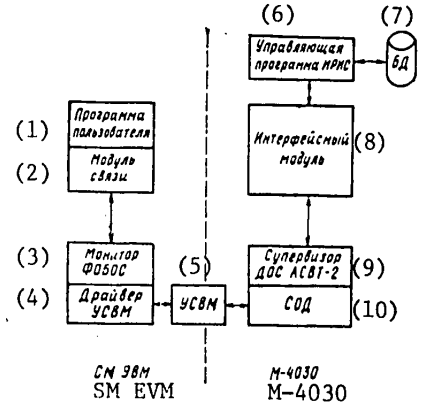

Fig. 2. Interaction of Program Components

Key:
1. user program
2. communication module
3. FOBOS monitor
4. USVM driver
5. USVM [computer communication device]
6. IRIS control program
7. data base
8. interface module
9. ASVT-2 DOS supervisor
10. SOD [data exchange system]

IRIS/teleprocessing is a subsystem of the interactive access to the IRIS data base and supports this access in two modes, functioning jointly or separately: through the M-4030 data transmission multiplexor under control of the data transmission system (SPD); through the SM EVM connected to the M-4030 through the USVM (in this case, IRIS/teleprocessing operates jointly with IRIS/complex).

When operating in the first mode, there may be connected to the communications lines SM computers that in this case are used as concentrators or batch terminals for remote input of jobs to the batch programs of the IRIS/data base. In the second mode, the SM computer performs the functions of controlling the operation of the terminals, thereby unloading the M-4030 UVK.

For operating under the control of IRIS/teleprocessing, the user is given a special interactive language. This language facilitates the user's operation with the data base and includes three groups of statements: control statements, data manipulation statements and service statements.

Control statements control terminals and allow conducting the dialog protocol or individual parts of it.

Data manipulation statements support realization of queries for retrieval and direct change of data. The main statements include statements for opening and closing the data base, and obtaining information, and retrieval statements in the modes of query, question, counting the number of answers, etc.

Service statements allow changing the format for output of the answer to a screen, repeating access to the data base, and obtaining reference information.

The interactive language available to the SM EVM user is a subset of the language realized for the M-4030 and is similar to it in its functions and capabilities.

For the functioning of the full complex of IRIS programs during operation of all three of its subsystems, the following hardware configuration is the minimum needed:

M4030: central processor, 256K bytes of main memory, console, two magnetic disk storage units, ATsPU [alphanumeric printer], data transmission control unit and card input unit;

SM EVM: central processor SM-3P or SM-4P, 56K bytes of main memory, computer communication device, two magnetic disk storage units, perforated tape input unit, alphanumeric printer, console and video terminals (maximum of eight).

Thus, IRIS gives the SM EVM user all the capabilities for operating with a data base with a small-size memory (56K bytes) and a real-time control operating system.

This suggested use of SM EVM in hierarchic multimachine complexes is very promising for operating in control systems needing an efficient real-time system at the lower level and the capability of managing a large data base at the upper level.

The system for managing the data base proper is realized on the M-4030 control computer complex. Since the basic set of instructions for the M-4030 and the YeS EVM are about the same, transfer of the data base management system to the YeS EVM should not be difficult. It is also advisable to develop the IRIS program components in the small computer to create a data base in it that is capable of interacting with the data base in the upper level computer.

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CSO: 1863/157

COMPUTER INSTRUCTION INTERPRETER

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 142-144

[Article by D. Simeonov, scientific associate, People's Republic of Bulgaria (NRB), and B. Iliyev, scientific associate, NRB, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The basic computer functions of the YeS EVM-2 ("Ryad-2" [series-2]) system have been realized by using a standard instruction set that is an expansion of the set used in the YeS EVM-1 ("Ryad-1") system. For a series-1 computer, data fields with fixed length such as a halfword or doublewords are stored in main memory by the address of the integral boundary for the given unit of information. This requirement does not pertain to series-2 computers: storage of an arbitrary byte boundary of the operands is permitted for the majority of nonprivileged operations.

Software that extends the effectiveness of computer systems has been and continues to be developed for series-2 computers. In many cases, the new developments can be adjusted and checked on series-1 computers, and even utilized if this is expedient. For this purpose, it is sufficient, for example, to create an "Interpreter" program that is able to simulate the nonprivileged instructions of the expanded set and align the operands at the integral boundary when necessary.

Two approaches to developing an interpreter are possible: minimize memory size or maximize response speed.

In the first case, instructions are prepared for execution in a general subroutine that analyzes them as a function of the format of the computing address of the operands. With RX format instructions, the second operand is also aligned at the address of the integral boundary. Then a jump is made to one or another subroutine as a function of the operation code of the interpreted instruction. With this method of organizing the interpreter, a large number of checks are performed which reduces the response speed of the general subroutine, but memory size is minimized.

The second approach is more efficient. In this case, each instruction is interpreted by a separate subroutine that allows eliminating a number of checks on the format of an instruction and its operands. A five-fold greater memory size is required to hold the interpreter in rough estimates when interpreting instructions by the second method, but a 1.5- to 3-fold greater response speed is achieved.

Following is a brief description of the interpreter developed at the EVTs [experimental computing center] of the IVT (Institute of Computer Technology, Sofia, NRB) and used in adjusting some new software components.

To achieve high speed, the interpreter is included in the supervisor nucleus. It processes program interrupts by operation code and by situation adjusts the instruction operands to integral boundaries, executes the instructions and transfers control to the program that called the program interrupt at the interrupt point. The interpreter consists of three subroutines for processing instructions by formats: register-register (RR), register-indexed store (RX) and register-store (RS).

When an attempt is made to execute an instruction with an opcode that does not exist for this processor, a program interrupt is registered for the opcode. Also, if an instruction requires an address of its operand to be aligned by integral boundary and this condition is not met, a program interrupt for the condition is registered. All types of program interrupts are recorded in main memory by writing the old SSP (program status word) [PSW] and selecting a new one.

The reason for the interrupt is identified by the corresponding interrupt code written in the PSW. Automatic entry to the interpreter is provided for upon receipt of an interrupt, since the address in the new PSW during a program interrupt is changed and indicates the point of entry to the program.

The characteristics of the instruction that caused the program interrupt, and its format and address are determined by using the PSW with the program interrupt. After all necessary values are determined and analyzed, a jump is made to the appropriate subroutine to interpret and execute the instruction.

The interpreter processes only program interrupts for opcode and condition. Other types of program interrupts are sent for processing to the standard program that is a part of the supervisor.

During operation of the interpreter, input-output interrupts are masked. Other program interrupts and interrupts involving access to the supervisor are not possible. During operation in the multiprogram mode, the interpreter services all active partitions. When a lower priority program is being serviced, higher priority programs are in the wait mode, although they are ready for execution, since the interpreter operates in the supervisor mode.

The interpreter may be obtained through the Central Library for Documentation and Programs (NRB, Sofia, ul. Kamenodel'ska, 6a).

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CSO: 1863/157

SM-5304 MAGNETIC TAPE STORAGE UNIT

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 139-142

[Article by L. Mirgos, engineer, Polish People's Republic, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] The SM-5304 magnetic tape storage unit (see photo reproduced below) is designed to store information in systems for data preparation (used for source data storage), data transmission (used as buffer storage), data conversion, data processing (used as external storage), automatic equipment and telemetry (used as a digital recorder).

The SM-5304 magnetic tape storage unit records and reproduces information on half-inch magnetic tape. The magnetic tape moves at a speed of 25 ips (0.635 m/s) under the unit of magnetic heads, consisting of a ferrite read-write head with two gaps--for write and read and an erase head. The recording is made on nine-track tape using the method of "nonreturn to zero," invert (NRZI) at a density of 800 bpi (32 bits/mm) or the method of phase encoding (PE) at a density of 1600 bpi. Data is written, read and erased on tape in accordance with the ISO standard which ensures full data compatibility with devices having the same write format. The tape drive method causes no program restrictions. Tape tension is controlled by spring supports. The drive arrangement in the SM-5304 allows use of reels up to 10.5 inches (267 mm) in diameter.

The SM-5304 can operate autonomously or with a computer. For interaction with a computer, a control unit is used that has an outlet to the interface conforming to MM SM EVM [Methodological Materials for the system of small computers], "Small Magnetic Tape Storage Units--Interface." The SM-5304 fits standard frames of 19 and 24 inches. It consists of three panels.

The mechanism and drive panel contains the set of circuits and assemblies needed to drive the tape. The following units have been mounted on the panel face:

capstan drive motor;

reel drive motor;
buffer levers to maintain required tape tension using spiral springs;

magnetic heads assembly, mounted on separate board along with spring idlers and a dust remover;

tape start-end sensors, and sensors for extreme positions of buffer lever;

capstans that direct magnetic tape motion; and

read preamplifier.

Mechanisms located on the panel are protected by a housing. At the upper part of the panel are the push-button controls and light indicator, as well as the electronic circuits controlling drive operation.

Located on the rear side of the panel are: capstan drive circuit, reel drive circuit, panel assembly cables, cable connectors for power supply.

The electronics board contains the circuits for the information transmission channel. Assembled on the board are the circuits for read, write and interface. The electronics board is connected with the other units using cables with connectors for the read preamplifier, record head, automatics board and power supply.

The power supply is an autonomous module containing five sources of stabilized voltage and six sources of unstabilized voltage for supplying the electronic drive circuits and light indicators. It is supplied from a network of single-phase current with a voltage of 105 to 250 V and a frequency of 48 to 60 Hz. The power supply is inserted into the storage unit cabinet from the rear.

Tape is moved under the heads by the drive capstan set on the shaft of the bidirectional direct-current motor. The tape drive is regulated by speed. Used as the feedback signal source is the tachometer, the frequency of pulses of which is converted into the level of voltage.

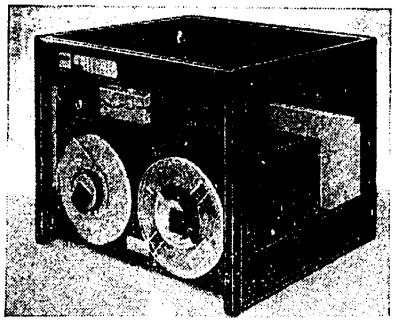
The reel drive includes the two reels--removable and fixed, operating in the arrangement of the servomechanism with regulation by position. In the tape path between the capstan drive and the reels, there are buffer levers that maintain a constant tension of the tape by using spiral springs. Use of buffers allows obtaining great acceleration of capstan rotation when the tape is started and stopped. On the shaft for the buffer levers, there are photooptical sensors that convert angular position into electric signals. These signals are fed to the inputs of the amplifiers of the current going to the reel motors.

The write circuits are on the write board. They are grouped into nine identical channels, each of which implements the functions of electronic compensation for static bias (for the NRZI method), encoding of information to be recorded, amplification of current going to the record head coil, and creation of current in the erase head. The read circuits are on three boards containing nine identical channels; each channel consists of a read head signal amplifier, a filter-amplifier and differentiating circuits, as well as circuits to detect and limit read signals and bias compensation circuits.

The read-write head allows reproduction of information recorded at a given moment for monitoring. Read and write control functions are handled by circuits on a separate board. Also on this board are the line transmitter and receiver circuits, circuits for control and matching with electrical parameters of the cable, and circuits for pulse shaping and regulation of static and dynamic biases during reading by the NRZI method. Control of the operation of the drive circuits and control of

the motion of the individual operations are provided by the circuits on the automatics board which contains: the unit of push-buttons that initiate tape movement operations at the rated speed, and tape loading and unloading; circuits for indication of the status of operation of the storage unit; status signal generation circuits; circuits for tape drive control as a function of commands received from the control unit and status of the sensors.

The BOT/EOT [beginning/end of tape] sensor is photooptical; it detects the reflecting markers for the beginning and end of the tape; the EOT and BOT signals block tape movement and are sent to the control unit.



SM-5304 magnetic tape storage unit.

The electrical and mechanical parameters for the SM-5304 magnetic tape storage unit are:

tape width, mm	12.7 (0.5 inch)
tape thickness, micrometers	40
reel diameter, mm	267 (10.5 inches)
rated tape tension, g	226
tape operating speed, m/s	0.635 (25 ips) ±2%
tape rewind speed, m/s	4.4 (175 ips) ±4%
write biases (maximum bias tolerated between two bits during write), micrometers	3.81
read biases (maximum delay tolerated between two bits when reading from a reference tape of biases), micrometers	6.5
start time, ms	12 ±1
stop time, ms	12 ±1
start-stop section, mm	4.8 ±0.5
recording method	NRZI [as published] or PE (in accordance with ISO)
BOT and EOT sensors (space between marker sensors and heads is about 70 mm)	photoelectrical
weight, kg	54
dimensions, mm:	
height	609 (24 inches)
width	483 (19 inches)
overall length	419
length to front panel	470

operating temperature (if tape parameters permit), °C	+5 to +40
shipping temperature, °C	-40 to +55
operating altitude permissible	6000 m above sea level
maximum wattage, W	500
operating voltage, V	105, 115, 125, 210, 220, 230, 240, 250

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CSO: 1863/157

NEW HARDWARE FOR THE SYSTEM OF SMALL COMPUTERS

Moscow VYCHISLITEL'NAYA TEKHNIKA SOTSIALISTICHESKIKH STRAN in Russian No 8, 1980 (signed to press 17 Nov 80) pp 144-154

[Article compiled by V. M. Zenin, candidate of engineering science, USSR, and Yu. A. Lavrenyuk, engineer, USSR, from book "Computer Technology of the Socialist Countries", a collection of articles, edited by M. Ye. Rakovskiy, Izdatel'stvo "Statistika", 16,000 copies, 168 pages]

[Text] Units Developed in the CSSR

The SM-2001 programmable timer is designed to readout prescribed time intervals, shape series of pulses used in other units and monitor the serviceability of the SM-3 and SM-4 computer complexes. In design the timer is made in one unit of elements.

Main characteristics of the timer:

precision of time interval (determined by crystal oscillator), %	±0.01
clock pulse generation	100 kHz, 10 kHz, 50 Hz
interface	common bus
dimensions, mm	280 x 240 x 14
weight, kg	no more than 0.45

The SM-2301 processor is intended for use in SM-3 control computer complexes. The general view of the processor is shown in fig. 1 [see below]. The processor is an autonomous complete unit that may be installed in a desk (instrument version) or cabinet.

Main characteristics of the processor:

type	parallel
word size	16
control principle	microprogram
execution time for register-register type of operations, microseconds	3.3
number of general-purpose registers	8
maximum addressable size of memory (16-bit words)	28K
interrupt system	multilevel
interface	common bus
weight, kg	not more than 40

The SM-3510 semiconductor memory module is used to receive, store and output binary information in the SM-3 and SM-4 computer complexes. The module is made in the form of a unit of elements.

Main characteristics of the unit:

word size, bits	16 (plus two check bits)
size, words	16K
cycle time, microseconds	0.7
fetch time, microseconds	0.55
dimensions, mm	425 x 240 x 11
weight, kg	no more than 0.5

The SM-6001 general-purpose controller with outlet for the IRPR (interface radial with parallel transmission of information) is designed to connect peripherals with an outlet for the small interface of the SM EVM IRPR to the SM-3 and SM-4 computer complexes. The SM-6001 controller supports connection of a perforated tape unit with keyboard or display with keyboard to the SM-3 and SM-4 complexes. The controller is made in the form of one unit of elements.

Main characteristics of the controller:

interface on the processor side	common bus
interface on the peripheral side	IRPR
number of individual channels	one input channel, one output channel
number of data bits sent in parallel	8
maximum distance from peripheral to controller, m	15
dimensions, mm	280 x 240 x 14
weight, kg	no more than 0.4

The SM-6002 general-purpose controller with outlet for the IRPS and the S2 is used to connect peripherals and terminals with an outlet for the "styk 2" (S2) interface or the small interface SM EVM IRPS (interface radial with serial transmission of information) to the SM-3 and SM-4 computer complexes. The peripherals and terminals may be alphanumeric printers and displays with or without keyboards. Remote terminals are connected through modems and communications lines. The controller is made in the form of one unit.

Main characteristics of the controller:

interface on the processor side	common bus
interface on the peripheral side	IRPS, S2
number of individual channels	one input channel, one output channel
number of data bits	5, 6, 7 and 8 (set by the connectors)
number of stop bits (standardized time interval corresponding to one sending of signals)	1; 1.5 or 2 (set by connectors)
maximum distance from peripheral to controller with direct connection, m	up to 500
dimensions, mm	280 x 240 x 14
weight, kg	no more than 0.5

The SM-6208 perforated tape input unit is intended for reading information from perforated tape and inputting it into computer complex units. The SM-6208 is an autonomous complete unit, insertable into a cabinet. The general view of the unit is shown in fig. 2 [see below].

Main characteristics of the unit:

operating mode	start-stop, continuous
maximum read rate in start-stop mode, rows/second	100
maximum read rate in continuous mode, rows/second	300
number of tracks on perforated tape	8
dimensions, mm	482.5 x 714 x 221.5
weight, kg	no more than 30

The SM-7108 alphanumeric matrix printer with keyboard (fig. 3) [see below] is used to input and output alphanumeric data. The unit includes the "Konsul 211.I" matrix printer, the "Konsul 259.II" solid-state keyboard, a control unit, power supply and table.

Main characteristics of the unit:

printing rate in start-stop mode, cps	80
number of characters per line	up to 132
number of characters in the set	up to 96
number of copies printed	up to 3
dimensions, mm	1000 x 960 x 800
weight, kg	no more than 130

The SM-7202 alphanumeric video terminal is designed to input/output alphanumeric data in computer complexes. In the off-line mode, the unit allows editing, modifying and correcting data files before putting them into a computer. The general view of the video terminal is shown in fig. 4 [see below].

Main characteristics of the video terminal:

screen size, mm	200 x 140
number of characters on the screen	up to 1920
number of lines	24
number of characters in a line	80
number of characters in the set	96
dimensions, mm	800 x 480 x 350
weight, kg	no more than 40

The SM-8501 remote communications (asynchronous) adapter is used to send data between a processor and peripherals having an outlet for interface S2 or the IRPS. The adapter is an autonomous complete unit, insertable in a cabinet. The unit holds up to eight separate controllers with an outlet for the S2 or IRPS. The general view of the unit is shown in fig. 5 [see below].

Main characteristics of the unit:

interface on the processor side	common bus
interface on the peripheral side	IRPS, S2
number of individual channels	from 1 to 8
data transmission rate, baud	selectable, 50, 100, 200, 300, 600, 1200, 2400, 4800, 9600
data transmission mode	simplex, half-duplex, duplex
method of operation	asynchronous (start-stop)
number of data bits	5, 6, 7 or 8
number of stop bits	1, 1.5 or 2
dimensions, mm	714 x 482.5 x 221.5
weight, kg	no more than 45

Units Developed in the Hungarian People's republic

The MF 3200 (SM-5601) floppy disk storage unit (includes power supply and control unit) is designed to operate within external storage units and input/output units in the system of small computers, systems for data preparation and acquisition, as well as terminal stations. Design of the control unit depends on the features of the units in which it is used. The general view of the storage unit is shown in fig. 6 [see below].

Main characteristics of the unit:

capacity, Mbits	3
data transfer rate, kbits/s	250
movement of magnetic head, ms:	
step time from track to track	10
head transient period	25
head latch period	40
dimensions, mm	134 x 217 x 375
weight, kg	8

The VT 42111 (SM-6101) card reader. General view of the unit is shown in fig. 7 [see below]. The unit uses standard 80-column cards carrying data in accordance with standard MS 6135, GOST 6198-75 and ISO 1681.

Main characteristics of the unit:

throughput rate, cards/min	600
capacity of feed hopper, cards	600 cards with the capability of additional loading
capacity of card stacker, cards	640
approximate dimensions, mm	335 x 640 x 330
weight, kg	no more than 32

The VT 25120 (SM-6306) alphanumeric printer is a parallel printer. It can be connected to any digital data porcessing system, and in the off-line mode--to perforated tape or card input units, to a magnetic tape storage unit or to remote user consoles. The general view of the unit is shown in fig. 8 [see below].

Main characteristics of the unit:

printing rate, lines/min	900
character set	96
characters per line	up to 132
number of copies printed	up to 6
dimensions, mm	1168 x 1232 x 622
weight, kg	up to 260

The 47607 (SM-7301) point graphic video terminal is designed for input/output of alphanumeric and graphic information in computer complexes; it allows establishing rapid and convenient communication with a computer both when connected directly and through data transmission lines. There may be displayed on the screen jointly or independently: two single-valued graphs or histograms by the raster of 512 x 236 points, a grid formed from arbitrary combinations of 236 horizontal and 512 vertical lines, any combination of 512 markers of both graphs, special graphic symbols and the set of alphanumeric characters. The general view of the video terminal is shown in fig. 9 [see below].

Main characteristics of the unit:

screen size, mm	220 x 150
number of characters on the screen	up to 1920
number of lines	24
number of characters per line	80
character set	125
raster format (points):	
horizontal	512
vertical	236
type of graphic image	two single-valued functions for the X coordinate, controlled independently (graph or histogram)
raster	composed from arbitrary set of 236 horizontal and 512 vertical lines
graphic marker	512 for each graph (1024 in all), each of which is controlled individually
dimensions, mm	500 x 530 x 340
weight without keyboard, kg	not over 25
keyboard weight, kg	no more than 8

The 47605 (SM-7401) alphanumeric programmable video terminal is used both as a peripheral with many functional capabilities and as a stand-alone microcomputer easily programmed by the user. The general view of the terminal is shown in fig. 10 [see below]. The basic peripheral is the alphanumeric display; the user can program its functional characteristics to optimally match the application. The unit has two built-in microcassette storage units that are used as external storage; with them, programs of indicators are loaded into main memory. There is also a keyboard for the operator to communicate with the unit and a central computer.

Main characteristics of the base unit:

Display	
screen size, mm	220 x 150
number of characters on screen	up to 2000
numer of lines	25
number of characters per line	80
expansion of buffer storage at user's option	4000 characters with capability of bidirectional ROLL operation
dimensions, mm	500 x 530 x 340
weight without keyboard, kg	no more than 28
keyboard weight, kg	no more than 8
Microprocessor	
instruction word format, bytes	1, 2, 3
data word format, bytes	1
number of instructions	78
instruction execution time, microseconds	1.3 to 2
size of addressable storage, Kbytes	64
Microcassette Storage (built-in)	
cassette capacity, Mbytes	100
transfer rate, bytes/second	2400
average access time, seconds	30
Operating System	
organizing program	monitors, input-output control system, logic level of control of peripherals
programming language	at the level of Assembler
service of program	conversion subroutines, management of minicassette library; editing-sorting programs
preventive maintenance programs	test programs, tracing program

Optional units include:

additional buffer storage with 2000 characters;

semiconductor main storage, size of which is expanded by 8 or 16 Kbytes;

programmable interface for printers;

programmable parallel interface;

asynchronous data transmission unit; and

line display generator.

The "Modem-200" (SM-8101) is intended for asynchronous transmission and reception of serial binary signals through dial-up or dedicated channels of the general-purpose telephone network. The general view of the SM-8101 is shown in fig. 11 [see below].

Main characteristics:

interface meets the recommendations of the MKKTT [International Telegraph and Telephone Consultative Committee=ITTCC]	V24 and V28
operating mode	duplex
transmission rate, bits/s	up to 300
dimensions, mm	188 x 398 x 100
weight, kg	no more than 5.7

The unit allows automatic call reception. A telephone can be connected to it which serves as an order wire over double lines in interruptions of data transmission.

The "Modem-1200" (SM-8102) is used for synchronous or asynchronous transmission and reception of serial binary signals through dial-up or dedicated channels of the general-purpose telephone network.

Main characteristics:

interface meets the recommendations of the ITTCC	V24
operating mode	duplex or half-duplex
transmission rate, bits/s	600, 1200
dimensions, mm	188 x 398 x 100
weight, kg	not over 5.7

The unit allows automatic call reception. A telephone can be connected to it to serve as an order wire over double lines in interruptions of data transmission.

The "Modem-2400" (SM-8103) is used for synchronous transmission and reception of serial binary signals over dial-up or dedicated lines of the general-purpose telephone network.

Main characteristics:

interface meets recommendations of ITTCC	V24 and V28
operating mode	duplex or half-duplex
transmission rate, bits/s	2400, 1200
dimensions, mm	330 x 410 x 100
weight, kg	no more than 7.6

The unit allows automatic call reception. A telephone can be connected to it to serve as an order wire over double lines in interruptions of data transmission.

The external view of the SM-8102 and the SM-8103 is similar to that of the SM-8101 [see fig. 11 below].

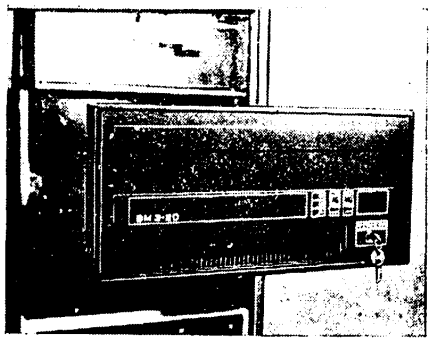

Fig. 1: SM-2301 processor

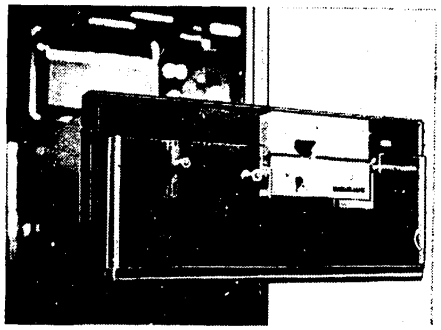

Fig. 2: SM-6208 perforated tape input unit

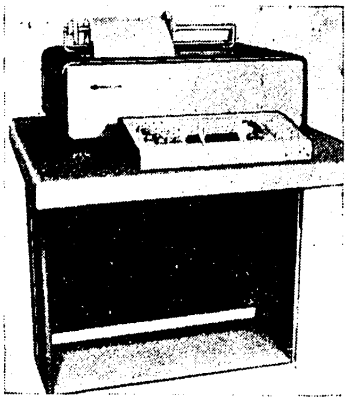

Fig. 3: SM-7108 alphanumeric matrix printer

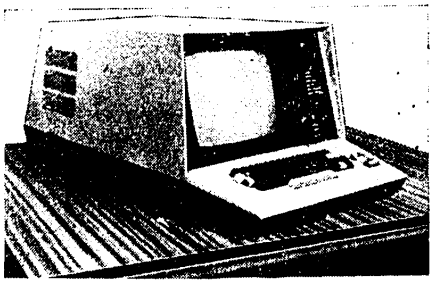

Fig. 4: SM-7202 alphanumeric video terminal

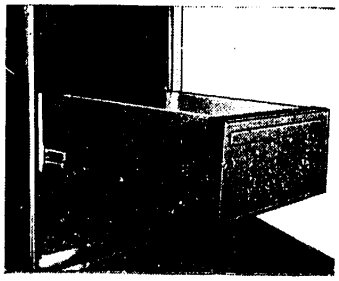

Fig. 5: SM-8501 remote communications adapter

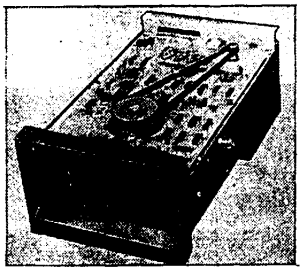

Fig. 6: SM-5601 floppy disk storage unit

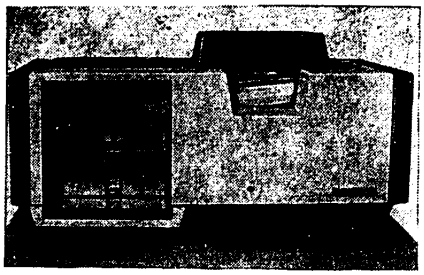

Fig. 7: SM-6101 card reader

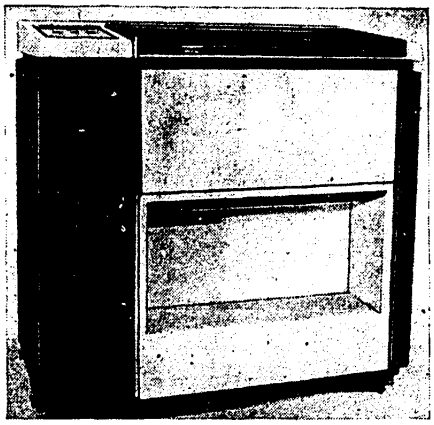

Fig. 8: SM-6306 alphanumeric printer

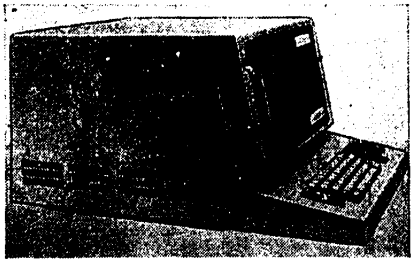

Fig. 9: SM-7301 graphic video terminal

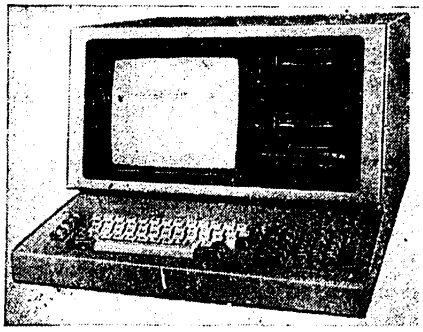

Fig. 10: SM-7401 alphanumeric video terminal

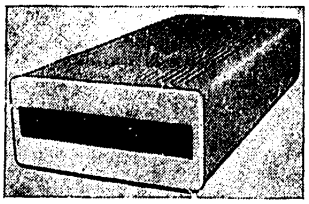

Fig. 11: "Modem-200" (SM-8101)

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END