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CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 18/81)

Excerpts from 'HANDBOOK ON INTEGRATED MICROCIRCUITS'

Ed. by

B.V. Tarabrin

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EXCERPTS FROM 'HANDBOOK ON INTEGRATED MICROCIRCUITS'

Moscow SPRAVOCHNIK PO INTEGRAL'NYM MIKROSKHEMAM in Russian 1980 (signed to press 22 Feb 80) pp 2-41, 564-816

[Annotation, table of contents, foreword to second edition, parts 1 and 5, and appendices from book "Handbook on Integrated Microcircuits," edited by B.V. Tarabrin, Izdatel'stvo "Energiya," second edition revised and enlarged, 100,000 copies, 816 pages, UDC 621.3.049.77(03)]

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[Text] This handbook presents information on digital and analog integrated microcircuits. Soviet-made integrated microcircuits are classified. Types of housings and their general characteristics and parameters are described. Detailed information is provided on each series of integrated microcircuits: the basic purpose of each series, the basic electric circuits, base design, and electric parameters. The first edition was published in 1977.

This handbook is intended for engineers and technicians involved in the development, use, and repair of electronic equipment.

Contents

Part Two
Reference Information on Digital Integrated Microcircuits

Part Three
Reference Information on Analog Integrated Microcircuits

Foreword to Second Edition

The period since the time of preparation and publication of the first edition of the "Handbook of Integrated Microcircuits" has been typified by swift introduction of integrated microcircuits into general-purpose and control computer complexes; into peripheral equipment; into the data recording and transmission devices of automatic production process control systems; into instruments and equipment intended for scientific research and mechanization of engineering and control; into medical instruments and household appliances; into agricultural and environmental control equipment, and so on.

Broad introduction of integrated microcircuits into the national economy is promoted by decisions of the 25th CPSU Congress, which determined that: "The main task of the 10th Five-Year Plan is to successively implement the Communist Party's policy of raising the material and cultural standard of living of the people on the basis of dynamic and proportionate development of social production, enhancement of its effectiveness, acceleration of scientific-technical progress, growth of labor productivity, and all-out improvement of the quality of work done in all units of the national economy."

Use of integrated microcircuits has made it possible to improve and to create new methods for planning, designing, and producing electronic equipment for various purposes, to upgrade its technical and operating characteristics, and to introduce electronics into a number of devices traditionally designed on the basis of mechanical or electromechanical principles of operation.

But at the same time, the practical experience of the handbook's authors provides the grounds for asserting that mistakes are sometimes made in selecting the nomenclature of integrated microcircuits when designing and producing electronic apparatus: The conditions of their application are violated; a number of requirements concerning links between integrated microcircuits are not accounted for, resulting in unstable operation of the electronic equipment.

One of the causes behind these mistakes is an insufficient knowledge of the parameters and operating features of integrated microcircuits on the part of electronic equipment developers and manufacturers.

As with the first, the second edition has the goal of acquainting the reader with integrated microcircuits that have enjoyed the greatest application in different types and classes of electronic equipment (rather than the entire nomenclature of industrially produced microcircuits), and to provide the reader with a minimum amount of information on parameter measurements, assembly, and design of electronic subassemblies, and so on.

This handbook is not a replacement for official documents (operational certificates, specifications, instructions for use), but it does allow the user to review the great assortment of integrated microcircuits being produced by Soviet industry, their parameters, and their operating conditions, to compare them with the requirements imposed on the equipment, and to correctly select both series-produced and custom-made microcircuits.

The microcircuit nomenclature of this edition of the handbook is significantly different from that of the first edition (1977). In particular the composition of series TTL and KMOP microcircuits, series-produced operational amplifiers, and backup electric power supplies have been significantly supplemented as offering major promise today; microcircuits exhibiting high resistance to interference and series-produced superhigh-speed microcircuits employing emitter-linked logical circuits have been included. Concurrently a number of series-produced microcircuits enjoying limited use today were dropped from the handbook.

The section describing the applications of different classes of microcircuits (TTL, KMOP, ESL, VPL) was expanded, and a reference table of correspondence between old and new identification codes is provided.

The authors feel that separate editions will have to be published in order to provide fuller information on this subject, including the behavior of integrated circuits in response to changes in temperature and load.

The materials presented in this handbook are based on a generalization of experience in using microcircuits, and on a study of their properties and parameters.

The authors hope that this handbook will be useful to engineers and technicians developing and using electronic equipment based on integrated microcircuits.

The authors request that all comments and suggestions for improvement of the handbook be sent to the following address: 113114, Moscow, M-114, Shlyuzovaya nab., 10, izdatel'stvo "Energiya".

Part One. General Information on Integrated Microcircuits

1-1. Terminology

Microelectronics is the field of electronics encompassing the problems of the investigation, design, manufacture and application of microelectronic products.

A microelectronic product is an electronic device with a high degree of integration.

An integrated microcircuit (microcircuit, IC) is an electronic product which performs a defined function of signal conversion and processing and has high packing density of electrically connected elements (or elements and components) and (or) crystals, which is considered as a unit whole from the point of view of test, acceptance, delivery and operating requirements.

An integrated circuit element is a part of a microcircuit which performs the function of any electronic element and which is executed inseparably from the crystal or substrate and cannot be isolated as an independent element from the point of view of the test, acceptance, delivery and operating requirements (electronic elements include transistors, diodes, resistors, capacitors, and so on).

An integrated circuit component is a part of a microcircuit performing the functions of any electronic element which can be isolated as an independent product from the point of view of test, acceptance, delivery and operating requirements.

A semiconductor integrated microcircuit is a microcircuit, all the elements and interelement connections of which are executed within and on the surface of a semiconductor.

A film integrated microcircuit (film microcircuit) is a microcircuit all the elements and interelement connections of which are in the form of films (the versions of film microcircuits include thick-film and thin-film microcircuits).

A hybrid integrated microcircuit (hybrid microcircuit) is a microcircuit that, in addition to the elements, contains components and (or) crystals (the versions of microcircuits include multicrystalline IC).

An integrated microcircuit crystal is a part of a semiconductor plate within and on the surface of which the elements of a semiconductor microcircuit, interelement connections and terminal areas are formed.

An analog integrated microcircuit is a microcircuit designed for the conversion and processing of signals that vary according to a continuous function law [a special case of an analog IC is a microcircuit with linear characteristic (a linear microcircuit)].

A digital integrated microcircuit is a microcircuit designed for the conversion and processing of signals that vary according to a discrete function law (one of the forms of a digital microcircuit is a logical IC).

The case of an integrated microcircuit is the structural part of the microcircuit designed to protect it from external effects and for connection with external electric circuits by terminals.

The scale of integration of an integrated microcircuit is the index of the degree of complexity of the microcircuit characterized by the number of elements and components contained in it.

The scale of integration of a microcircuit is defined by the formula $K = \lg N$, where K is a coefficient defining the scale of integration rounded to the nearest higher whole number; N is the number of elements and components entering into the microcircuit.

A series of integrated microcircuits is a set of types of microcircuits which can perform different functions, have a unified structural engineering execution and are designed for joint application.

1-2. Structural Engineering Types of Integrated Microcircuits

Technology

Modern microelectronics is developing predominantly along two basic structural engineering lines--creation of semiconductor integrated microcircuits and creation of hybrid integrated microcircuits.

Semiconductor Microcircuits. The production of these microcircuits is based on a planar process permitting simultaneous manufacture of a large number of IC on a single plate of semiconductor material. This process involves:

planar technology making use of semiconductor material, with elements isolated by p-n spacing junctions;

planar technology making use of semiconductor material, with elements isolated by a layer of silicon dioxide;

planar-epitaxial technology, with components isolated by p-n spacing junctions;

combined circuit technology, where the active elements (transistors, diodes) are created in semiconductor material by planar technology, and passive elements (capacitors, resistors) are created on the surface of the semiconductor material by the methods of thin-film technology.

Each of these production methods has its advantages for specific semiconductor microcircuits, but planar-epitaxial technology is the most widespread today.

Hybrid Integrated Microcircuits. These microcircuits are made primarily by two basic technological processes:

thick film production by silk screen printing;

thin film production by thermal vacuum deposition, and so on.

Integrated microcircuits manufactured by silk screen printing have come to be called thick-film circuits, while those manufactured by the methods of vacuum deposition, ion-plasma spraying, reactive sputtering, and so on are referred to as thin-film integrated microcircuits.

The applications of semiconductor and hybrid integrated microcircuits have shown that they do not compete, but mutually complement one another.

Types of Cases

According to GOST [All-Union State Standard] 17467-72, integrated microcircuit cases are divided into four types (Table 1-1).

Table 1-1

Type	Shape of Case Base	Location of Case Terminals Relative to Base
1	Rectangular	On base and perpendicular to it
2	Rectangular	Off base and perpendicular to it
3	Round	On base and perpendicular to it
4	Rectangular	Parallel to plane of base but off it

Cases are classified by standard sizes on the basis of their overall dimensions and mounting dimensions; a code is assigned to each standard size, consisting of a number designating the type of case (1, 2, 3 or 4) and a double-digit number (from 01 to 99) designating the standard size.

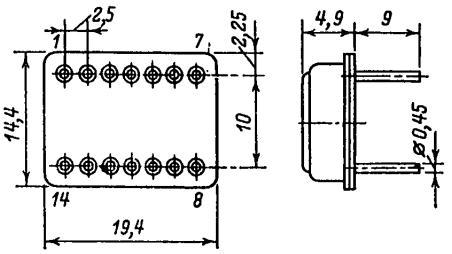
The identification code for a case design consists of the standard size code of the case, the number of terminals and the version number.

For example, a 201.14-2 case is a type-2 rectangular case, standard size 01, with 14 terminals, version 2.

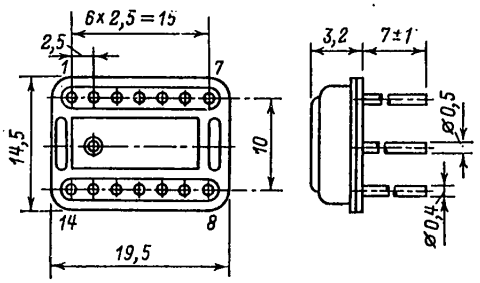
The overall and mounting dimensions are indicated on drawings (in the IC specifications, handbooks, and certificates) without regard to special elements or

devices used for additional removal of heat from the microcircuit cases, if these devices are not inseparable parts of the cases. Special elements or devices (heat transfer devices) and the means of their attachment are indicated in the technical materials accompanying specific types of microcircuits.

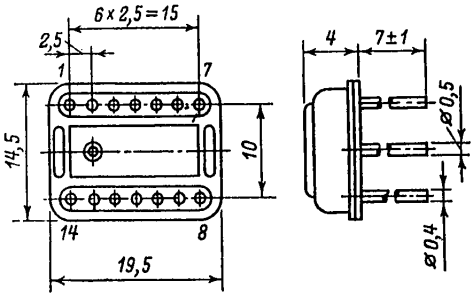
151.14-1



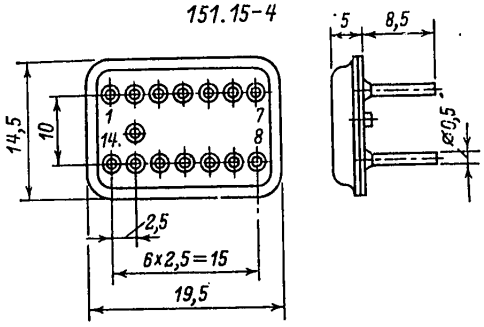
151.15-3



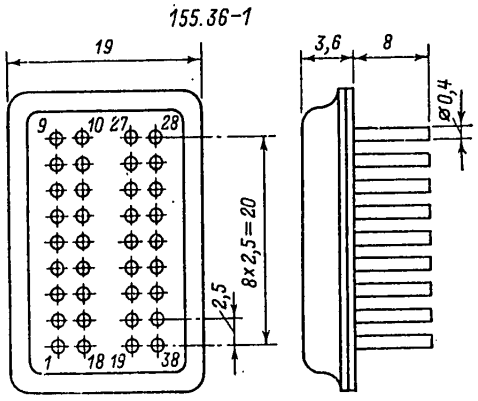
151.15-2



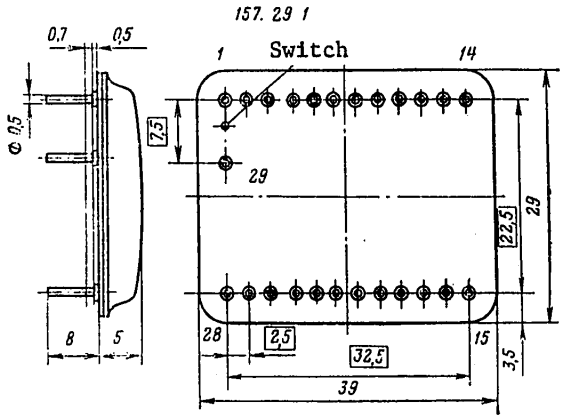
151.15-4

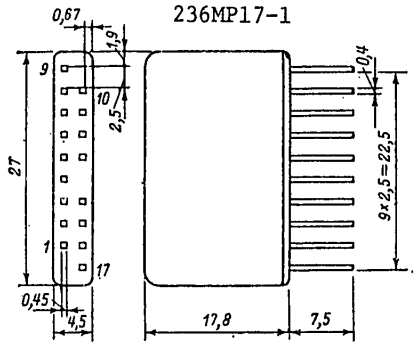


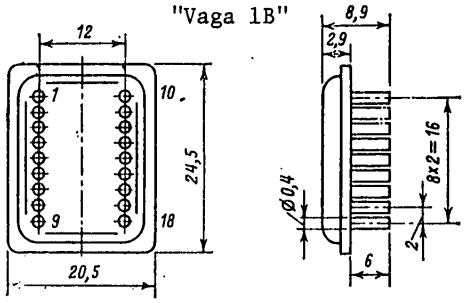
155.36-1



The following terminal spacings have been established for microcircuit cases: For type 1 and 2 cases, 2.5 mm; type 3, at an angle of 30 or 45°; type 4, 1.25 mm.



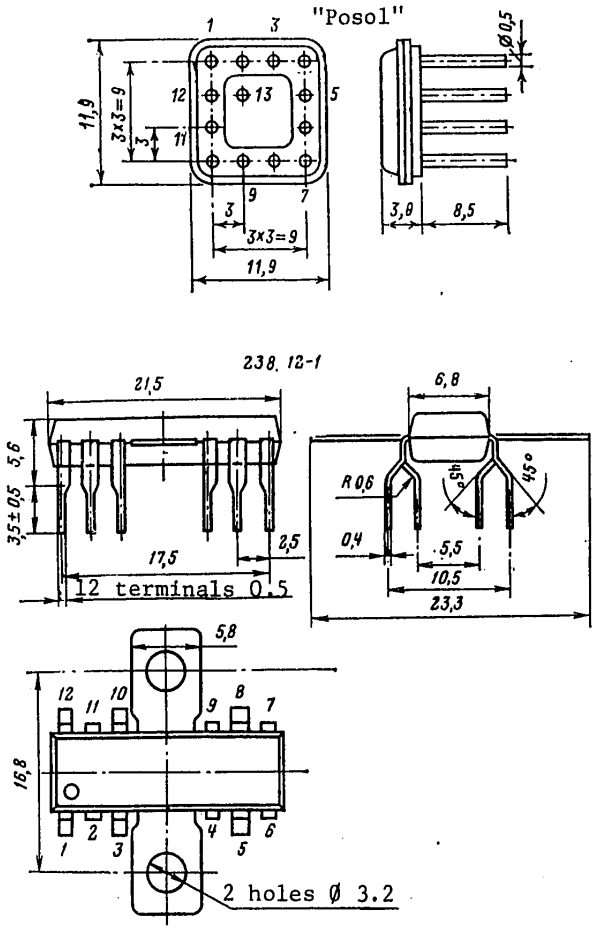




Case terminals can be round or rectangular in shape. As a rule, the diameter of round terminals is within 0.3-0.5 mm, while the dimensions of terminals having rectangular cross section lie within a circle 0.4-0.6 mm in diameter.

Integrated microcircuits of some series developed prior to introduction of the GOST mentioned above are encapsulated in nonstandard cases.

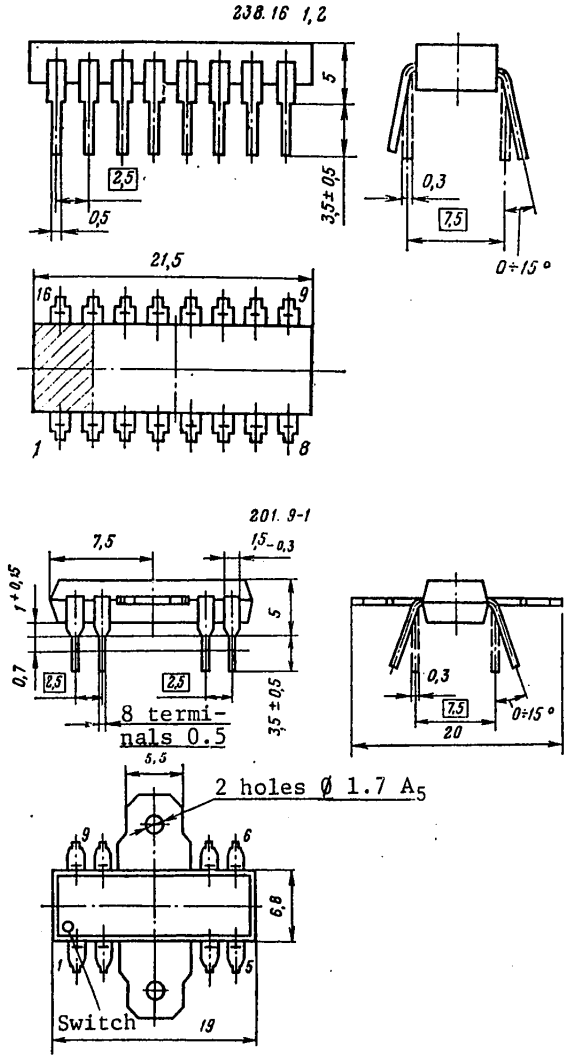
The structural designs of some types of industrially produced microcircuit cases and their overall and mounting dimensions are shown on pp 10-17.



Caseless Microcircuits. A caseless microcircuit is a semiconductor crystal with elements created within it and on its surface. The crystal is protected by a lacquer film or by a thin layer of sealing compound. Caseless microcircuits are connected to wiring boards by flexible wire terminals with a diameter of 40-50 μ, or by rigid terminals having the form of balls or posts 0.3-0.4 mm in diameter. The structural design of some caseless microcircuits are presented on p 17.

1-3. Classification of Integrated Microcircuits by Functional Purpose, and Type Designation

A GOST effective in the USSR since July 1974 applies to newly developed and modified integrated microcircuits, and it establishes their classification and provides a system of identification codes.



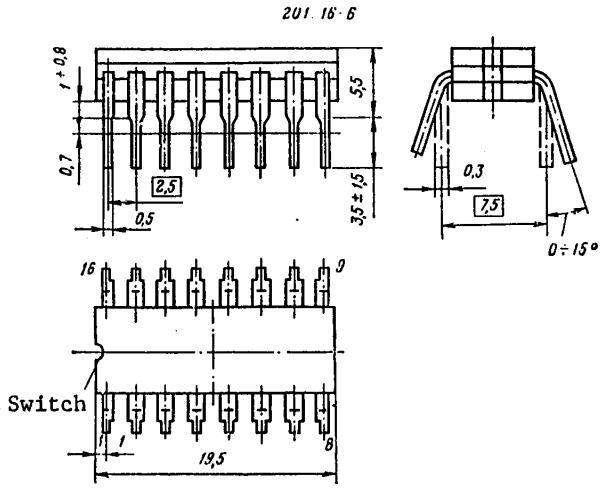
In accordance with this GOST, microcircuits are subdivided into three groups on the basis of their structural engineering design; these three groups are designated as follows:

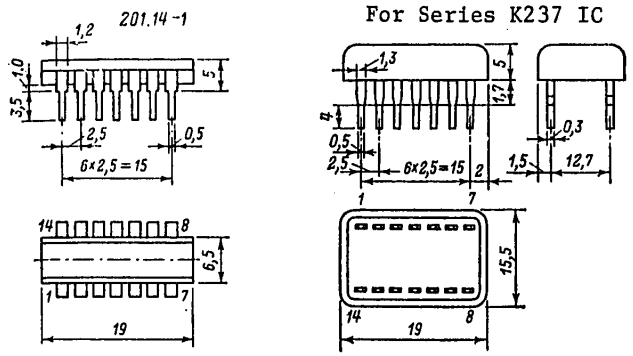
1; 5; 7--semiconductor;

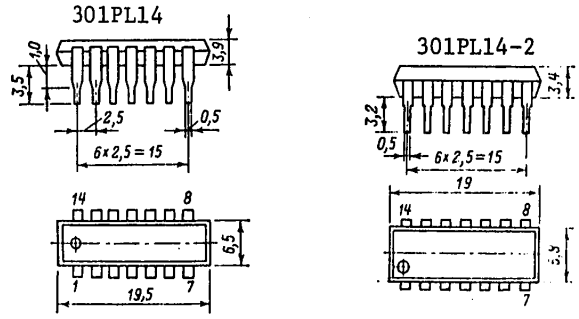
2; 4; 6; 8--hybrid;

3--other (film, vacuum, ceramic, and so on).

The identification code for the type of integrated microcircuit consists of four elements.





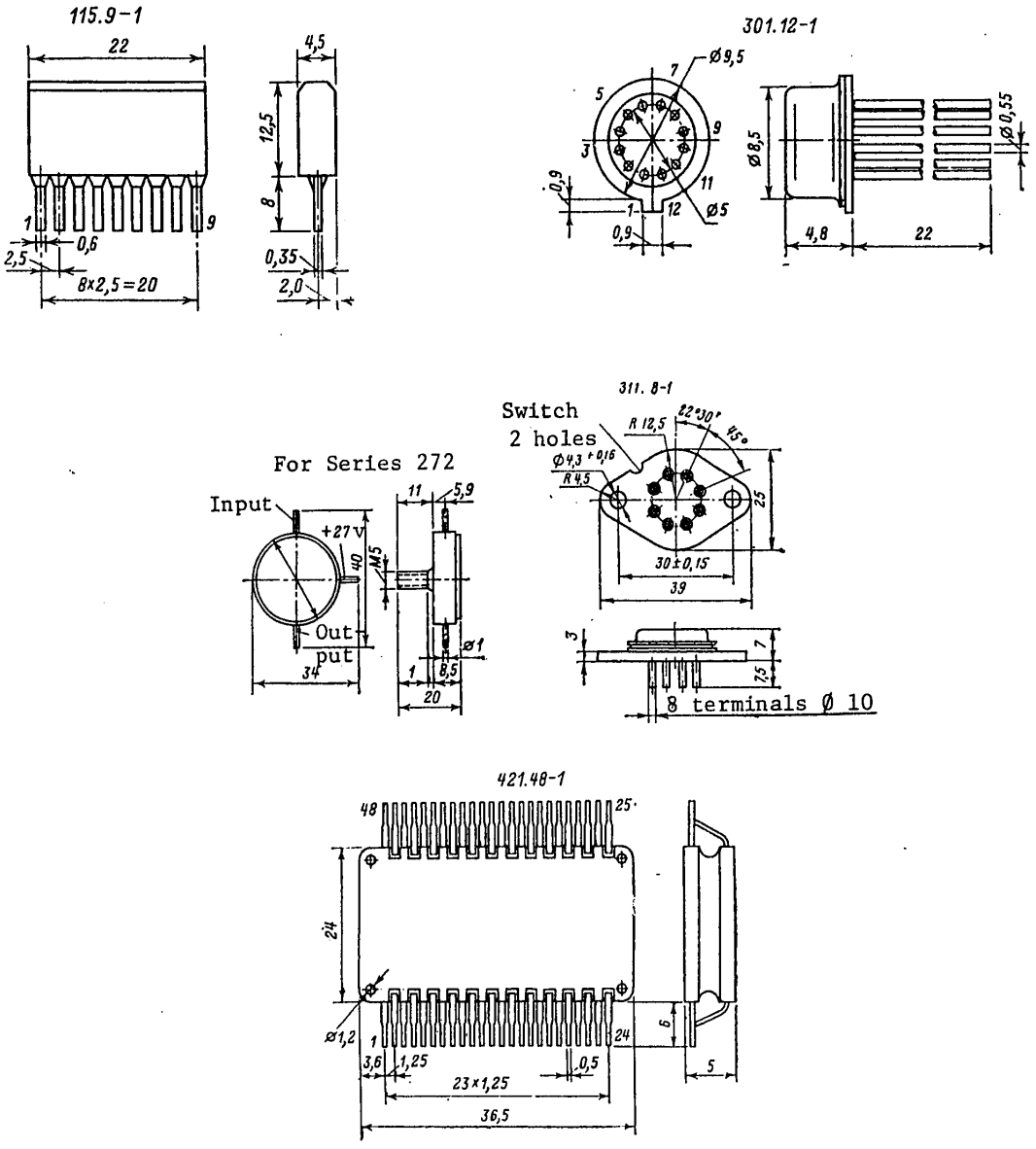


The first element--a number indicating the structural engineering design of the microcircuit (semiconductor, hybrid);

the second element--two numbers designating the serial number of the microcircuit series (from 00 to 99);

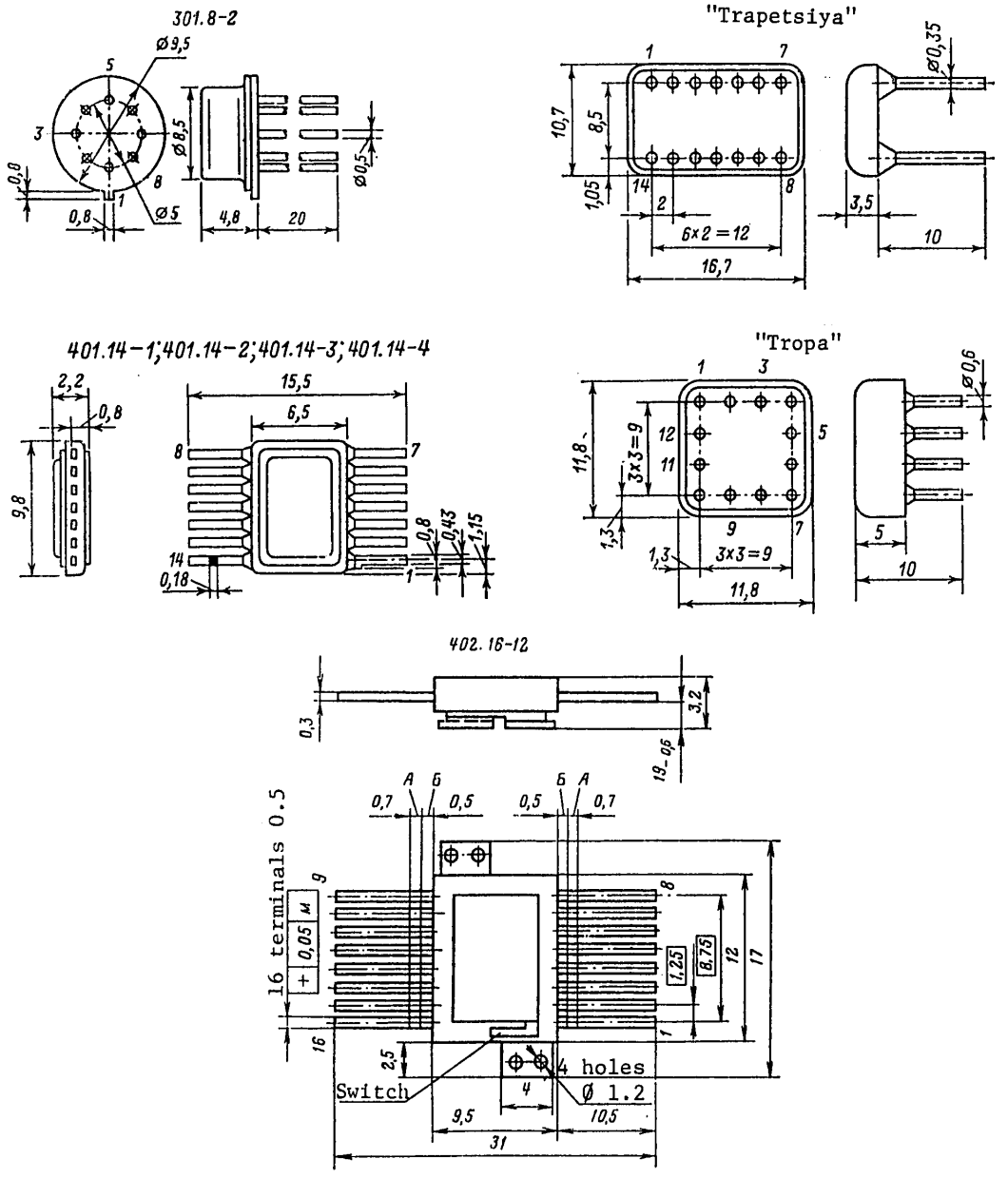
the third element--two letters designating the functional purpose of the microcircuit, in accordance with Table 1-2;

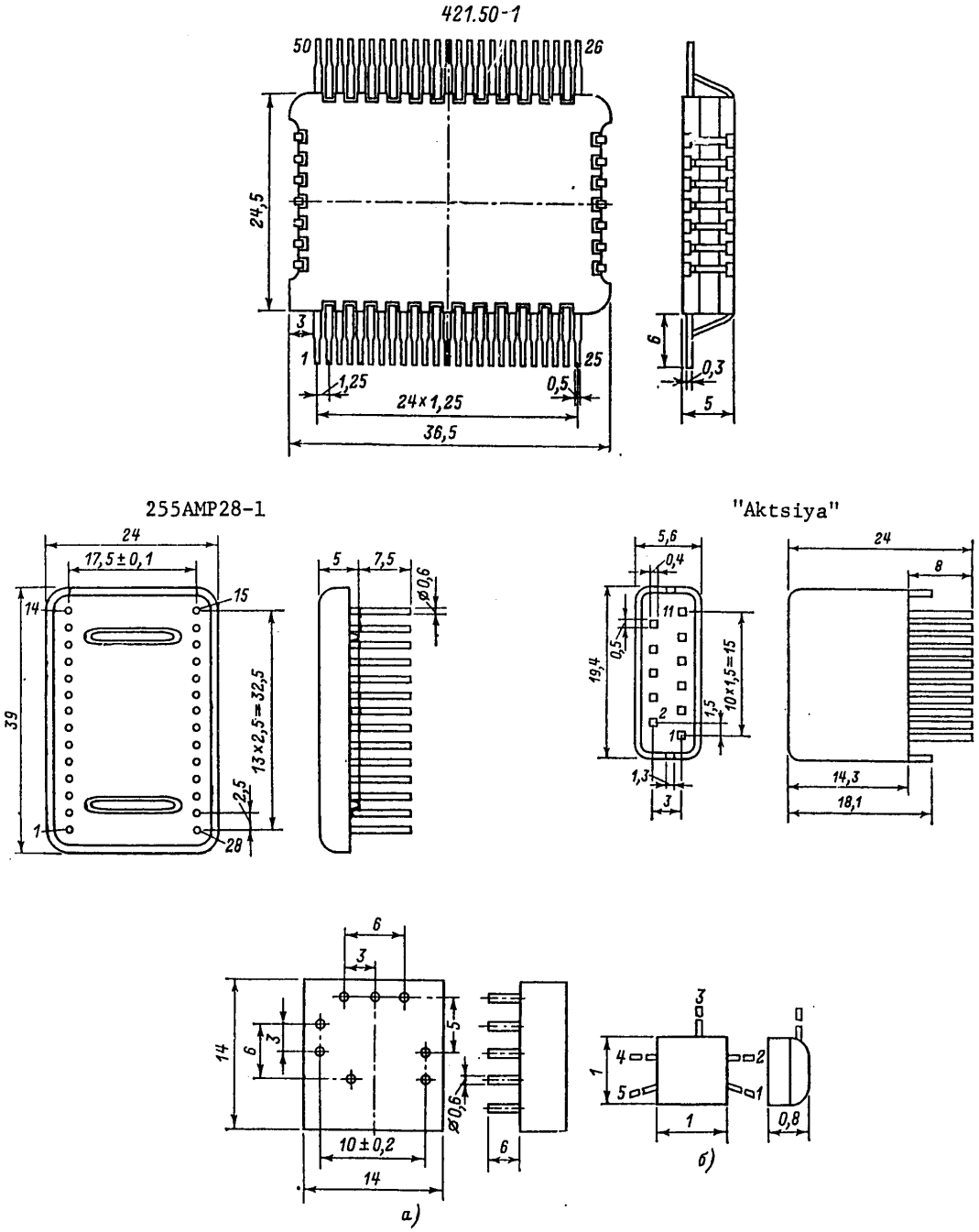
the fourth element--the serial number of the microcircuit, based on the functional characteristic in the given series.



The first two elements designate the number of the microcircuit series. The first of three numbers in the identification codes of microcircuits developed

prior to July 1974, is positioned at the beginning of the type designation, while the second and third numbers are placed after the alphabetic index. Alphabetic designations of microcircuit function are shown in Table 1-2. Alphabetic designations following the conventions in effect prior to introduction of the GOST are shown in the far right column of Table 1-2.





Rectangular case for microcircuits (a) and caseless encapsulation of microcircuits with sealing compound (b).

Many microcircuits described in this handbook were developed prior to introduction of the GOST, and their functional designations are presented in accordance with the previous conventions.

Old and new identification codes representing the same types of microcircuits can be encountered in the literature and in technical materials today. This causes some difficulty for engineers and technicians developing and operating electronic equipment employing microcircuits.

Table 1-2

Functions Performed by Integrated Microcircuits	Alphabetic Designation By GOST 18682-73	Alphabetic Designation By Convention Used Before GOST
Oscillators		
Harmonic signals	GS	GS
Square signals[1]	GG	--
Linearly variable signals	GL	--
Specially shaped signals	GF	GF
Noise	GP	--
Other		
Detectors:		
Amplitude	DA	DA
Pulse	DI	DI
Frequency	DS	DS
Phase	DF	DF
Other	DP	DP
Commutators and switches:		
Current	KT	--
Voltage	KN	--
Other	KP	KP
Transistor switch	--	KT
Diode switch	--	KD
Logical elements:		
AND-NOT element	LA	--
OR-NOT element	LYe	--
AND element	LI	LI
OR element	LL	LL
NOT element	LN	LN
AND-OR element	LS	LS
AND-NOT element, OR-NOT element	LB	LB
AND-OR-NOT element	LR	LR
AND-OR-NOT/AND-OR element	LK	LK
OR-NOT/OR element	LK	LK
Expanders	LD	LP
Other	LP	LE

Table 1-2 (continued)

Functions Performed by Integrated Microcircuits	Alphabetic Designation By GOST 18682-73	Alphabetic Designation By Convention Used Before GOST
Modulators:		
Amplitude	MA	MA
Frequency	MS	MS
Phase	MF	MF
Pulse	MI	MI
Other	MP	MP
Converters:		
Frequency	PS	PS
Phase	PF	PF
Duration	PD	--
Voltage	PN	PN
Power	PM	--
Level (matchers)	PU	PU
Signal shape	--	PM
Digital-analog	PA	PD
Analog-digital	PV	PK
Digital-digital	PR	--
Other	PP	PP
Secondary power supplies:		
Rectifiers	YeV	--
Converters	YeM	--
Voltage stabilizers	YeN	YeN, PP
Current stabilizers	YeT	YeT
Other	YeP	--
Delay circuits:		
Passive	BM	--
Active	BR	--
Other	BP	--
Selection and comparison circuits:		
Amplitude (signal level)	SA	SA
Time	SV	SV
Frequency	SS	SS
Phase	SF	SF
Other	SP	--
Triggers:		
JK type	TV	--
RS type	TR	TR
D type	TM	--
T type	TT	TS
Dynamic	TD	TD
Schmitt	TL	TSh
Combined (DT, RST and other types)	TK	TK
Other	TP	--

Table 1-2 (continued)

Functions Performed by Integrated Microcircuits	Alphabetic Designation By GOST 18682-73	Alphabetic Designation By Convention Used Before GOST
Amplifiers:		
High frequency[3]	UV	--
Intermediate frequency[3]	UR	--
Low frequency[3]	UN	--
Pulsed signals[3]	UI	UI
Repeaters	Uye	UE
Reading and playback	UL	--
Display	UM	--
Direct current[3]	UT	UT
Sinusoidal signals[4]	--	US
Videoamplifiers	--	UB
Operational and differential[3]	UD	--
Other	UP	--
Filters:		
Upper frequencies	FV	FV
Lower frequencies	FN	FN
Band	FYe	FP
Rejection	FR	FS
Other	FP	--
Shapers:		
Square pulses[5]	AG	--
Specially shaped pulses	AF	--
Address currents[6]	AA	--
Discharge currents[6]	AR	--
Other	AP	--
Memory elements		
Matrix storage elements:		
Ready access memory	RM	--
Permanent storage	RV	--
Ready access memory with control circuits	RU	--
Permanent storage (mask) with control circuits	RYe	--
Permanent storage with control circuits and with single programming	RT	--
Permanent storage with control circuits and with multiple programming	RR	--
Associative memory with control circuits	RA	--
Other	RP	--

Table 1-2 (continued)

Functions Performed by Integrated Microcircuits	Alphabetic Designation By GOST 18682-73	Alphabetic Designation By Convention Used Before GOST
Arithmetic and digital circuit elements:		
Registers	IR	IR
Adders	IM	IS
Half-adders	IL	IL
Counters	IYe	IYe
Coders	IV	ISh
Decoders	ID	ID
Combined	IK	IK
Other	IP	IP
Multifunctional IC:[2]		
Analog	KhA	ZhA
Digital	KhL	ZhL
Combined	KhK	--
Other	KhP	--
Microassemblies, sets of elements:		
Diodes	ND	ND
Transistors	NT	NT
Resistors	NR	NS
Capacitors	NYe	NYe
Combined	NK	NK
Other	NP	--

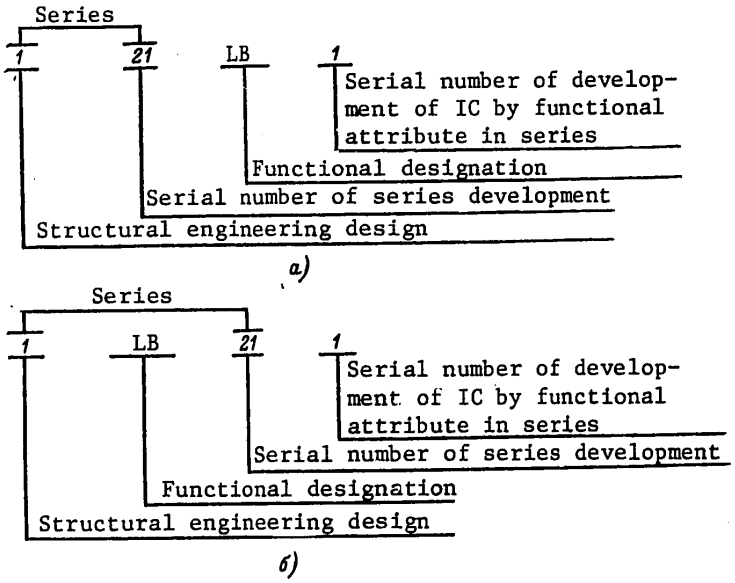
1 Auto-oscillatory multivibrators, blocking oscillators, and so on.
2 Microcircuits performing several functions simultaneously.
3 Voltage or power amplifiers (including low-noise).
4 Independently of the operating frequency range.
5 Single-shot multivibrators, blocking oscillators, and so on.
6 Voltage and current shapers.

In order to eliminate this type of difficulty a table of the correspondence between old and new identification codes for microcircuits is presented in Appendix 2.

The letters K, KM and KR at the beginning of the microcircuit code characterize their acceptance conditions by the manufacturer.

Example 1. The designation of the type of semiconductor logical circuit AND-NOT/OR-NOT with the serial number of the development of the series 21 and the number in the series by functional attribute 1 according to GOST is 121LB1. A diagram showing how to construct the identification code for this microcircuit is presented on p 22, Figure a.

Example 2. The semiconductor microcircuit AND-NOT/OR-NOT series 121 has an identification code by the revoked convention: 1LB211. The diagram for constructing the identification code for this microcircuit is presented on p 22, Figure b.



Examples of constructing the code designation for the type of microcircuit according to GOST 18682-73 (a) and the microcircuit developed before introduction of this GOST (b).

In the presence of dispersion of individual electrical parameters, the maximum operating parameters of the same type of microcircuits, an additional letter (from A to Ya) is placed at the end of the identification code. When marking the microcircuits, the final letter on their cases can be replaced by a colored dot. The specific values of the dispersion of the microcircuit parameters and the color of the marking dot are indicated in the corresponding technical materials.

1-4. Operating Conditions of Integrated Microcircuits

Integrated microcircuits maintain their parameters within the limits of the standards established by the technical specifications for specific types of IC, under the effect of various operating factors on them and after the effect of these factors.

The operating conditions of the IC, information about which is available in the present handbook, are indicated in Table 1-3.

Key to Table 1-3:

a. Series number
b. Operating temperature range, °C
c. Multiple cyclic temperature variation, °C
d. Relative humidity of the air 98 percent at a temperature of, °C
e. Atmospheric pressure, Pa
f. Vibration
g. Frequency range, Hz
h. Acceleration, g
i. Multiple impacts with acceleration, g
j. Linear load with acceleration, g
k. Single impacts with acceleration, g

Table 1-3 [÷ = to]

Номер серии	Интервал рабочих температур, °C	Многократное циклическое изменение температуры, °C	Относительная влажность воздуха 98% при температуре, °C	Атмосферное давление, Па	Вибрация (f)		Многократные удары с ускорением, g	Линейная нагрузка с ускорением, g	Одиночные удары с ускорением, g
					Диапазон частот, Гц	Ускорение, g			
(a)	(b)	(c)	(d)	(e)	(g)	(h)	(i)	(j)	(k)
101	−60 ÷ +85	−60 ÷ +85	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K101	−10 ÷ +70	−10 ÷ +70	40	—	10—600	7,5	75	25	—
K108	−45 ÷ +85	—	20	$0{,}3 \cdot 10^5 - 3 \cdot 10^5$	5—600	—	15	25	—
109	−60 ÷ +125*	−60 ÷ +125*	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K109	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
114	−60 ÷ +85	—	25	—	5—5000	40	150	150	1000
K114	−10 ÷ +70	—	20	—	5—600	5	15	25	—
115	−60 ÷ +85	−60 ÷ +85	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K115	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
K118	−10 ÷ +70	—	40	—	5—600	5	15	25	—
119	−60 ÷ +125	−60 ÷ +125	40	$1{,}3 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K119	−40 ÷ +85	−40 ÷ +85	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	10—600	7,5	75	25	—
K120	−45 ÷ +85	—	25	—	5—600	5	15	25	—
121	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K121	−10 ÷ +70	−10 ÷ +70	40	—	5—600	5	15	25	—
123	−60 ÷ +125	−60 ÷ +125	40	$1{,}3 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K123	−60 ÷ +85	—	40	—	5—600	5	15	25	—
124	−60 ÷ +85	−60 ÷ +85	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K124	−60 ÷ +70	−60 ÷ +70	40	—	5—600	5	15	25	—
128	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K128	−45 ÷ +85	—	20	$0{,}3 \cdot 10^5 - 3 \cdot 10^5$	5—600	5	15	25	—
129	−60 ÷ +125	−60 ÷ +125	40	$1{,}3 \cdot 10^{-4} - 3 \cdot 10^5$	5—5000	40	150	150	1000
K129	−60 ÷ +85	−60 ÷ +85	40	—	5—600	5	15	25	—
130	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K130	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
K131	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
133	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K133	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
134	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^5 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K134	−45 ÷ +85	—	20	$0{,}27 \cdot 10^5 - 3 \cdot 10^5$	5—600	5	15	25	—
136	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K136	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
K137	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
K138	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
140	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K140	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
KR140	−10 ÷ +70	—	25	—	1—600	10	75	25	—
K141	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
K142	−45 ÷ +85	—	25	—	1—600	10	75	25	—

Table 1-3 (continued)

Номер серии	Интервал рабочих температур, °С	Многократное циклическое изменение температуры, °С	Относительная влажность воздуха 98% при температуре, °С	Атмосферное давление, Па	Вибрация (f)		Многократные удары с ускорением, g	Линейная нагрузка с ускорением, g	Одиночные удары с ускорением, g
					Диапазон частот, Гц	Ускорение, g			
(a)	(b)	(c)	(d)	(e)	(g)	(h)	(i)	(j)	(k)
К144	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
К148	−45 ÷ +75**	—	25	—	1—600	10	75	25	—
149	−60 ÷ +125	−60 ÷ +125	40	$3 \cdot 10^{-4} - 3 \cdot 10^5$	5—5000	40	150	150	1000
К149	−45 ÷ +85	−45 ÷ +85	20	$0{,}27 \cdot 10^2 - 3 \cdot 10^5$	5—600	5	15	25	—
153	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К153	−45 ÷ +85***	—	20	—	5—600	5	15	25	—
155	−10 ÷ +70	−10 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—2000	10	35	50	150
К155	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
КМ155	−45 ÷ +85	—	20	—	1—2000	10	75	50	150
156	−60 ÷ +125	—	40	—	5—5000	40	150	150	1000
К158	−10 ÷ +70	−10 — +70	20	—	5—600	5	15	25	—
159	−60 ÷ +125	—	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К159	−60 ÷ +100	—	20	—	1—600	10	75	25	—
162	−60 ÷ +85	—	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К162	−10 ÷ +70	—	20	—	5—600	5	15	25	—
К166	−45 ÷ +70	—	20	$0{,}2 \cdot 10^2 - 3 \cdot 10^5$	5—600	5	15	25	—
К167	−45 ÷ +70	—	20	—	5—600	7,5	75	25	—
168	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—3000	15	75	150	500
К170	−10 ÷ +70	—	25	—	1—600	10	75	25	—
К172	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
К174	−30 ÷ +55	—	40	—	1—600	10	75	25	—
175	−60 ÷ +125	−60 ÷ +125	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К176	−10 ÷ +70	−10 ÷ +70	20	—	5—600	5	15	25	—
177	−60 ÷ +125	—	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К177	−45 ÷ +85	—	40	$0{,}3 \cdot 10^5 - 3 \cdot 10^5$	5—600	5	15	25	—
178	−60 ÷ +85	−60 ÷ +85	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—3000	15	75	100	500
К178	−45 ÷ +70	−45 ÷ +70	20	—	5—600	5	15	25	—
185	−60 ÷ +85	−60 ÷ +125	40	$6{,}7 \cdot 10^5 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К187	−10 ÷ +70	—	40	—	5—600	5	15	25	—
188	−60 ÷ +85	−60 ÷ +85	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
190	−60 ÷ +85	−60 ÷ +85	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К190	−45 ÷ +85	−45 ÷ +85	40	—	5—600	5	15	25	—
198	−60 ÷ +125	—	40	$1{,}3 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К198	−45 ÷ +85	—	40	—	1—600	10	75	25	—
201	−60 ÷ +70	—	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К201	+ 1 ÷ +50	—	20	—	5—600	5	15	25	—
202	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
204	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К204	−25 ÷ +55	—	25	—	1—600	10	75	25	—
205	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
210	−10 ÷ +70	−10 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—1000	7,5	75	50	5000
К210	−10 ÷ +70	—	40	—	1—600	7,5	75	25	—
211	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	75	150	150
215	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
217	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К217	−20 ÷ +70	—	20	—	5—600	5	15	25	—
218	−60 ÷ +70	—	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К218	−45 ÷ +75	—	40	—	1—600	10	15	25	—
219	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	300	1000
221	−60 ÷ +70	−60 ÷ +70	40	—	5—5000	40	150	150	1000
223	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—2000	10	35	50	150
К223	−60 ÷ +70	—	20	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—600	5	15	—	25
К224	−30 ÷ +50	—	25	—	1—600	5	15	25	—
226	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—3000	15	75	100	150
К226	−45 ÷ +55	—	25	—	1—600	10	75	25	—
228	−60 ÷ +70	—	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
К228	−45 ÷ +70	—	25	—	1—600	10	15	25	—

Table 1-3 (continued)

Номер серии	Интервал рабочих температур, °C	Многократное циклическое изменение температуры, °C	Относительная влажность воздуха 98% при температуре, °C	Атмосферное давление, Па	Вибрация (f)		Многократные удары с ускорением, g	Линейная нагрузка с ускорением, g	Одиночные удары с ускорением, g
					Диапазон частот, Гц	Ускорение, g			
(a)	(b)	(c)	(d)	(e)	(g)	(h)	(i)	(j)	(k)
229	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	15	75	100	500
K229	−45 ÷ +55	−45 ÷ +55	25	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	1—600	10	75	25	—
230	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—3000	15	75	100	500
K230	−10 ÷ +70	−10 ÷ +70	25	—	1—600	10	75	25	—
231	−60 ÷ +85	—	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
235	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—3000	15	75	100	500
K237	−30 ÷ +70	—	40	—	5—600	5	10	15	—
239	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—3000	15	35	50	150
243	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K243	+1 ÷ +50	+1 ÷ +50	20	—	5—600	5	15	25	—
K252	−45 ÷ +55	—	25	—	1—600	10	75	25	—
263	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K264	−10 ÷ +55	—	40	—	5—80	5	15	10	—
265	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K265	−60 ÷ +70	−60 ÷ +70	20	—	1—600	10	75	25	—
272	−60 ÷ +125	—	30	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K272	−45 ÷ +85	—	20	—	5—600	15	—	25	—
284	−60 ÷ +70	−60 ÷ +70	40	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K284	−45 ÷ +55	—	25	—	1—600	10	75	25	—
301	−60 ÷ +85	−60 ÷ +85	30	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—3000	15	75	100	500
K500	−10 ÷ +75****	—	25	—	1—600	10	75	25	—
504	−45 ÷ +125	—	30	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	5—5000	40	150	150	1000
K504	−45 ÷ +85	—	40	—	1—600	10	75	25	—
K511	−10 ÷ +70	—	25	$6{,}7 \cdot 10^2 - 3 \cdot 10^5$	1—600	10	75	25	—

* For the 1LI091 integrated microcircuits the operating temperature range is from -60 to +85° C.

** For the K148UN2 integrated microcircuits the operating temperature range is from -25 to +55° C.

*** For the K1UT531B integrated microcircuits the operating temperature range is from -10 to +85° C.

**** The relative humidity of the air for the integrated microcircuits K500LS18, K500LS18A, K500LS19, K500LS19A, K500ID61, K500ID61A, K500ID62, K500ID62A, K500ID64, K500ID64A is 98 percent at t = 35° C.

The general technical specifications establish a minimum service life of the microcircuits of less than 10,000 or 15,000 hours, and under light conditions, 25,000 hours. The magnitude of the minimum service life of specific types of microcircuits under the corresponding conditions is guaranteed in the technical specifications for the delivery of these types of microcircuits.

The microcircuits can be stored no less than 6 or 15 years in the manufacturer's packing, built into equipment or in a ZIP [spare parts, tools and accessories kit]. The storage life and conditions are established in the technical specifications for delivery of specific types of microcircuits.

Caseless microcircuits in unsealed or nonmoistureproofed packaging can be kept no more than 30 days under production conditions with humidity of no more than

65 percent and at normal temperature, and in the field or moistureproof manufacturer's packaging, the IC can be kept no more than 2 years under warehouse conditions.

The caseless IC installed in sealed packaging (the cases of modules, subassemblies or equipment blocks, and so on) permit storage for the same length of time as the IC in cases. In all cases the storage life of the IC is reckoned from the month in which they were manufactured (in accordance with the marking on the case or certificate of the microcircuit).

1-5. Electrical Parameters of Integrated Microcircuits

A list of the electrical parameters of integrated microcircuits, their letter designations and definitions established by GOST 19480-74 "Integrated Microcircuits. Electrical Parameters. Terms, Definitions and Alphabetic Designations," GOST 18683-73 "Integrated Logical Microcircuits. Methods of Measuring Electrical Parameters," GOST 19799-74 "Integrated Analog Microcircuits. Methods of Measuring the Electrical Parameters and Determining the Characteristics," and also a number of other electrical parameters not entering into the mentioned standards but available in the handbook are presented below.

If real concept characters are contained in the literal value of the term, the definition of the parameter is not presented. Moreover, the designations and definitions of parameters which are widespread in scientific and technical literature on electronics such as the input voltage U_{inp}, output voltage U_{out}, pulse duration t_i, and so on are not included in the list.

Parameters Having the Dimensionality of Voltage

Maximum input voltage $U_{inp\ max}$--the largest value of the input voltage of an integrated microcircuit for which the output voltage corresponds to the given value.

Minimum input voltage $U_{inp\ min}$--least value of the input voltage of a microcircuit for which the output voltage corresponds to the given value.

Sensitivity S--least value of the input voltage for which the electrical parameters of the microcircuit correspond to the given values.

Input voltage range ΔU_{inp}--the range of voltages from the minimum input voltage to maximum.

Quiescent input voltage $U_{o\ inp}$--the voltage at the input of the microcircuit in the absence of an input signal.

Quiescent output voltage $U_{o\ out}$--voltage at the output of the microcircuit in the absence of an input signal.

Clipping input voltage $U_{inp\ clip}$--least input voltage of the microcircuit for which clipping of the output voltage occurs.

Bias voltage U_{bias}--DC voltage at the input of the microcircuit for which the output voltage is equal to zero.

Cophasal input voltages $U_{coph\ inp}$--value of the voltages between each of the inputs of the microcircuit and the common output, the amplitudes and phases of which coincide.

Noiseproofness $U_{noise\ max}$--largest value of the interference voltage at the input of the microcircuit for which no change in level of its output voltage occurs.

Static noiseproofness $U_{noise\ st}$--largest admissible static interference voltage with respect to high and low levels of the input voltage for which no change takes place in the output voltage levels of a digital integrated microcircuit.

Maximum output voltage $U_{out\ max}$--largest output voltage for which the changes in the microcircuit parameters correspond to the given values.

Minimum output voltage $U_{out\ min}$--lowest output voltage for which the variations in the microcircuit parameters correspond to the given values.

Noise voltage reduced to the input $U_{noise\ inp}$--ratio of the characteristic noise voltage at the output of the microcircuit with short-circuited input to the voltage amplification coefficient.

Residual voltage U_{res}--voltage drop at the output of the threshold microcircuit in the open state.

Response voltage U_{resp}--least value of the DC voltage at the input of the microcircuit for which it goes from one stable state to another.

Dropout voltage U_{drop}--least DC voltage at the input of the microcircuit for which it goes from one stable state to another.

Minimum forward voltage on the junctions $U_{for\ min}$--least voltage drop on the microcircuit junctions for which the given value of its electrical parameters is ensured.

Maximum return voltage $U_{ret\ max}$--largest voltage drop on the p-n junction of the microcircuit with the return current flowing through it.

Power supply voltage $U_{p\ s}$.

Residual electronic switch voltage $U_{res\ o}$--signal voltage drop on an open electronic switch.

Input voltage pulse amplitude $U_{inp\ A}$--peak value of the voltage pulses at the microcircuit input.

Maximum pulse amplitude of the input voltage $U_{inp\ A\ max}$--largest peak value of the voltage pulses at the microcircuit input for which distortion of the output voltage pulse shape does not exceed the given value.

Maximum output voltage pulse amplitude $U_{out\ A\ max}$--largest peak value of the voltage pulses at the microcircuit output for which distortion of the shape of the output voltage pulse does not exceed the given value.

Logical one voltage U^1--value of the high voltage level for "positive" logic and value of the low voltage level for "negative" logic.

Logical zero voltage U^0--value of the low voltage level for "positive" logic and value of the high voltage level for "negative" logic.

Threshold logical one voltage U^1_{thresh}--least value of the high voltage level for "positive" logic or largest value of the low voltage level for "negative" logic at the microcircuit input for which it goes from one stable state to another.

Threshold logical zero voltage U^0_{thresh}--largest value of the low voltage level for "positive" logic or least value of the high voltage level for "negative" logic at the input of the microcircuit for which it goes from one stable state to another.

Parameters Having the Dimensionality of Current

Input current difference ΔI_{inp}--difference in current flowing through the microcircuit input in the given mode.

Mean input current $I_{inp\ mean}$--arithmetic mean value of the input current flowing through the inputs of a balanced microcircuit.

Maximum output current $I_{out\ max}$--largest value of the output current for which the given microcircuit parameters are ensured.

Minimum output current $I_{out\ min}$--least value of the output current for which the given parameters of the microcircuit are ensured.

Logical one input current I^1_{inp}.

Logical zero input current I^0_{inp}.

Logical one output current I^1_{out}.

Logical zero output current I^0_{out}.

Leakage current at the input $I_{leak\ inp}$--current in the input circuit of a microcircuit for the closed state of the input and given conditions on the remaining terminals.

Leakage current at the output $I_{leak\ out}$--current in the output circuit of a microcircuit for the closed state of the output and given conditions on the remaining terminals.

Intake current I_{int}--current intake by the microcircuit from the power supplies in the given mode.

Intake current in the logical one condition I^1_{int}.

Intake current in the logical zero condition I^0_{int}.

Average intake current $I_{int\ ave}$--current equal to the half-sum of the currents required by a digital microcircuit from the power supplies in two different stable states.

Short-circuit current $I_{s\ s}$--current intake by the microcircuit with short-circuited output.

No-load current $I_{n\ l}$--current intake by an integrated microcircuit with the load switch off.

Maximum commutatable current $I_{com\ max}$--largest current flowing through the open electronic switch for which the voltage drop on the microcircuit is equal to the given value.

Maximum closed switch current $I_{closed\ max}$--current flowing through the closed electronic switch with maximum input voltage and given mode.

Parameters Having the Dimensionality of Power

Intake power P_{int}--power intake by the microcircuit from the power supplies in the given mode.

Maximum intake power $P_{int\ max}$--power intake by the microcircuit in the limiting intake mode.

Intake power in the logical one condition P^1_{int}.

Intake power in the logical zero condition P^0_{int}.

Mean intake power $P_{int\ mean}$--half-sum of the powers consumed by the digital microcircuit from the power supplies in two different stable states.

Parameters Having Predimensionality of Frequency

Lower passband frequency bound f_{low}--least frequency on which the amplification coefficient of the microcircuit decreases by 3 db from the value at the given frequency.

Upper passband frequency bound f_{up}--highest frequency on which the amplification coefficient of the microcircuit decreases by 3 db from the value at the given frequency.

Passband Δf--frequency range between the upper and lower passband frequency bounds of the microcircuit.

Central passband frequency f_{cent}--frequency equal to the half-sum of the lower and upper passband frequency bounds of the microcircuit.

Unit amplification frequency f_1--frequency on which the amplification coefficient of the integrated microcircuit is one.

Cutoff frequency of the amplitude-frequency characteristic f_{cut}--frequency of the amplitude-frequency characteristic at which the amplification coefficient of the microcircuit is 0 db.

Pulse repetition frequency of the input voltage f^*_{inp}.

Oscillation frequency f_{osc}.

Parameters Having the Dimensionality of Time

Pulse delay time t_{del}--time interval between the input and output pulse fronts of the microcircuit measured on the given voltage or frequency level.

Output voltage buildup time t_{build}--time interval during which the output voltage of the microcircuit varies from first reaching the 0.1 level to first reaching the 0.9 level of the steady-state value.

Output voltage setup time t_{set}--time interval during which the output voltage of the microcircuit varies from first reaching the 0.1 level to last reaching the 0.9 level of the steady-state value.

Transition time of the integrated microcircuit from the logical one state to the logical zero state $t^{1.0}$--time interval during which the voltage at the output of the microcircuit goes from the logical one voltage to the logical zero voltage measured on the 0.1 and 0.9 levels or on the given voltages.

Transition time of the microcircuit from the logical zero state to the logical one state $t^{0.1}$--time interval during which the voltage at the output of the microcircuit goes from the logical zero voltage to the logical one voltage measured on the 0.1 and 0.9 levels or on the given voltages.

Connect delay time $t^{1.0}_{del}$--time interval between the input and output pulses on transition of the voltage at the output of the microcircuit from the logical one voltage to the logical zero voltage measured at the 0.1 level or on the given voltages.

Disconnect delay time $t^{0.1}_{del}$--time interval between the input and output pulses on transition of the voltage at the microcircuit output from the logical zero

voltage to the logical one voltage measured on the 0.9 level or on the given voltages.

Connect signal propagation delay time $t^{1.0}_{del\ p}$--time interval between the input and output pulses for transition of the voltage at the microcircuit output from the logical one voltage to the logical zero voltage measured on the 0.5 level or for the given voltages.

Disconnect signal propagation delay time $t^{0.1}_{del\ p}$--time interval between the input and output pulses for transition of the voltage at the microcircuit output from the logical zero voltage to the logical one voltage measured on the 0.5 level or for the given voltages.

Average signal propagation delay time $t_{del\ p\ ave}$--time interval equal to the half-sum of the connect and disconnect signal propagation delay times of the digital microcircuit.

Information readout time t_{read}--time interval between the fronts of the address and read signals of the microcircuit measured on the given levels in the given mode.

Information write time t_{write}--time interval between the beginning of the address signal and the appearance of the written information at the output of the microcircuit measured on the given levels.

Recovery time after read t_{rec}--time interval between the ends of the address and read signals of the microcircuit measured on the given levels.

Relative Parameters

Voltage amplification coefficient $K_{amp\ U}$--ratio of the output voltage of the microcircuit to the input voltage.

Voltage transfer coefficient K^*_{trans}.

Power amplification coefficient $K_{amp\ p}$--ratio of the output power of the microcircuit to the input power.

Cophasal input voltage attenuation factor $K_{att\ coph}$--ratio of the voltage amplification coefficient of the microcircuit to the amplification coefficient of cophasal input voltages.

Influence coefficient of the instability of the power supplies on the input current $K_{inf\ p\ s}$--ratio of the increment of the input current of the microcircuit to the power supply voltage causing its increment. (The influence coefficients of the instability of the power supply on the difference in input currents, the bias EMF and the bias voltage are defined analogously.)

Relative dynamic range with respect to voltage $\Delta U_{dyn\ rel}$--ratio of the maximum output voltage of the microcircuit to the minimum output voltage expressed in decibels.

Relative automatic gain control range with respect to voltage $\Delta U_{AGC\ rel}$--ratio of the highest value of the voltage amplification coefficient to its least value on variation of the input voltage within given limits.

Harmonic coefficient K_{harm}--ratio of the mean square voltage of the sum of all of the signal harmonics except the first to the mean square voltage of the first harmonic.

Instability factor with respect to voltage $K_{instab\ U}$--ratio of the relative variation of the output voltage (output current) of the microcircuit to the relative variation of the input voltage causing it.

Current instability coefficient $K_{instab\ I}$--ratio of the relative variation of the output voltage (output current) of the microcircuit to the relative variation of the load current or load resistance causing it.

Coefficient of nonuniformity of the frequency-amplitude characteristic (PAC nonuniformity coefficient) $K_{non\ Af}$--ratio of the maximum value of the output voltage of the microcircuit to the minimum value in the given passband frequency range expressed in decibels.

Suppression coefficient K_{sup}--ratio of the output voltages of the microcircuit measured for different control voltages expressed in decibels.

Other Parameters

Output voltage buildup rate $v_{U\ out}$--rate of variation of the output voltage of the microcircuit under the effect of a square maximum input voltage pulse.

Steepness of the volt-ampere characteristic S_{V-A}--ratio of the output current strength to the input signal voltage causing it.[1]

Conversion steepness S_{conv}--ratio of the output current of the mixer to the input voltage causing its increment for the given heterodyne voltage.

Fan-in K_{fan-in}--number of inputs of the microcircuit through which a logical function is realized.

Fan-out $K_{fan-out}$--number of unit loads which can be simultaneously connected to the output of the microcircuit[2] (a unit load is one input of the basic logical element of a given series of integrated microcircuits).

Output grouping factor $K_{group\ out}$--number of outputs of the integrated microcircuit connected to each other for which the realization of the corresponding logical operation is ensured.

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1 The term and notation have not been established by GOST 18683-73, GOST 19480-74 and GOST 19799-74.

2 The maximum values of $K_{fan-out}$ are indicated in the tables of Part Two of this reference if not stipulated otherwise for integrated microcircuits of individual types.

Load resistance R_{load}--active resistance connected to the output of an integrated microcircuit for which the given value of the output voltage (output current) or given amplification is ensured.

Load capacitance C_{load}--maximum capacitance connected to the output of the integrated microcircuit for which the given frequency and other parameters are ensured.

Diode and transistor parameters entering into the microassemblies (sets of diodes and transistors) are designated in the handbook by symbols established for these semiconductor devices corresponding to the USSR State Standards.

Part Five. Application of Integrated Microcircuits

5-1. Recommendations for the Assembly of Integrated Microcircuits

One of the basic conditions ensuring reliable operation of electronic equipment constructed with the broad application of integrated microcircuits is observation of the rules for their assembly, soldering and wiring. The basic structural elements of the electronic equipment subassemblies and modules permitting the most complete realization of the advantages of IC are the printed circuit boards. When assembling the IC on the printed circuit boards it is necessary to observe the following requirements and specifications:

the assembly and fastening of the microcircuits to the printed circuit boards must provide for their normal operation under the operating conditions of the equipment;

the spacing from the IC cases to the bends and soldering points of their leads indicated in the instructions and manuals must be strictly maintained;

the assembly spacing of the IC on the printed circuit boards must be a multiple of 2.5, 1.5 or 0.5 mm (depending on the type of case and the structural design of the subassembly or module);

linear-multirow (or checkerboard) arrangement of the IC must be observed, ensuring the greatest density of layout and possibility of mechanized assembly of the units;

microcircuits with spacing between the terminals, that is, a multiple of 2.5 mm, must be arranged on the printed circuit board in such a way that their terminals coincide with the corners of the coordinate grid (Figure 5-1); if the spacing between the IC terminals is not a multiple of 2.5 mm, they must be arranged so that one or several of the microcircuit terminals coincide with the corners of the coordinate grid;

the installation and fastening of the microcircuits must provide for access to any of them and the possibility of their replacement;

for proper orientation of the IC on the printed circuit board, "alignment pins" must be provided which determine the position of the first terminal of each microcircuit (Figure 5-2);

the arrangement and the fastening of the IC must offer the possibility of group soldering with subsequent moisture protection;

if necessary the board with the mounted IC must be protected from climatic factors.

In addition, when arranging the IC on the printed circuit boards the following rules must be followed during the design phase:

the microcircuits must be at a distance from the elements which generate a large amount of heat during operation so as to exclude overheating of the microcircuits;

it is inadmissible to locate microcircuits in the magnetic fields of permanent magnets, transformers and chokes;

it is necessary to provide for air convection at the element radiators and elements releasing a large quantity of heat.

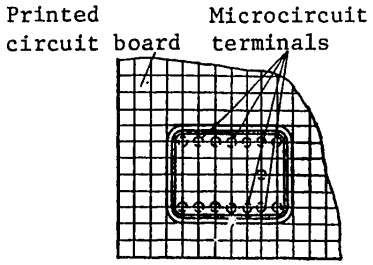


Figure 5-1. Assembly of a microcircuit on a printed circuit board.

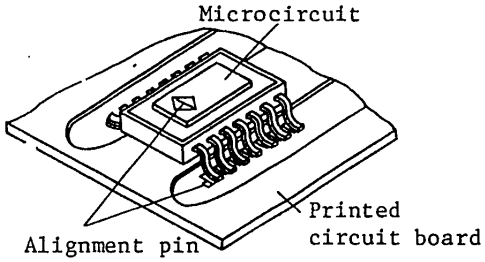


Figure 5-2. Orientation of the microcircuit on the printed circuit board.

It is necessary to take measures excluding the effect of static electricity on the IC.

Microcircuits with terminal posts in the type-1 cases must be mounted on only one side of the printed circuit without additional fastening with a clearance of

$1.0^{+0.5}$ mm between the microcircuit case and the board (Figure 5-3) or through an electrical insulating insert 1.0-1.5 mm thick with traditional fastening to the board and the entire base plane of the case to the insert using adhesive or coating with lacquer if there are no other instructions in the technical specifications for the microcircuit. The insert must be placed under the entire area of the base of the case or between the terminals in an area of no less than two-thirds of the base; the insert must prevent touching of the protruding terminal insulators. The clearance between the IC case and the board must be no less than 1.5 mm; the clearance between the IC cases must be no less than 1.6 mm; the protruding parts of the terminals must be above the surface of the board within the limits of 0.5-1 mm (if not stipulated otherwise in the technical specifications).

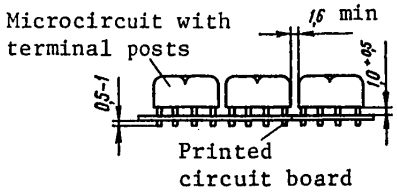


Figure 5-3. Assembly of microcircuits with terminal posts on a printed circuit board.

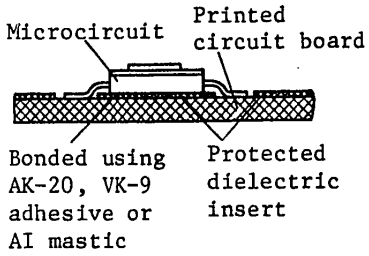


Figure 5-4. One-sided assembly of microcircuits on a printed circuit board.

Microcircuits in type-2 cases must be mounted on the boards with metal-plated holes with a clearance provided by the structural design of the terminals.

Microcircuits with planar leads are also recommended for installation on one side of a printed circuit board (Figure 5-4); only in technically justifiable cases is it permissible to mount them on both sides of the board (Figure 5-5). Such IC are mounted on an insert of insulating material or punch tape; they are fastened to the surface of the printed circuit board by microglue or epoxy adhesive. In some cases it is permissible to mount the IC tightly against the board or with a clearance of no more than 0.7 mm (if the technical specifications do not stipulate otherwise).

When mounting the IC on the printed circuit boards frequently the necessity arises for forming terminals (Figure 5-6). The requirements imposed on the

forming are stipulated in the technical materials. The round or strip terminals must be formed, and strip terminals pressed using the mounting tool or attachment in such a way as to exclude mechanical loads on the points where the terminal is fastened to the case.

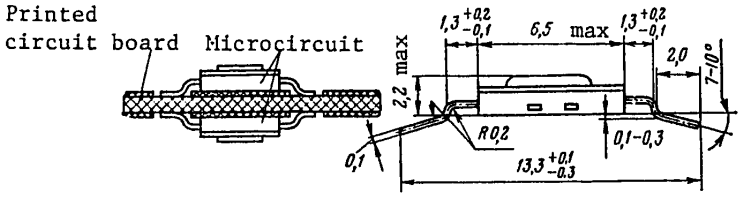


Figure 5-5. Two-sided mounting of microcircuits on a printed circuit board.

For IC with planar terminals the forming, as a rule, is done with a radius of bending of no less than 2 c (c is the thickness of the terminal) and a distance from the case to the center of the circle of bending of no less than 1 mm (unless stipulated otherwise in the technical specifications).

For microcircuits with terminal posts, as a rule the forming is done with a radius of bending of no less than 2 d (d is the terminal diameter) and a distance from the microcircuit case to the center of the circle of bending of no less than 1 mm (unless stipulated otherwise in the technical specifications).

The microcircuits are joined to the other elements of the subassemblies and modules of electronic equipment, as a rule, by soldering the terminals; therefore special attention must be given to the quality of the assembly. Frequently group soldering and "wave" soldering are used in series production. Under laboratory conditions and when replacing the microcircuits in operation, soldering by a single-tip soldering iron is used.

When making soldered connections of planar IC terminals by a single-tip soldering iron the following requirements must be observed (unless stipulated otherwise in the technical specifications): the temperature of the tip of the soldering iron must be no more than 265° C; the contact time with each terminal must be no more than 3 sec, the interval between soldering adjacent terminals must be 3-10 sec (depending on the type of IC case), and the distance from the case to the soldering point along the length of the terminal must be no less than 1 mm.

For microcircuits with terminal posts, the temperature of the soldering iron tip must not be greater than 280° C.

In the case of making group soldered connections in an IC, the temperature of the molten solder must be no more than 265° C, the time of its effect simultaneously on all of the terminals must not exceed 2 sec for planar terminals and 3 sec for terminal posts. The interval between repeated solderings of the terminals of one IC must be no less than 5 min.

It is often necessary to protect the case and the insulators of the IC terminals from vapor and spray from the soldering flux. After assembly, the soldering points must be cleaned to remove the flux by a liquid recommended in the technical specifications for the microcircuits. After mounting and cleaning off the flux the boards with the microcircuits are coated with protective lacquer (the types of lacquers are indicated in the technical specifications).

In order to eliminate the effect of the electrostatic charges on the microcircuits it is necessary:

a) to ground the tip of the soldering iron;

b) to ground the measuring and testing equipment;

c) perform the operations of preparing, assembling and checking the microcircuits using antielectrostatic bracelets or other means of removing the electric charge from the operator.

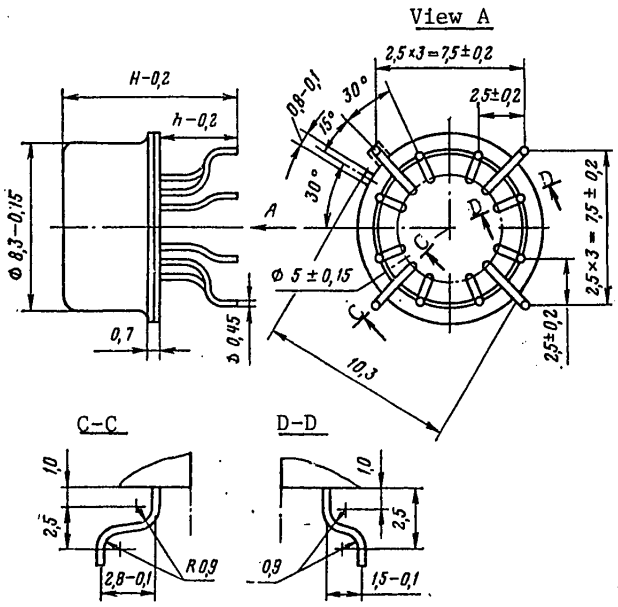


Figure 5-6. Forming the microcircuit terminals in case type 4 (a) and in case type 3 (b).

5-2. Examples of Constructing the Functional Subassemblies of Electronic Equipment Based on Digital Microcircuits

The series of digital microcircuits, as a rule, are functionally complete systems and can be used to construct the logical units of digital computers and the circuitry of digital automatic equipment of any functional complexity.

Each of the series of digital microcircuits is predominantly realized on a defined logical base. Thus, for example, the series of microcircuits of diode-transistor and transistor-transistor logic (for example, series 109, 217, K511, K131, K155, KM155, K158) contain predominantly the AND-NOT logical elements, combinations of them and different types of triggers. The transistor-transistor logic series popular among equipment developers (for example, the series K155, KM155) contain in practice finished functional units (counters, registers, adders, decoders, code converters, and so on).

Microcircuits based on resistor-transistor logic (series 114, 115, 211), resistive-capacitive transistorized (series 204), emitter-coupled logic (series K137, K138, K500), and microcircuits based on MDS-transistors (series K172, K178) are made on the basis of the OR-NOT logical elements, from which AND-OR, AND-OR-NOT, AND-OR/AND-OR-NOT and other elements are realized by defined circuit diagrams.

Series of digital microcircuits (for example, the series K176 based on the complementing MDS-transistors) consisting of two basic types of logical elements AND-NOT, OR-NOT are made.

When designing digital computers and the circuitry of digital automation, the necessity arises for the performance of many other auxiliary logical functions.

When designing the functional units it is necessary to consider the parameters of the microcircuits such as the average propagation delay time, switching speed, and noiseproofness of the microcircuits. It is especially important to consider the indicated parameters when designing printed circuit boards and modules and when calculating communication lines.

Therefore examples are presented below from the realization of logical and functional units based on digital microcircuits with a broad range of speeds, noiseproofness, intake power and different functional layout of the microcircuits of the following series:

K500 (based on the emitter-coupled logic);

K511 (microcircuits with high noiseproofness);

K176 (microcircuits with low intake power based on complementing MDS-transistors);

K131, K155, K158 (base on transistor-transistor logic).

All of the examples correspond to positive logic for which the logical one level corresponds to the most positive, and the logical zero level, the least positive value of the digital signal voltage.

K500 Series Microcircuits

General Instructions for Use. The recommendations with respect to the methods of connecting the inputs and combining outputs are as follows:

The K500 series microcircuits can be used in different mutual-connection versions and also when working with other radio-electronic elements under the condition of observation of the requirements of the technical specifications for the IC.

The inputs and outputs of the K500 series microcircuits unused in the diagram solutions remain free with the exception of the K500LP115, K500LP116 and K500PU124 microcircuits.

The free inputs of the K500LP115 and K500LP116 microcircuits are connected to the reference voltage source (to lead 9 for the K500LP115 microcircuit and to lead 11 for the K500LP116 microcircuit) or to a power supply voltage of 5.2 volts ± 5 percent.

The free inputs of the K500PU124 microcircuit are connected to a power supply voltage of 5.0 volts ± 5 percent through a 1-kilohm resistor. It is permissible to connect up to 20 free inputs to 1 resistor.

If microcircuits are installed on a printed circuit board to which it is necessary constantly to feed a logical zero voltage, then in order to obtain this voltage it is possible to use any logical microcircuit forming the indicated voltage level at the outputs. The number of loads connected to 1 output of such an element must not exceed 24.

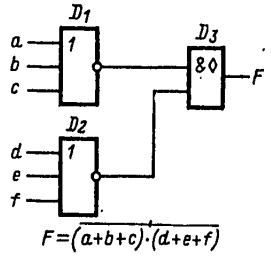


Figure 5-7. Circuit diagram of direct outputs to the "wired OR."

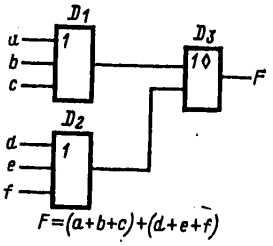


Figure 5-8. Circuit diagram of inverse outputs in a "wired AND."

The K500 series microcircuits permit combining with respect to outputs. The outputs of several elements (including triggers) can be combined into a "wired OR" and a "wired AND" with output grouping factor $K_{group\ out} \leq 4$ which is highly convenient for constructing the OR and the AND-OR-NOT logical circuits based on a large number of inputs.

Examples of the grouping of microcircuits with respect to outputs and the realized functions are presented in Figures 5-7 to 5-9.

This grouping method permits also the reception and transmission of data along one common signal line connecting several units as shown in Figure 5-10.

It is necessary to consider that depending on the number of groupings with respect to output $K_{group\ out}$ and the number of grouped inputs $K_{fan\text{-}in}$, the output voltage levels U^0_{out}, U^1_{out} vary, and the static noiseproofness of the microcircuits is reduced by an amount which can be defined by the formula

$$\Delta U_{int} \approx 25 \ln (K_{fan\text{-}in} K_{group\ out}).$$

In the mode of grouping the elements into a "wired OR" the situation can arise in which the logical one voltage at the output of the transmitting circuits will be maintained by several elements.

On switching at least one transmitting element from the logical "1" state to the logical "0" state, negative interference appears at the output of the combined circuits (C_3 of the diagram in Figure 5-11a) as a result of redistribution of the load current between the elements combined into the "wired OR," as shown in Figure 5-11b.

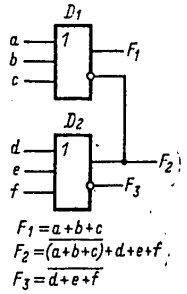


Figure 5-9. Circuit for combining the direct output with the inverse.

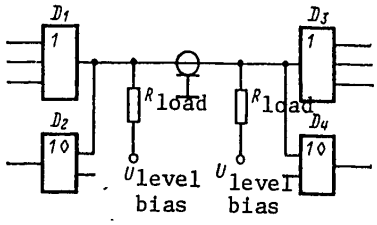


Figure 5-10. Circuit for combining the elements into a common communications line.

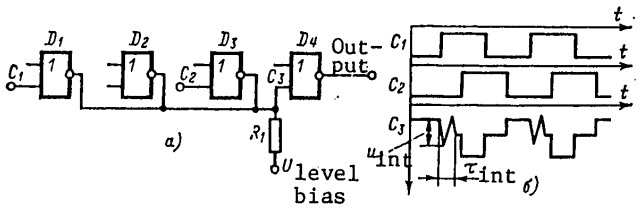


Figure 5-11. Coupling diagram for combining in a "wired OR" (a) and time diagram of the work (b). D_1, D_2, D_3 are K500 series microcircuits (signal force); D_4 is the K500 series microcircuit (element, load); R_1 is the B19-3-5 type resistor matrix.

The interference amplitude and duration depend on the length of the communications line connecting the elements into the "wired OR."

Combining the respective outputs to form logical functions is permissible within the limits of only one standard replacement element (TEZ) and the combined microcircuits arranged in a row insofar as possible.

The exit from the TEZ is made from any microcircuit not having a grouping with respect to output.

It is not recommended that information be transmitted beyond the TEZ from the inverse outputs of the K500LK117, K500LK121 microcircuits, directly from the outputs of the K500ID161, K500ID 162 microcircuits, directly from the outputs of the K500TM130, K500TM131 triggers, but it is permitted when using buffer elements at their output.

Recommendations With Respect to Load Capacity of the Microcircuits. As a result of the small output impedance of the emitter repeaters of the microcircuits and the low input current (less than 265 microamps), for one logical element input the connection of a significant number of logical loads to the circuit output in practice has no significant influence on the static parameters of the microcircuits. Therefore the load capacity depends only on the resistance of the load resistor R_{load} required to obtain the required output voltage levels in the logical zero and logical one state and the required output signal delays.

The maximum fan-out of the logical element $K_{fan-out}$ is equal to 20 for operation of the microcircuits within 1 TEZ and 10 for operation on external communication lines.

The minimum fan-out for the K500LL110 and K500LYe111 microcircuits designed for operation simultaneously on three transmission lines is 30, respectively.

For operation of a logical element on a load resistor R = 51 ohms on connection to the level bias voltage $U_{level\ bias}$ = -2 volts the increment in the delay on connection of each additional input of the load microcircuit is minimal and it amounts to about 0.1 nanosecond, and the variation in duration of the output front under load from 1 to 10 inputs does not exceed 0.5 nanosecond.

It is recommended that the output of the trigger microcircuits not be loaded with more than six loads. The output of the microcircuits combined in the "wired OR" should be loaded by no more than 16 loads; here it is necessary to consider the increase in the propagation delay time and reduction in the output voltage level.

In these cases for determination of the admissible number of inputs of the load microcircuits it is necessary to consider the grouping of several inputs of the elements within these microcircuits. The number of grouped inputs of the microcircuits is indicated in Table 5-1.

Table 5-1

Type of Microcircuit	Terminal Number (microcircuit input)	No of Inputs Connected to Given Output Inside Microcircuit	Type of Microcircuit	Terminal Number (microcircuit input)	No of Inputs Connected to Given Output Inside Microcircuit
K500LM101	12	4	K500TM130	09	2
K500LK117	09	2	K500TM131	09	2
K500LS118	09	2	K500TM133	13, 10, 05	2
K500LS119	10	2	K500TM134	07	2
K500LK121	10	2			

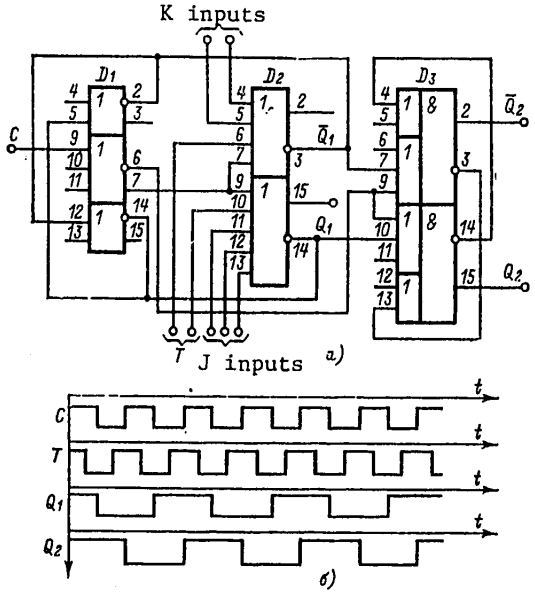


Figure 5-12. Functional diagram of a synchronous JK trigger (a) and operating time diagram (b). D_1--K500LM105 microcircuit; D_2--K500LM109 microcircuit; D_3--K500LK117 microcircuit.

When designing the functional units based on K500 series microcircuits it is necessary to consider that the microcircuits used include integrated microcircuits having a different number of elements and logical stages in them. Accordingly, the signal propagation delays for different "input-output" pairs can turn out to be different from each other. A different number of elements can be connected (inside the microcircuit) to the microcircuit input; the output elements of the microcircuit can be loaded on other elements (inside the microcircuit).

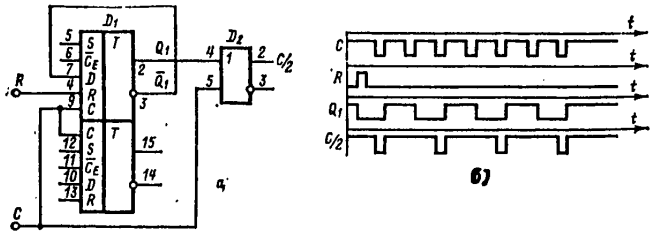


Figure 5-13. Functional diagram of a frequency divider by 2 (a) and operating time diagram (b). D_1--K500TM131 microcircuit; D_2--K500LM105 microcircuit.

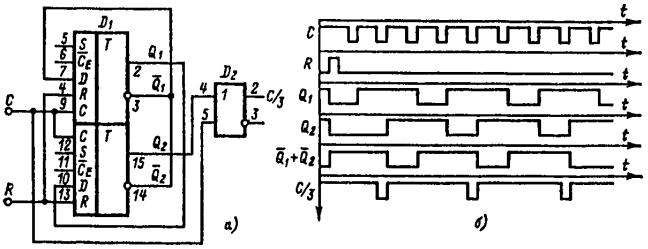


Figure 5-14. Functional diagram of a frequency divider by 3 (a) and operating time diagram (b). D_1--K500TM131 microcircuit; D_2--K500LM105 microcircuit.

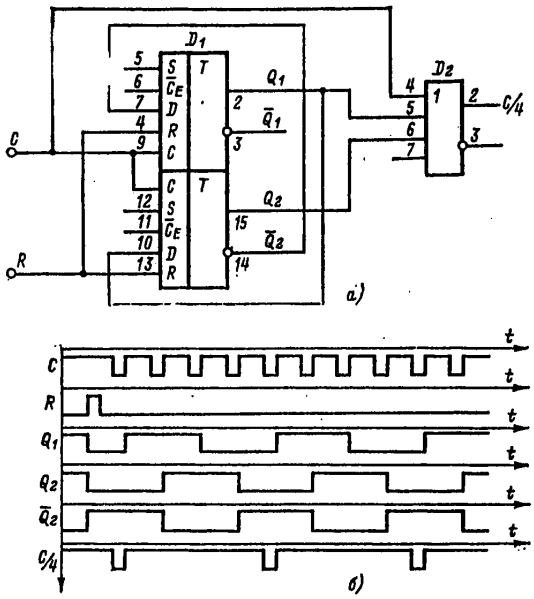


Figure 5-15. Functional diagram of a frequency divider by 4 (a) and operating time diagram (b). D_1--K500TM131 microcircuit; D_2--K500LM109 microcircuit.

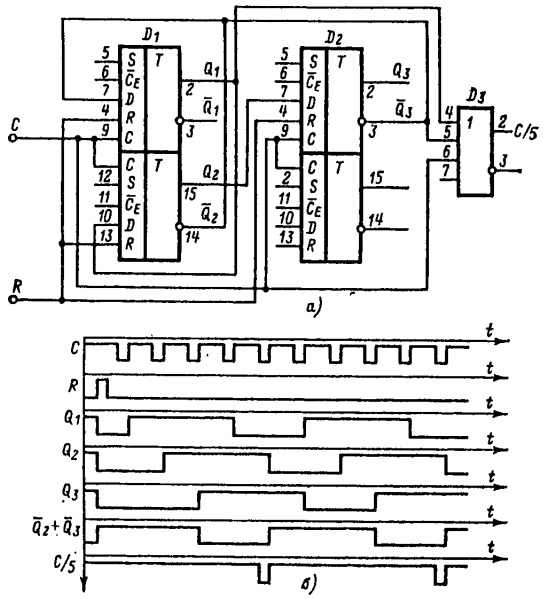


Figure 5-16. Functional diagram of a frequency divided by 5 (a) and operating time diagram (b). D_1, D_2--K500TM131 microcircuit; D_3--K500LM109 microcircuit.

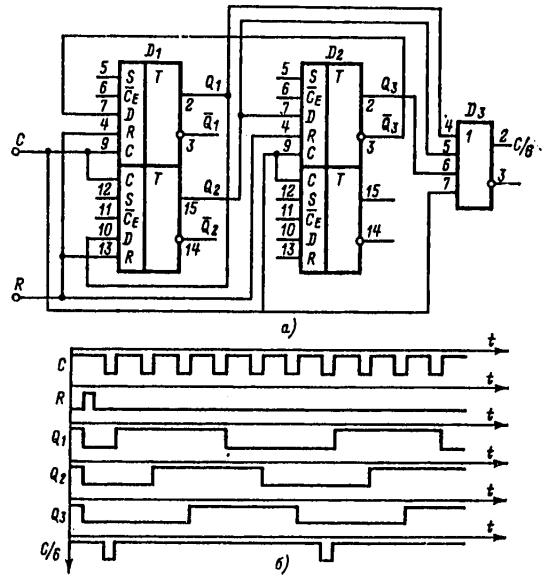


Figure 5-17. Functional diagram of a frequency divider by 6 (a) and operating time diagram (b). D_1, D_2--K500TM131 microcircuit; D_3--K500LM109 microcircuit.

The minimum duration of the setting and clearing pulses at the input of the K500TM131 microcircuits for which the trigger reliably switches to state "0" or "1" is equal to 4 nanoseconds.

The input signal frequency with respect to the synchronization input of the K500TM130, K500TM131, K500TM133, K500TM134 microcircuits must not exceed 200 millihertz.

For direct operation of the elements on each other (short unmatched communication lines), depending on the number of loads and required speed in the emitter circuits of the output repeaters load resistors of different ratings can be used which are connected either to the voltage power supply $U_{p\ s} = -5.2$ volts or to $U_{level\ bias} = -2.0$ volts.

The low output impedance of the elements ensures the possibility of exciting the transmission lines with wave impedance $\rho = 50$ ohms while maintaining high speed and the required noiseproofness.

The static potential on the microcircuit leads must not exceed the power supply voltage.

Standard Diagrams of the Application of K500 Series Microcircuits. Examples of the structure of the functional units in K500 series microcircuits are presented.

Triggers. The JK trigger executed from K500LM105, K500LM109 and K500LK117 microcircuits and its operating time diagram in the counting T-trigger mode are presented as an example in Figure 5-12.

Dividers. Figures 5-13 to 5-22 show the diagrams of frequency dividers by 2-10 constructed from K500TM131 triggers and the time diagrams explaining their operation. Gating by outputs is used to isolate the corresponding division pulse.

In Figures 5-14 to 5-21 gating is realized by the logical element of K500LM105 and K500LM109 microcircuits.

Resistors. Figure 5-23 shows the diagram of a 4-bit shift register. The output part of the diagram is executed from K500TM131 triggers, the diagram of the parallel information input is realized from K500LS119 microcircuits, the input part is a decoder for 2 inputs and 4 outputs, and it is executed from two K500LM105 microcircuits.

In order to increase the number of bits of the register, the information is fed to the D_{n-1} input from the output of the preceding bit and to the D_{n+4} input from the next bit.

Depending on the state of the signal at the inputs S_1 and S_2, the circuit performs the operations presented in Table 5-2.

For logical one at the inputs S_1 and S_2 the circuit operates four triggers with separate inputs and outputs.

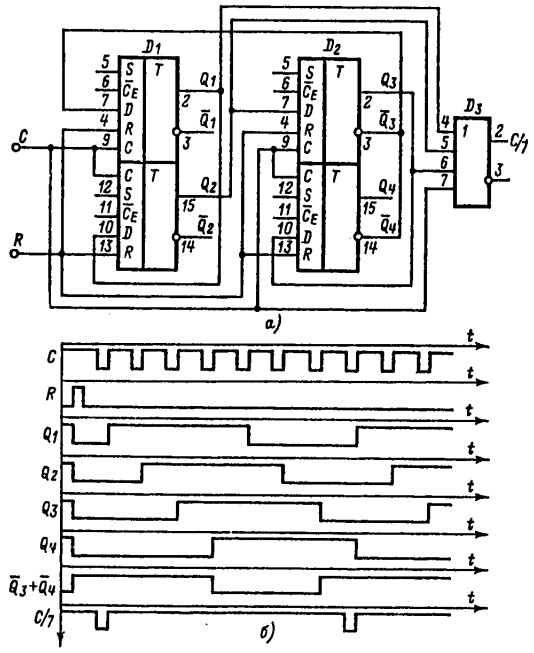


Figure 5-18. Functional diagram of a frequency divider by 7 (a) and operating time diagram (b). D_1, D_2--K500TM131 microcircuit; D_3--K500LM109 microcircuit.

Counters. A diagram of a synchronous double-pulse counter from 0 to 15 is presented in Figure 5-24, and its operating time diagram is presented in Figure 5-25. The circuit is executed from K500TM131, K500LC118 and K500LM105 microcircuits.

Table 5-2

Inputs		Performed Function
S_1	S_2	
0	0	Blocking
1	0	Shift right
0	1	Shift left
1	1	Reception D

The input Q_{n-1} realizes the carry from the preceding bit, the output Q_{n+4}, the carry to the next bit. Control is by the S input of the microcircuit D_7.

For logical one at the input S the circuit operates as a counter; for logical zero at the input S the circuit operates as four triggers and provides for receiving information by inputs D_0-D_3. Initially the counter is zeroed either

with respect to inputs D_0-D_3 or forced with respect to the inputs of the R triggers.

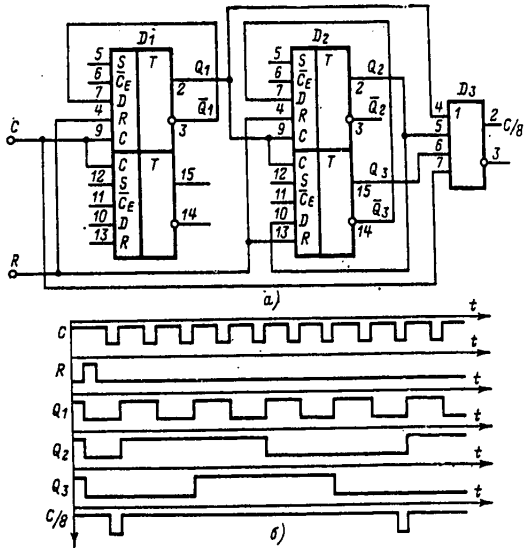


Figure 5-19. Functional diagram of a frequency divider by 8 (a) and operating time diagram (b). D_1, D_2--K500TM131 microcircuit; D_3--K500LM109 microcircuit.

Figure 5-26 shows the diagram of a synchronous binary-to-decimal counter built from K500TM131, K500LS119, K500LS118 and K500LM109 microcircuits. The binary-to-decimal counter counts from zero to nine.

The operating principle of the counter is analogous to the operation of a binary counter shown in Figure 5-24.

Figure 5-27 shows the diagram of a four-bit ring counter executed from K500TM131 microcircuits.

The circuit operates by the shift register principle. The counter is initialized with respect to the R trigger input.

Decoders. Figures 5-28 and 5-29 show diagrams of low- and high-level decoders for two inputs and four outlets executed from K500LM101 and K500LM105 microcircuits.

Figure 5-30 shows the diagram of a low-level decoder for 32 outputs executed from K500LM105 and K500ID161 microcircuits, and Figure 5-31 shows a high-level decoder for 16 outputs executed from the K500LM105 and K500ID 162 microcircuits.

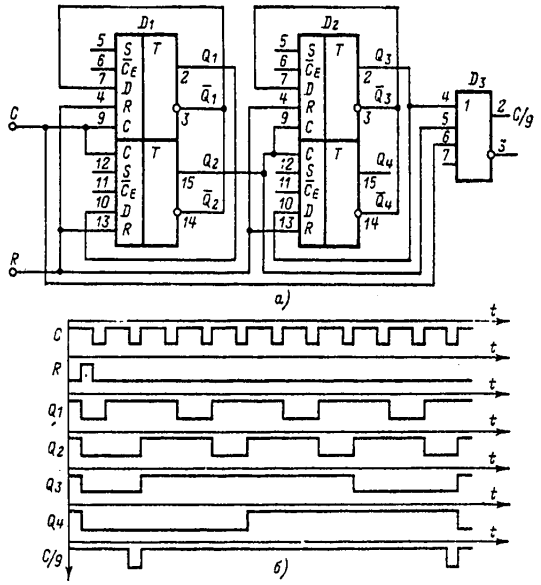


Figure 5-20. Functional diagram of a frequency divider by 9 (a) and operating time diagram (b). D_1, D_2--K500TM131 microcircuit; D_3--K500LM109 microcircuit.

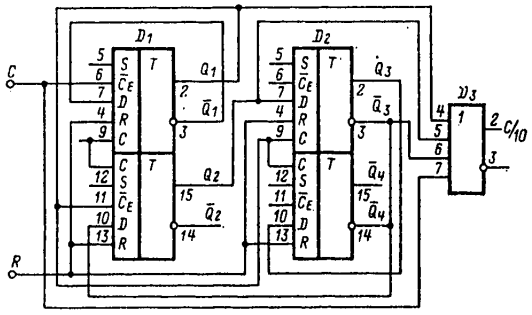


Figure 5-21. Functional diagram of a frequency divider by 10. D_1, D_2--K500TM131 microcircuit; D_3--K500LM109 microcircuit.

Parity Check Circuit. A diagram of a parity check circuit executed from K500IYe160 and K500LP107 microcircuits is presented in Figure 5-32.

Arithmetic Unit. In Figure 5-33 we have the diagram of a 16-bit logical-arithmetic unit with fast-carry circuit. The circuit is executed from K500IP181 and K500IP179 microcircuits.

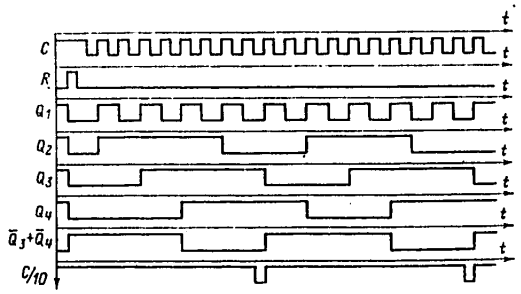


Figure 5-22. Operating time diagram of a frequency divider by 10.

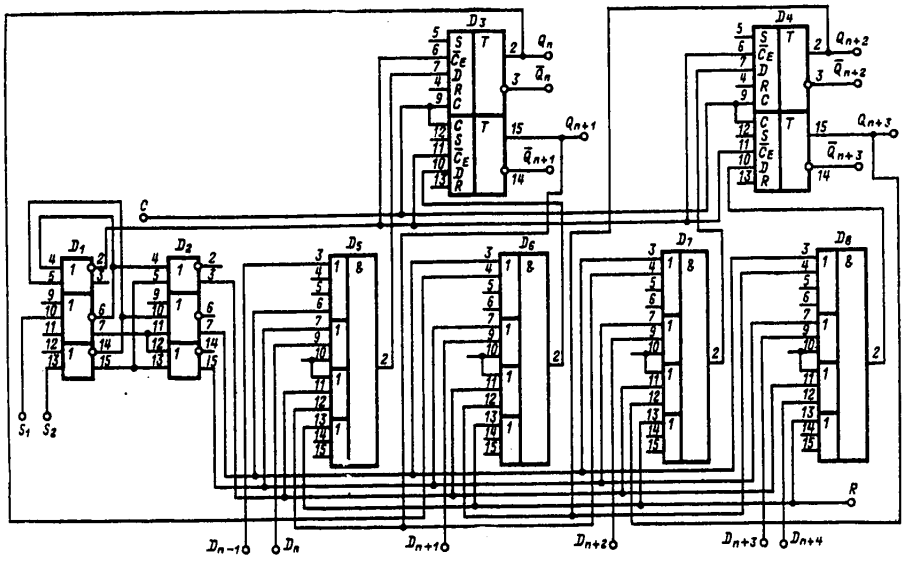


Figure 5-23. Functional diagram of a four-bit shift register. D_1, D_2--K500LM105 microcircuits; D_3, D_4--K500TM131 microcircuits; D_5-D_6--K500LS119 microcircuits.

Depending on the voltage level at the input M, the unit performs either logical or arithmetic operations.

With a logical one voltage at the input M the circuit performs only logical conversions of input variables A_0-A_{15} and B_0-B_{15}, and with a logical zero voltage, arithmetic operations on these variables.

Commutators. Figure 5-34 gives the diagram of a 32-channel commutator constructed from K500ID164 microcircuits.

The given circuit realizes conversion of parallel code (inputs X_1-X_{32}) to series code (output Y).

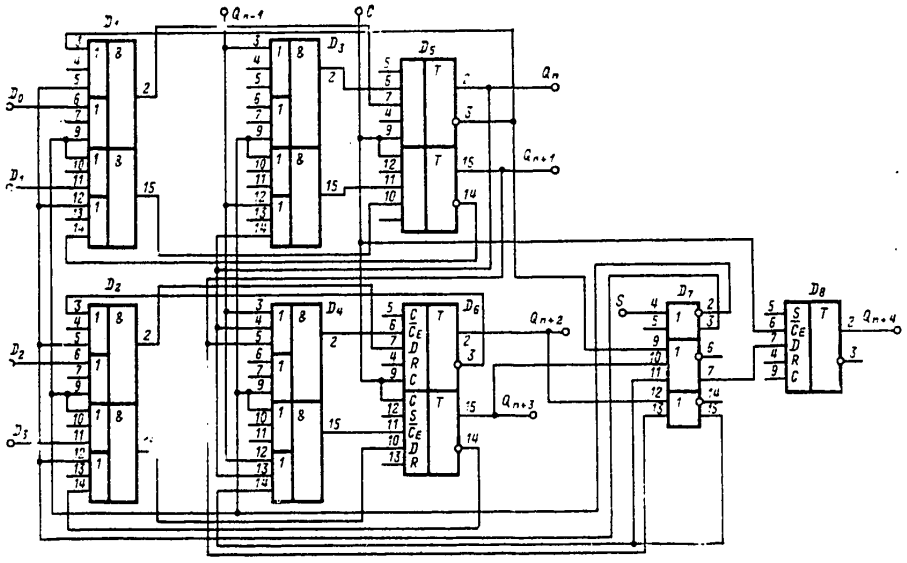


Figure 5-24. Functional diagram of a synchronous binary counter from 0 to 15. D_1-D_4--K500LS118 microcircuits; D_5, D_6, D_8--K500TM131 microcircuits; D_7--K500LM105 microcircuit.

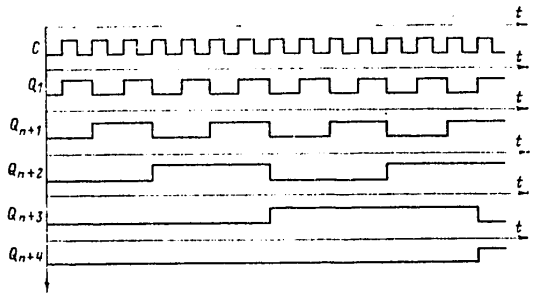


Figure 5-25. Operating time diagram of a synchronous binary counter from 0 to 15.

The control with respect to the address inputs C_0-C_4 can be realized by pulse counters.

The transmission of pulses from the information inputs X_1-X_{32} to the output Y depends on the state of the address inputs C_0-C_4.

Pulse Generators. The microcircuits K500LP115, K500LP116, K500ML101, K500LM105, K500LM109 with the application of a capacitor or delay line are recommended for use in the construction of pulse generators.

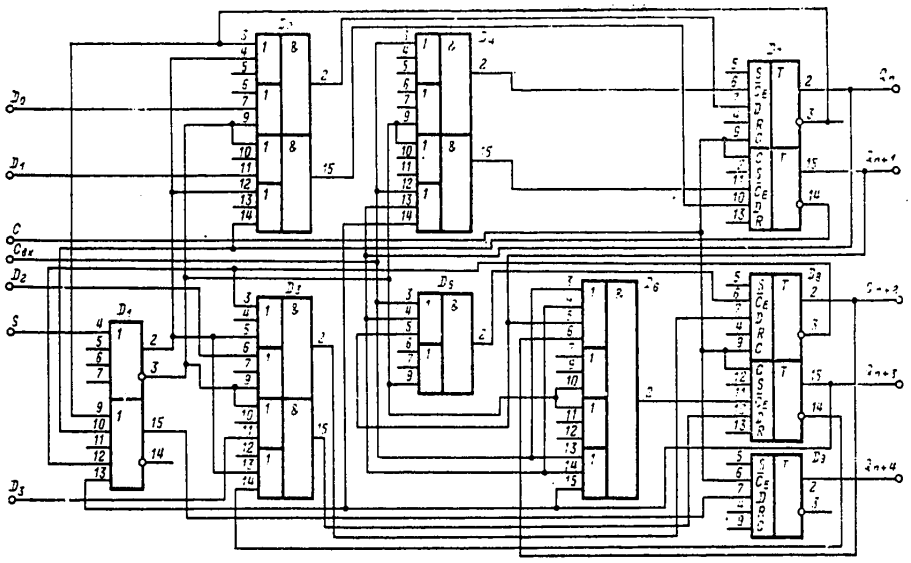


Figure 5-26. Functional diagram of a synchronous binary-to-decimal counter. D_1--K500LM109 microcircuit; D_2-D_5--K500LS118 microcircuits; D_6--K500LS119 microcircuit; D_7-D_9--K500TM131 microcircuits.

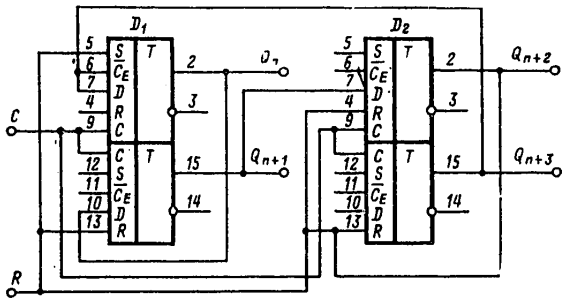


Figure 5-27. Functional diagram of a four-bit ring counter. D_1, D_2--K500TM131 microcircuits.

A diagram of a pulse generator constructed from a K500LP116 microcircuit with the application of external capacitor and resistors is presented in Figure 5-35.

A diagram of a pulse generator constructed from a K500LM105 microcircuit using a delay line and also its operating time diagram are presented in Figure 5-36.

As the delay line it is preferable to use a cable with wave impedance ρ = 50 ohms, type RK50-1-21. Another type of cable with ρ = 50 ohms is permissible.

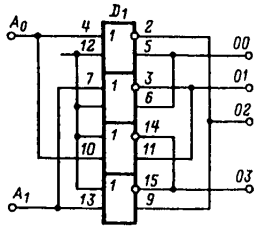


Figure 5-28. Functional diagram of a four-output low-level decoder. D_1--K500LM101 microcircuit.

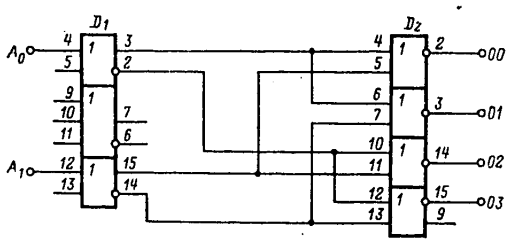


Figure 5-29. Functional diagram of a four-output high-level decoder. D_1--K500LM105 microcircuit; D_2--K500LM101 microcircuit.

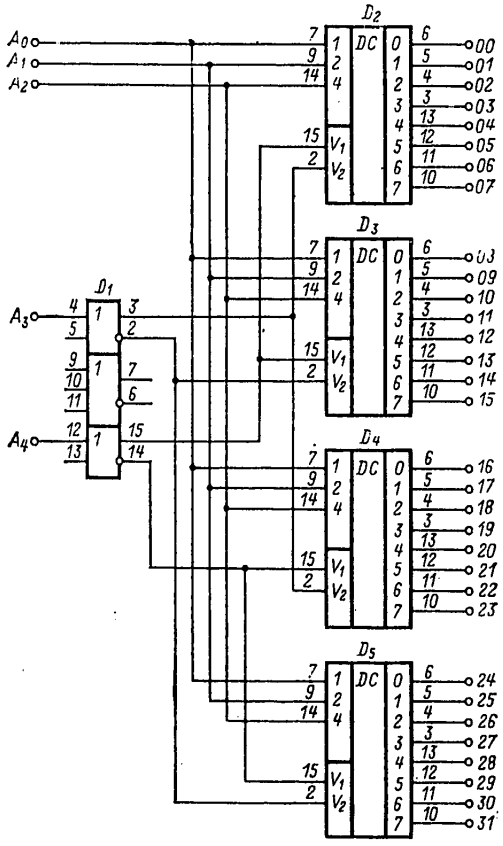


Figure 5-30. Functional diagram of a 32-output low-level decoder. D_1--K500LM105 microcircuit; D_2-D_5--K500ID161 microcircuits.

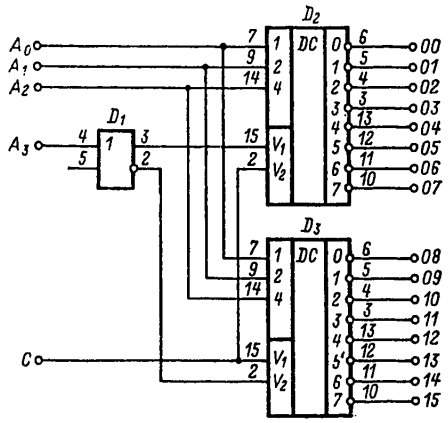


Figure 5-31. Functional diagram of a 16-output high-level decoder. D_1--K500LM105 microcircuit; D_2, D_3--K500ID162 microcircuits.

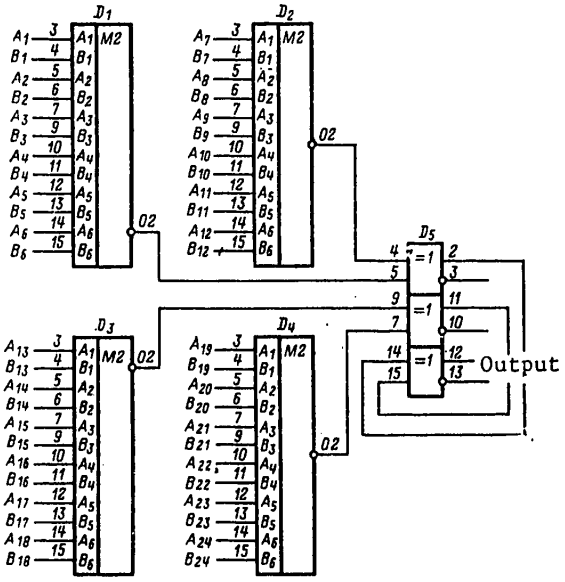


Figure 5-32. Functional diagram of a 48-input parity check circuit. D_1-D_4--K500IYe160 microcircuits; D_5--K500LP107 microcircuits.

The generator pulse duration is determined by the sum of the delays in the logical element and in the delay line. The maximum operating frequency of the generator is up to 35 millihertz.

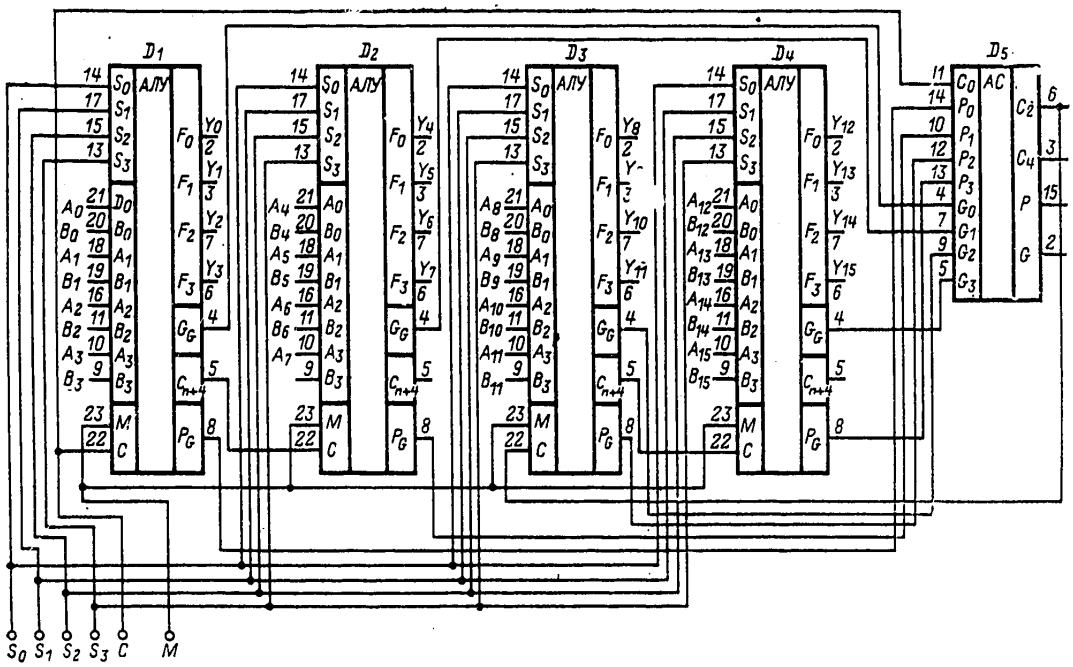


Figure 5-33. Functional diagram of a 16-bit arithmetic unit. D_1-D_4--K500IP181 microcircuits; D_5--K500IP179 microcircuit.

Display Circuit. The recommended display circuit constructed from K500PU125 microcircuit and K155LA7 microcircuit series K155 using incandescent tube SMN6.3-20 is presented in Figure 5-37.

Recommendations for Coupling the K500 Series Microcircuits to Other Series. For joint operation of the K500 series microcircuits with type TTL microcircuits (for example, K131, K155) the series includes the K500PU125 microcircuit, the ESL level converter and the TTL microcircuit. In Figure 5-38 we have a quarter of the schematic diagram of the K500PU125 microcircuit.

Each converter consists of a current switch with transistorized current generator in the emitter circuit assembled from the VT_6 transistor and the resistor R_9 and a saturated output stage analogous to the inverter of the TTL circuits.

The built-in reference voltage power supply (VT_1, VT_2, VD_1, VD_2, VD_3, VD_4, R_2, R_3, R_1, R_4) provides for a bias on the current generator (VT_6, R_9) and generates two reference voltages: $U_{ref\ 1}$ equal to minus 2.8 volts picked up from the collector of the transistor (VT_2 and $U_{ref\ 2}$ equal to minus 1.29 volts picked up from the emitter of the transistor VT_1.

The reference voltage $U_{ref\ 1}$ is required for fixing the logical zero output voltage when the circuit inputs are connected to the minus 5.2-volt power supply or they are free.

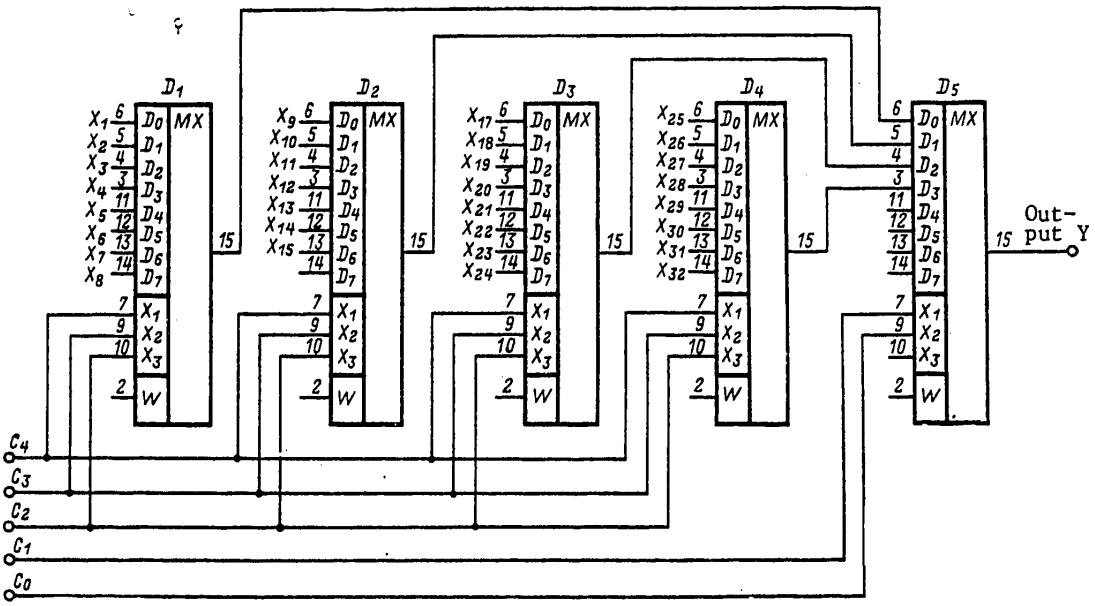


Figure 5-34. Functional diagram of a 32-channel commutator.

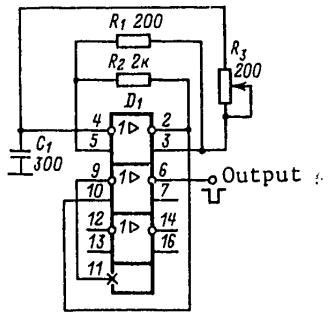


Figure 5-35. Diagram of a pulse generator.

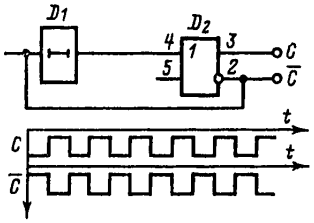


Figure 5-36. Diagram of a pulse generator and its time diagram.

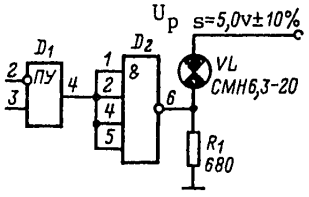


Figure 5-37. Display circuit with the application of an incandescent tube. D_1--K500PU125 microcircuit; D_2--K155LA7 microcircuit.

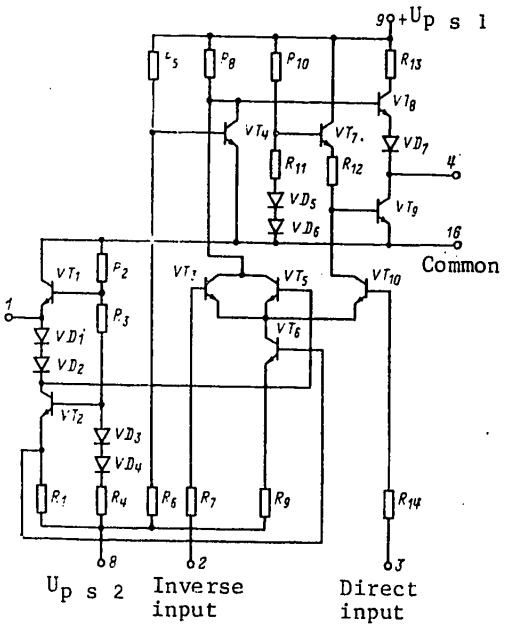


Figure 5-38. K500PU125 microcircuit.

When using the circuit as a single-input level converter, the voltage $U_{ref\ 2}$ from the terminal 1 is connected to terminal 2 or 3 depending on whether the inverted or not inverted conversion must be made by the circuit. Thus, in the case of connecting the $U_{ref\ 2}$ to the input 3 and with a logical one voltage on the input 2 the transistor VT_3 is open, and VT_{10} is closed, and the resistor R_8 is selected so that in the investigated case the voltage on the base of the transistor VT_8 will be about 1 volt, which is sufficient for blocking the transistor VT_8. Here the divider (R_{10}, R_{11}) ensures operating conditions of the transistor VT_7 for saturation of the transistor VT_9, and at the output 4, the logical zero voltage.

When feeding the logical zero voltage to the input 2, the transistor VT_{10} opens, and the transistor VT_3 closes. Here the base potential of the transistor VT_9 drops to minus 1 volt, and the transistor VT_9 closes, and the logical one voltage is ensured at the output 4.

When using all four elements of the K500PU125 microcircuit the reference voltage $U_{ref\ 2}$ from the terminal 1 is fed to the corresponding inputs of the four elements.

When designing the functional units it is necessary to consider that the output voltage of the K500PU125 microcircuit $U^0_{out} \leq 0.5$ volt, which lowers the noiseproofness by 100 millivolts on matching with the TTL circuits of the K131 and K155 series.

Operating Conditions of the K500PU125 Microcircuit. A feed voltage of 5.0 volts ± 5 percent is fed to the terminal 9, a feed voltage of 5.2 volts ± 5 percent is fed to terminal 8, terminal 16 of the microcircuit is common, and the outputs are terminals 4, 5, 12 and 13.

The fan-out of the K500PU125 microcircuit when operating on logical elements of the K155 series microcircuits is no more than eight, and for elements of the K131 series, no more than six.

For transition from the TTL levels to the ESL levels, the K500PU124 microcircuit is used in the K500 series. A quarter of the K500PU124 microcircuit is presented in Figure 5-39.

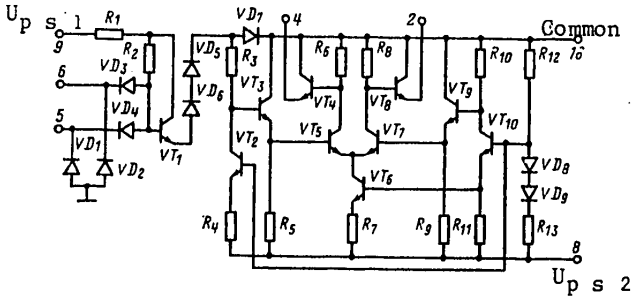


Figure 5-39. K500PU124 microcircuit.

Each of the four converters consists of input diodes, VD_1-VD_4, the input emitter repeater based on the VT_1 transistor, the differential amplifier based on the VT_5 and VT_7 transistors operating in the current switch mode, the input emitter repeaters and source of reference voltages based on the VT_9, VT_{10} transistors.

The reference voltage source forms the bias on the current generator VT_6 picked up from the emitter of the transistor VT_{10} and two reference voltages: $U_{ref\ 1}$ equal to minus 1.2 volts and $U_{ref\ 2}$ equal to minus 0.7 volt.

The voltage $U_{ref\ 1}$ from the emitter of the transistor VT_9 is fed to the right arm of the differential amplifier (VT_7); the voltage from the resistor R_{12} is fed to the base of the current generator (VT_2).

With a logical one voltage at the input equal to 2.4 volts, on the base of the transistor VT_3 there will be a voltage on the order of 0.05 volt, the voltage on the base of the transistor VT_5 in this case is approximately minus 0.8 volt, which corresponds to the logical one voltage of the ESL circuit. The transistor VT_5 is open, and the logical zero voltage is set on the output 4, and the logical one voltage, on output 2.

Operating Conditions of the K500PU124 Microcircuit. A feed voltage of 5.0 volts ± 5 percent is fed to the terminal 9; a feed voltage of minus 5.2 volts ± 5 percent is fed to terminal 8, the terminal 16 is common, the load is connected correspondingly to the paraphase outputs 4 and 2, 3 and 1, 12 and 15, 13 and 14.

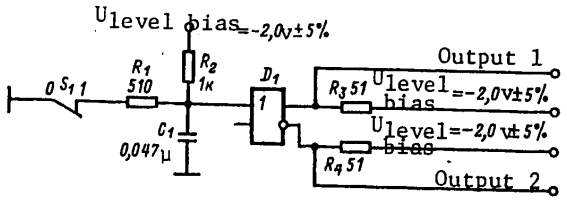


Figure 5-40. Diagram of the switching unit based on the K500LM105 microcircuit.

In order to realize the possibility of gating all four of the circuit elements the second inputs of each element are grouped at the input 6.

In the saturated logic circuits, as is known, during switching significant pulse interference arises which can lead to a breakdown during information transmission over the signal lines. For suppression of such interference all of the circuit inputs are connected to a common bus through the return-bias diodes VD_1, VD_2.

The signal communication lines ESL and TTL of the logical levels must be laid separately using shielded bunched conductors or cables.

Recommendations for Coupling Mechanical Switching Elements With Series K500 Microcircuits. For manual control of the operating conditions of the functional units, mechanical switching elements are used.

For conversion of the "on-off" state of mechanical elements (buttons, toggle switches, switches, and so on) to the logical levels of the series K500 IC, it is recommended that converter systems presented in Figures 5-40 and 5-41 be used.

In logical circuits where the "jarring" of the voltage level at the output of the pulse counter of the converter can be permitted on switching of the mechanical elements, it is recommended that the switching unit diagramed in Figure 5-40 be used.

In logical circuits where the "jarring" of the voltage level at the output of the IC of the converter is inadmissible, it is recommended that the trigger type switching unit shown in Figure 5-41 be used.

The "on" state of the mechanical element corresponds to a high voltage level on the direct output of the converter pulse counter and a low voltage level on the inverse output.

The "off" state of the mechanical element corresponds to a low voltage level on the direct output of the pulse counter of the converter and high on the inverse output.

It is recommended that the connections between the mechanical elements and the converter inputs be made by single, unshielded wires laid in a separate cable assembly.

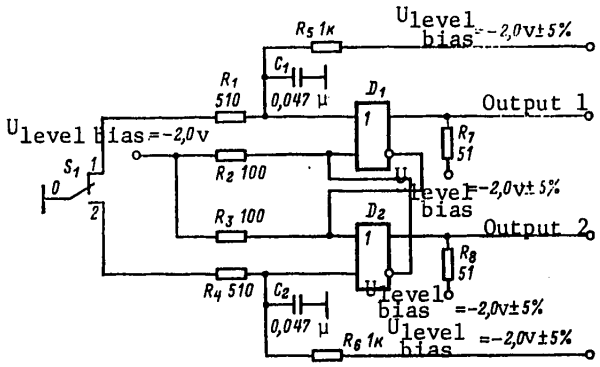


Figure 5-41. Diagram of a trigger-type switching unit based on the K500LM105 microcircuit.

It is not permissible to combine the couplings to the mechanical elements and the signal communication lines in one cable assembly.

Recommendations With Respect to Matching and Electrical Communication Lines. The signal transmission beyond the TEZ can be accomplished both by paraphase and single-phase signals. The transmission of paraphase signals can be accomplished using the K500LP115 and K500LP116 microcircuits which are signal receivers from the line and are used for two purposes:

as signal receivers from the paraphase signal reception line from two-wire communication lines; here the leads of the reference voltage sources (terminal 9 of the K500LP115 microcircuit and terminal 11 of the K500LP116 microcircuit) are not used;

as logical elements with logical zero or logical one DC voltages at the input with external commutation of terminal 9 with the inputs 5, 6, 11, 12 or 4, 7, 10, 13 of the K500LP115 microcircuit and commutation of terminal 11 with inputs 5, 10, 13 or 4, 9, 12 of the K500LP116 microcircuit.

Simultaneous use of both regimes for the elements entering into one microcircuit case is permitted.

The single-phase signal must reach one of the inputs of the receiving element of the K500LP115 or K500LP116 microcircuit, and a reference voltage must be fed to the second input which will be generated by a reference voltage source in the K500LP115 microcircuit (terminal 9) or K500LP116 microcircuit (terminal 11) located in the panel transmitting the signal.

One reference voltage source in the transmitting panel must be loaded in the receiving panel for no more than 10 inputs of the receivers.

Each K500LP115 or K500LP116 microcircuit can be used simultaneously as a reference voltage source for transmissions beyond the panel and a line signal receiver.

The reference voltage transmission line must be decoupled on the transmitting and receiving end by capacitors with a capacitance of no less than 100 picofarads.

The decoupling capacitors must be placed in each receiving TEZ one at each input of the receiving IC independently of the number of receiving microcircuits K500LP115 or K500LP116 in the given TEZ.

The interpanel signal transmission circuit is presented in Figure 5-42.

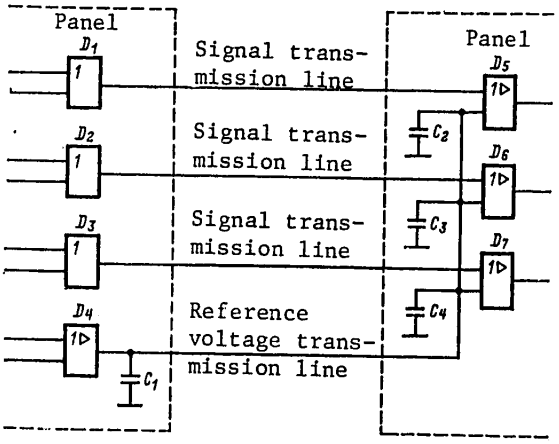


Figure 5-42. Diagram of interpanel signal transmission. D_1-D_3--K500 series microcircuits; D_4-D_7--K500LP115 (K500LP116) microcircuits; C_1-C_4--reference voltage decoupling capacitors.

Three basic methods of making the connections between elements are recommended in the TEZ: series method of load distribution along the communication line (Figure 5-43) without taps (load elements D_2, D_3, D_8, D_9) and with taps (load elements D_4, D_5, D_6, D_7); radial (the ray method) as illustrated in Figure 5-44; lumped load method at the end of the communication line as illustrated in Figure 5-45.

When combining elements into the "wired OR" it is recommended that the following two methods be used to make the connections between them:

the one-sided method in which the elements--signal forces--are placed on one side with respect to the outputs of the load elements; alternation of the outputs of the elements--signal sources--and the inputs of the load elements along the communication line is not permitted in this case;

two-sided method in which the elements--signal sources--are placed on both sides with respect to the inputs of the load elements as illustrated in Figure 5-46; here the inputs of the load elements are connected to one point of the communication line joining the microcircuit output.

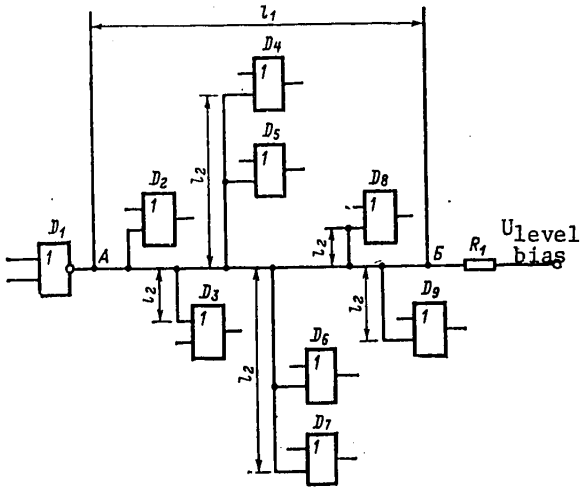


Figure 5-43. Diagram of the series method of splitting the load with taps. D_1--K500 series microcircuit (signal source); D_2-D_9--K500 series microcircuits (load element); R_1-B19-3-5-type resistor matrix; ℓ_1--recommended length of the communication line A, B no more than 200 mm; ℓ_2--recommended tap length of the communication line no more than 30 mm.

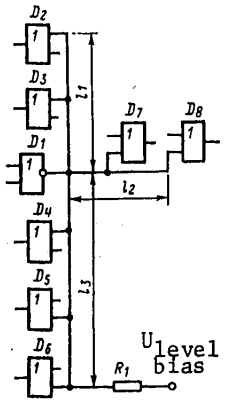


Figure 5-44. Diagram of the radial (ray) method of load distribution. D_1--microcircuit of the K500 series (signal source); D_2-D_8--microcircuits of the K500 series (load element); R_1--resistor matrix of the B19-3-5 type; ℓ_1, ℓ_2, ℓ_3--recommended length of the communication line no more than 70 mm.

It is recommended that the communication lines be matched. In the unmatched communication lines when the level bias voltage of the transmitting element is

realized by the power supply voltage of minus 5.2 volts, as illustrated in Figure 5-47, when switching the D_1 element a "jarring" arises at the input of the element D_2, the magnitude of which can be transmitted through the open transistor to the output of the element D_2. The occurrence of a "jar" and the magnitude of its amplitude depend on the length of the communication line between the elements D_1, D_2.

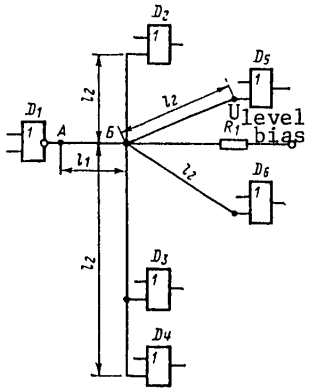


Figure 5-45. Diagram of the lumped method of splitting the load. D_1--K500 series microcircuit (signal source); D_2-D_6--K500 series microcircuit (load element); R_1--B19-3-5-type resistor matrix; ℓ_1--recommended length of communication line no more than 200 mm; ℓ_2--recommended length of communication line tap no more than 200 mm.

The recommended maximum length between the elements D_1, D_2 of a microstrip line with signal propagation delay in the line of 0.05 nanosecond/cm and a strip line with signal propagation delay in the line of 0.1 nanosecond/cm is presented in Table 5-3 as a function of the number of loads N connected to the element D_1.

Table 5-3

Communication Line	Line Resistance ρ, ohms	N = 1 (4 pf) ℓ, mm	N = 2 (8 pf) ℓ, mm	N = 4 (16 pf) ℓ, mm	N = 8 (32 pf) ℓ, mm
Microstrip line	50	200	190	170	145
	75	175	150	115	90
	100	160	130	90	65
Strip line	50	165	150	130	115
	75	135	115	90	70
	100	120	100	70	55

When the coupling length indicated in Table 5-3 is exceeded, the coupling must be matched.

Series and parallel methods of matching are recommended.

The series method of matching is recommended for concentrated load at the end of the communication line. The diagram of the series method of matching is presented in Figure 5-48.

The B19-3-5-type resistor matrix with the following parameters, R_1 = 43 ohms, R_2 = 240 ohms, for matching the communication line with the wave impedance ρ = 50 ohms is recommended for matching the communication line in Figures 5-48 to 5-51.

Other types of resistor matrices or individual resistors can be used.

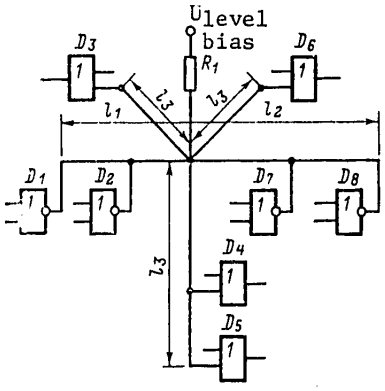


Figure 5-46. Diagram of two-sided method of coupling when grouping in a "wired OR." D_1, D_2, D_7, D_8--K500 series microcircuits (elements combined in the "wired OR"); D_3, D_4, D_5, D_6--K500 series microcircuits (load element); R_1--B19-3-5-type resistor matrix; ℓ_1, ℓ_2--recommended length of the communication line no more than 150 mm; ℓ_3--tap length of the communication line no more than 30 mm.

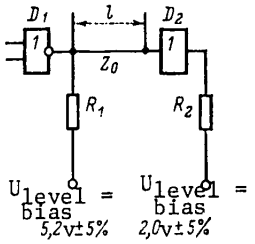


Figure 5-47. Diagram of connecting the load to an unmatched communication line. D_1--K500 series microcircuit (signal source); D_2--K500 series microcircuit; R_1--resistor MLT-0.125-510 ohms ± 5 percent; R_2--resistor MLT-0.125-510 ohms ± 5 percent.

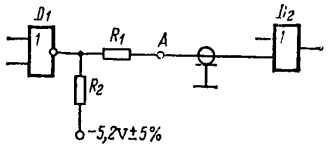


Figure 5-48. Series matching circuit of a communication line. D_1--K500 series microcircuit (signal source); D_2--K500 series microcircuit (load element); R_1, R_2--B19-3-5-type resistor matrix.

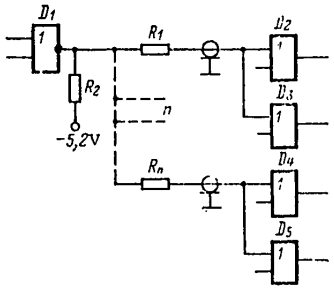


Figure 5-49. Series matching circuit with parallel communication lines. D_1--K500 series microcircuit (signal source); D_2-D_5--K500 series microcircuit (load element); n--number of parallel communication lines; R_1, R_2--B19-3-5-type resistor matrix.

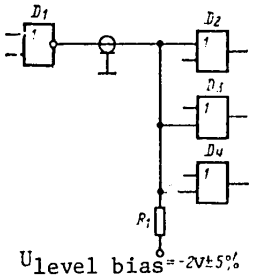


Figure 5-50. Parallel matching circuit of communication lines. D_1--K500 series microcircuit (signal source); D_2, D_3, D_4--K500 series microcircuit (load element); R_1--B19-3-5-type resistor matrix.

The resistance R_1 is selected within the limits of 10-75 ohms depending on the wave impedance of the communication line and it is selected from the condition of equality of equivalent resistance to the point A (Figure 5-48) to the wave impedance of the communication line. For a communication line with ρ = 75 ohms the resistance R_1 is about 68 ohms.

A deficiency of the series method of matching is the fact that the load must be lumped at the end of the communication line.

An admissible number of loads on the communication line must be no more than 10.

It is permissible during successive matching to increase the number of parallel communication lines as shown in Figure 5-49.

The resistance R_1-R_n is selected just as when using one communication line.

The value of the resistance R_2 must be selected so that the required current of each matching line will be ensured.

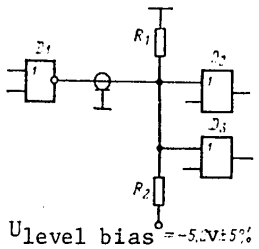


Figure 5-51. Parallel matching circuit of communication lines. D_1--K500 series microcircuit (signal source); D_2, D_3--K500 series microcircuit (load element); R_1, R_2--B19-3-5-type resistor matrix.

The maximum value of R_2 can be determined by the measurement method or estimated by the following formula:

$$R_2 = (10\rho - R_1)/n,$$

where n is the number of parallel matching lines, no more than 10. The total number of loads on the communication line must be no more than 10. For n = 4, ρ = 75 ohms, R_1 = 68 ohms, the value of the resistor resistance R_2 = 170 ohms.

In order to increase the speed and for control of the load elements distributed along the communication line, parallel matching of the communication line is used.

Parallel matching (Figure 5-50) is used for communication lines with ρ = 50 ohms using the level bias source voltage $U_{level\ bias}$ equal to minus 2 volts ± 5 percent.

The matching resistor R_1 with a resistance of 51 ohms is installed after all the load elements; it is also the load resistance of the output stage of the microcircuit.

Another method of parallel matching is permitted (Figure 5-51) with the help of two resistors using the level bias source voltage $U_{level\ bias}$ equal to minus 5.2 volts ± 5 percent.

The recommended values of the resistances R_1 and R_2 are presented in Table 5-4 as a function of the wave impedance ρ of the line.

Table 5-4

ρ, ohms	R_1, ohms	R_2, ohms
50	82	130
75	120	200
100	160	260
150	240	390

The length of the communication line, the taps from the communication line between the load elements depends on the specific structural design of the boards, the arrangement of the microcircuits on the boards which must be considered when designing a specific structure.

Estimating the Signal Propagation Delay Time in the Functional Circuits. When estimating the signal propagation time in the functional circuits it is necessary to consider that the propagation delay times depend to a significant degree on the communication lengths between the elements and the mutual arrangement of the microcircuits.

The signal propagation delay time in the functional circuits is estimated by the formula

$$t_{del\ p\ c} = t_{del\ p\ n} + t_{del\ p\ com} + t_{int}$$

where $t_{del\ p\ c}$ is the signal propagation delay time in a circuit of n logical elements and n - 1 communication lines; $t_{del\ p\ n}$ is the signal propagation delay time in n logical elements; $t_{del\ p\ com}$ is the propagation delay time in n - 1 communication lines; t_{int} is the duration of the interference.

The signal propagation delay time in n logical elements is made up of the values:

$$t_{del\ p\ n} = t_{del\ p\ mean} + t_{del\ p\ N} + t_{del\ p\ L},$$

where $t_{del\ p\ mean}$ is the mean signal propagation delay time in logical integrated microcircuits; $t_{del\ p\ N}$ is the signal propagation delay time occurring as a result of the effect of the loads (signal receivers) in the circuit; $t_{del\ p\ L}$ is the signal propagation delay time occurring as a result of the effect of the loads (signal sources) in the circuit when grouping the signal sources by output.

The duration of the interference t_{int} is defined as follows: If there are no elements in the circuit which are grouped by output, then $t_{int} = 0$; if there are elements in the circuit which are grouped by output and the elements are located in three or more microcircuit cases in a row, then $t_{int} = 3$ nanoseconds; if the elements are arranged along the length of the communication line to 150 mm, then $t_{int} = 10$ nanoseconds.

Effect of Pulsed Interference of Trigger Circuits on the Design of the Functional Units. When designing the functional units based on K500TM130, K500TM131, K500TM133 and K500TM134 microcircuits, it is necessary to consider that during synchronization and also during setting and clearing the indicated microcircuits generate pulsed interference at the trigger outputs, the amplitude of which can have a significant influence in the synchronized system on the speed of the systems and the correctness of functioning of the individual units.

In the synchropulse fronts pulsed interference is generated when switching the triggers, the maximum amplitude of which reaches 160 millivolts and the duration reaches 4 nanoseconds.

Recommendations With Respect to Filtering the Feed Voltage, Splitting of the Feed and Cooling. The power supply voltage is filtered with respect to the "ground" bus. It is recommended that no less than one 0.047-microfarad capacitor be installed for six microcircuits.

The recommended types of capacitors are as follows: KM-5a-890-0.047 microfarad, K53-4-15-6.8±20%. The capacitors are distributed uniformly with respect to the microcircuit installation rows.

The feed voltage of the units and modules executed from K500 series microcircuits ("feed" and "ground" buses) must be split using wires with the lowest possible resistance.

When using the multilayered printed circuit boards, it is recommended that the "feed" buses be laid out in one layer and the "round" buses in another, adjacent layer. The buses must be located one over the other. In the presence of a free area of the layer it is recommended that it be used to increase the surface of the "ground" bus.

During the design and operation of equipment using the K500 series microcircuits it is necessary to provide efficient cooling of the microcircuits by installing cooling radiators or blowing with air from the condition of ensuring the thermal resistance of the "crystal-medium" within the limits of 25-50° C/watt.

When using the K500 series microcircuits it is necessary to consider the time of establishment of thermal equilibrium in which the electrical parameters of the microcircuits become stabilized. The thermal equilibrium depends on the heat removal conditions.

Under the conditions of thermal "crystal-medium" resistance of no more than 50° C/watt and blowing with air at a velocity of 2.8 m/sec the setup time is 10-30 seconds depending on the power of the circuit.

K511 Series Microcircuits

The K511 series microcircuits are highly noise-resistant logical microcircuits (VPL IC), and they are designed for use in industrial automation, in the digital technological process control systems, in data transmission units for long

distances and they are capable of functioning under conditions of increased electrical interference.

The rules presented below are recommendations with respect to the most effective application of VPL IC.

The operating conditions of microcircuits as part of equipment must not exceed the operating conditions established by the technical specifications.

The splitting of the feed voltage of the units and modules executed on the basis of the K511 series microcircuits ("ground" and "feed" buses) must be done by wires with the lowest possible resistance.

When using the multilayered printed circuit boards it is recommended that the "feed" buses be in one layer and the "ground" buses in another adjacent layer; the buses should be located one above the other. In the presence of a free area of the layer it is recommended that it be used to increase the surface of the "ground" bus.

When using two-sided boards the best results are achieved if the "feed" and "ground" buses form continuous closed circuits. The edge contacts of the end plug are used for the ground circuits, and the contacts beside them, for feed circuits. The main "feed" and "ground" buses are run along the edges of the board, and perpendicular to them and the longitudinal axes of the VPL IC cases are the buses by which the feed and ground to all of the VPL IC are laid out. In the middle of the printed circuit board all of the "feed" and "ground" buses are also connected by foil strips.

It is most expedient to use two-sided printed circuit boards with arrangement of the wires by the principle of the rectangular coordinate grid and with arrangement of the VPL IC cases in regular rows.

It is expedient to place the elements which must be switched simultaneously in different cases.

When placing the VPL IC cases on the board it is necessary to connect the simultaneously switching circuits to different buses of the feed layout. In the case of connection to one bus it is necessary to separate them by circuits switching at different points in time.

The width of the wires must be within the limits of 0.13-0.50 mm. For conductors of this width the wave impedance will be within the limits of 75-100 ohms for a board with internal ground layer. This range of wave impedances is entirely acceptable for boards with VPL IC.

The maximum admissible length of the parallel wires with spacing of 0.5 mm for which the stray pickups do not exceed the switching threshold of the VPL IC is equal to 1,800 mm. The number of simultaneously switched valves connected to these wires can in this case reach 10.

Increasing the length of the parallel wires to 3,000 mm is permissible with an increase in spacing of the wires to 1.5 mm or decreasing the number of simultaneously switched wires to 3.

In order to decrease the crosstalk between parallel long lines it is necessary to install shorter ones.

On a two-sided printed circuit board a wire 3,000 mm long will create a capacitive load of about 180 picofarads for the logical element, which causes signal propagation delay of $t^{0.1}_{del\ p}$ = 200 nanoseconds, $t^{1.0}_{del\ p}$ = 100 nanoseconds.

The information communication lines between the boards can be made using panel mounting or dense-packed point-to-point wiring.

Panel mounting can be structurally in the form of a printed circuit board or panel having shielding coating on the wiring side. The shield must be connected to the "ground" bus of the equipment and the "ground" buses of the printed circuit boards. The length of the communication lines on the panel mounting is established considering the length of these lines on the board.

Communication lines to 10 m long can be made as unmatched cabled pairs.

It is recommended that communication lines more than 10 m long and also the communication lines going beyond the units be made as matched cabled pairs or coaxial cable with wave impedance ρ = 75 or 100 ohms.

The return wires of the cabled pairs or the braiding of the coaxial cable are grounded on two ends.

It is recommended that the commutation communication lines (the lines between switches, toggle switches, relay contacts and microcircuits) be made of shielded wire.

Laying the information, commutation and display communication lines in one set of bunched conductors is not permissible.

K511TV1, K511IYe1, K511ID1, K511LI1 Microcircuits. The K511LI1 microcircuit can be used to control the display elements (incandescent tubes or semiconductor light sources).

The operation of the K511LI1 microcircuit as a control unit for the display elements is illustrated in Figure 5-52. The recommended type of tube is the KM-12-90.

The JK-type K511TV1 trigger belongs to the category of universal triggers inasmuch as it is possible to obtain circuits that perform the functions of RS, T and D triggers on the basis of it.

It is possible to explain the operating principle of the trigger using the functional diagram presented in Figure 5-53.

The elements D_3 and D_4 are circuits that generate peak voltages of limited duration with corresponding combination of voltages at the trigger inputs and feed of the negative gradient to the complementing input. The inputs I_1, I_2 and I_3 are such that when the low-voltage level occurs on at least one of them, the peak voltage generation is impossible.

The D_1, D_2 elements are basic memory elements of the trigger.

The circuit operates as follows.

Let us propose that in the initial state the logical one voltage is present at the output Q, and the logical zero voltage at the output $\overline{Q}$. If the logical one level is present at the inputs J, K and $\overline{S}$, the generator D_4 generates a peak voltage for there is high level at all of its inputs at the same time as the generator D_3 does not respond on arrival of a pulse at input C, for at its input connected to the output Q there is a low level. On feeding a pulse to the input C on one of the inputs of the valve D_2, a negative voltage pulse appears which switches off the valve. The valve D_1 is switched on in this case.

When the next pulse arrives, analogous processes take place except the trigger outputs change roles (the logical zero voltage for Q, the logical one voltage for $\overline{Q}$). Thus, in the given case the trigger operates in the frequency division mode (the counting mode).

If there is a low level at the inputs J and K, simultaneously, both generators will fail to operate, and the negative gradient at the complementing input will not cause the trigger to be thrown.

Finally, if the logical zero state occurs at the input J, and the logical one state at the input K or vice versa, the given information will be transmitted to the output when the counting pulse reaches the input.

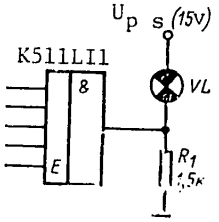


Figure 5-52. Display circuit with the application of an incandescent tube.

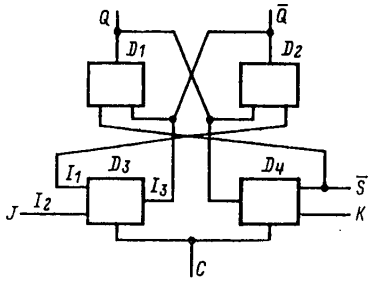


Figure 5-53. Electrical functional diagram of the JK trigger.

The effect of the asynchronous input also is obvious from the functional diagram. If there is a low-voltage level at the input $\overline{S}$, there will be a high level at

the output $\overline{Q}$; in this case under the effect of the counting pulses the D_4 generator will not generate pulses, and the trigger retains its state.

The K511IYe1 microcircuit is a four-bit binary-to-decimal counter constructed from JK triggers. Permitting asynchronous preliminary setting and being a multifunctional system, it can be used in the most numerous spheres of application of computers and industrial automation units. In the counter provision is made for parallel input of information when operating in the counting mode, and it is also possible to set a logical zero in all bits and set a logical one bit by bit. The circuit has two synchronous inputs of the circuit performing the function of logical multiplication, the input for setting the counter to zero ($\overline{R}$) and four preset inputs ($\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$, $\overline{S}_4$) having the possibility of setting any of the triggers to one.

For synchronous operation the counting pulse passes through the AND circuit to the inputs of three triggers simultaneously. The low-order bit trigger changes its state after arrival of the next pulse at the complementing input, and the rest of the triggers retain their states only if there is a high-voltage level on all inputs of the controlling AND circuits.

Information is transmitted to the basic trigger in the presence of a positive voltage drop on the input C_1 if there is a high level on the input C_2. Then when the negative drop reaches the input the information is transmitted to the auxiliary trigger and then to the output.

For asynchronous operation in order to set the trigger to zero it is necessary to feed a low level to the clearing input $\overline{R}$, and to set a one in any of the bits, to the corresponding setting input. The presence of setting inputs $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$, $\overline{S}_4$ permits setting any number from 0 to 9. On the basis of the 10-step counter K511IYe1 it is possible to construct several versions of counters which can count to a lower number. For this purpose it is necessary to feed the signals from the output at which the count ends (at the logical one outputs) through the AND-NOT element or NOT to the clearing bus, that is, to input 8, and the count stops. Examples of this construction are presented in Figure 5-54.

The K511ID1 microcircuit is a decoder that decodes binary-decimal code to decimal with high-voltage outputs.

The circuit diagram of the K511ID1 decoder for operation on a gas discharge tube is presented in Figure 5-55. The output signals from the high-voltage transistors go to the cathodes of the gas-filled digital tubes.

In the input circuits of the decoder the VPL IC are used at the same time as all of the "internal" logic is constructed from elements of resistive-transistor logic. This is done from the conditions of economicalness of the circuit and the possibility of matching with the K511 series circuits. The presence of the VPL IC elements at the input also determines noiseproofness of the decoder circuit with respect to input interference.

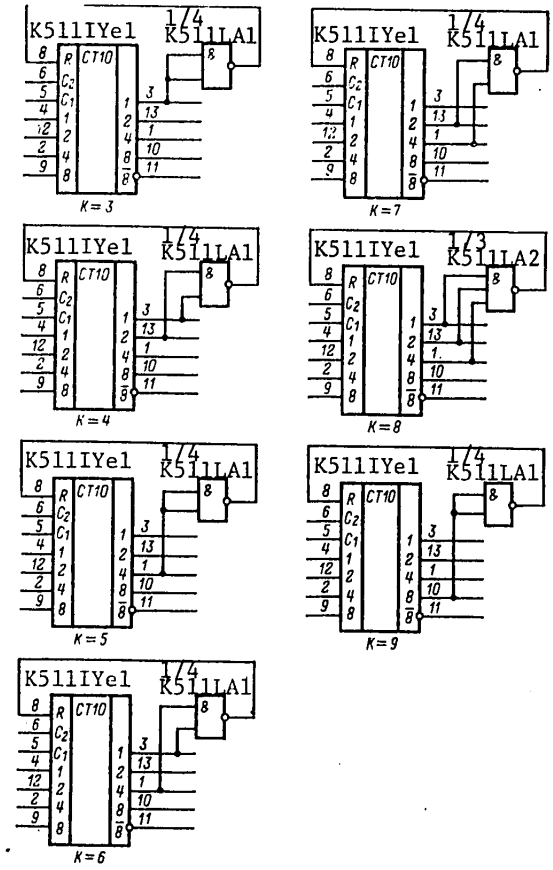


Figure 5-54. Functional counter system with counting modulus from 3 to 9 constructed on the basis of the K511IK1 circuit.

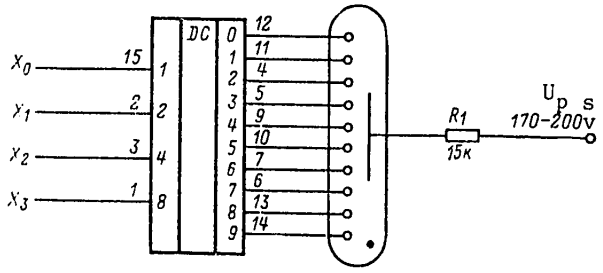


Figure 5-55. Circuit diagram of the K511ID1 microcircuit of the decoder for operation on an IN-type gas discharge tube.

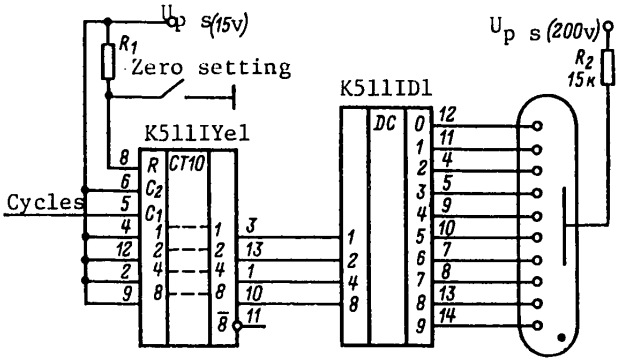


Figure 5-56. Circuit diagram of the K511IYe1 and K511ID1 microcircuits of the decoder and counter.

On feeding a redundant code to the decoder input, one or two outputs of the decoder respond.

In order to exclude the possibility of obtaining a redundant code at the information output, it is necessary to use a decoder with binary-decimal K511IYe1 counter according to Figure 5-56.

The decoder can operate with cold glow tubes having a cathode current to 7 milliamps.

Recommendations With Respect to Matching the K511 Series Microcircuits With Other Series. The presence in the K511 series of microcircuits of level conversion K511PU1 and K511PU2 permits matching of the given series with the TTL-type microcircuits, for example, K155 series, on the basis of which central computing and control units can be executed. Thus, a system can be realized which has high noiseproofness with respect to input and output, having high speed, small size and weight.

The diagram of the application of the VPL IC for the given case is presented in Figure 5-57.

In order to convert the logical levels of the zero and one signals of the VPL IC to logical zero and one levels of the TTL, DTL IC, the K511UP1 microcircuit is used which consists of the ordinary VPL valve, the output stage of which is executed with open collector. The signal amplitude at the converter output depends on the voltage fed to the auxiliary resistor included in series with the output transistor.

For conversion of the logical voltage levels of the K511 series microcircuits to logical levels of the K155 series microcircuits an additional resistor is connected to the voltage source $U_{p\ s}$ = 5 volts (Figure 5-58, a, b).

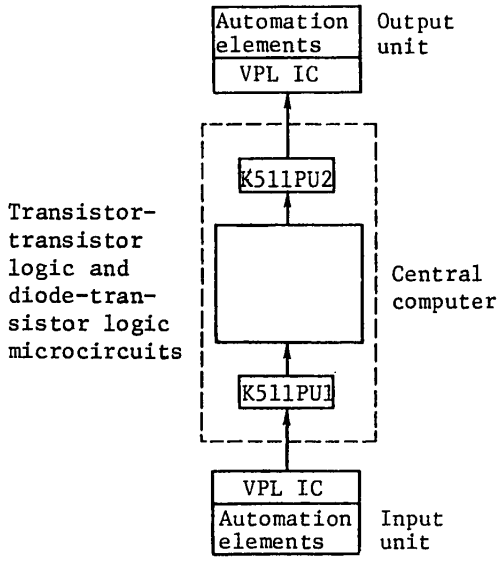


Figure 5-57. Diagram of the matching of the central computer with the peripheral devices based on VPL IC.

If the signal at the input of the K511PU1 element is equal to the logical one voltage, then the output transistor of the circuit is open and the load current flows through it (I^0_{out} = 12 mA for U^0_{out} = 0.45 volt).

For logical zero voltage at the input of the K511PU1 microcircuit the output transistor is closed and only the leakage current flows through it ($I^1_{out} \leq$ 0.1 mA).

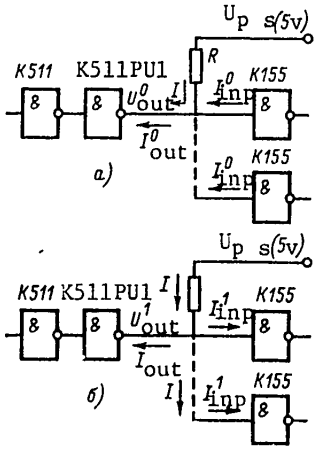


Figure 5-58. Circuit for matching the VPL IC with low-level series. a--For the state U^0_{out}; b--for the state U^1_{out}.

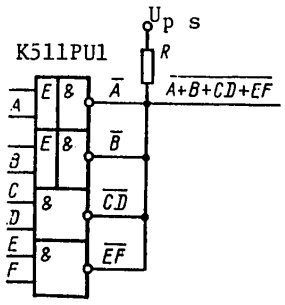


Figure 5-59. Output grouping circuit of the elements of the K511PU1 microcircuit for organizing the OR-NOT function.

The load resistance for logical zero at the output of the K511PU1 element must be selected so that the current I flowing through it summed with the current of the controlled elements ΣI^0_{inp} will be less than or equal to the current I^0_{out} flowing through the transistor of the K511PU1 element (Figure 5-58, a):

$$\Sigma I^0_{inp} + 1 \leq I^0_{out};\ I = (U_{p\ s} - U^0_{out})/R;\ R - (U_{p\ s} \geq U^0_{out})/(I^0_{out} - \Sigma I^0_{inp})$$

At the same time for logical one at the output of the K511PU1 (U^1_{out}), the resistance R must be not very large in order to ensure a current flowing into the controlled elements (Figure 5-58, b):

$$I \geq I^1_{out} + \Sigma I^1_{inp};\ I = (U_{p\ s} - U^1_{out})/R;\ R \leq (U_{p\ s} - U^1_{out})/(I^1_{out} + \Sigma I^1_{inp}).$$

The outputs of the K511PU1 elements can be combined for realization of the AND OR-NOT function (Figure 5-59). Here the rated value of the resistor depends on the number of grouped outputs and the number of loads.

The values of the resistor R, depending on the number of grouped outputs and the fan-out are presented in Table 5-5.

Table 5-5

K155 Series ($U_{p\ s}$ = 5 v)			K511 Series ($U_{p\ s}$ = 15 v)		
$K_{group\ out}$	$K_{fan\text{-}out}$	R, kilohms	$K_{group\ out}$	$K_{fan\text{-}out}$	R, kilohms
45	1	1.0	50	1	1.5
30	3	1.0	30	10	2.4
15	5	1.5	10	20	6.8

In Figure 5-60 the organization of the OR function at the output of the K511PU1 element controlled by other elements of the K511 series is illustrated.

The input and output pulse diagrams when matching the K511 series with the K155 series are presented in Figure 5-61.

The conversion of the voltages of the logical zero and one levels of the TTL IC to voltages of the logical zero and one levels of the VPL IC is accomplished using the K511PU2 converter. The diagrams of these valves differ from the standard ones in that the Zener diode in it is replaced by an ordinary diode included in the forward direction for reduction of the voltage passing through this diode. The circuit for conversion of the logical levels is presented in Figure 5-62.

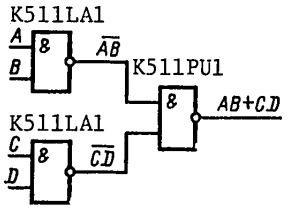


Figure 5-60. Diagram of the organization of the OR function.

When matching the K155 series elements with the open collector output (K155LA7, K155LA8) and K511PU2, the resistor R is connected to the collector. The resistor R is taken from the relation indicated in Figure 5-63, a, b.

The remaining elements of the K155 series are matched with the VPL IC of the K511 series without additional load. The fan-out for the IC of the K155 series is equal to 30 when matching with the K511PU2 microcircuit.

The diagrams of the input and output pulses when matching K155 series with K511 series are presented in Figure 5-64.

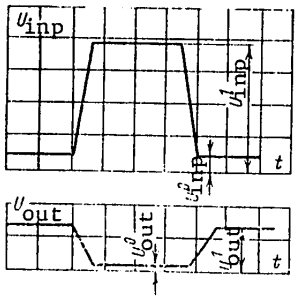


Figure 5-61. Input and output pulses when matching the K511 and K155 series microcircuits for the K511PU1 microcircuit. U^0_{inp}--the logical zero voltage at the input ($U^0_{inp} \leq 1.5$ volt); U^1_{inp}--the logical one voltage at the input (10 volt $\leq U^1_{inp} \leq 12$ volts); U^0_{out}--logical zero voltage at the output ($U^0_{out} \leq 0.45$ volt); U^1_{out}--logical one voltage at the output ($U^0_{out} \geq 4.2$ volts).

Special Cases of the Uses of Microcircuits. The K511 series microcircuits can be used when operating on a line with distributed parameters (a long line).

Reliable switching of the receiving circuit is ensured on transmission of a signal over a coaxial cable with wave impedance ρ = 100 or 75 ohms up to 300 m long.

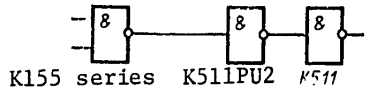


Figure 5-62. Circuit for matching the TTL microcircuits with the VPL IC.

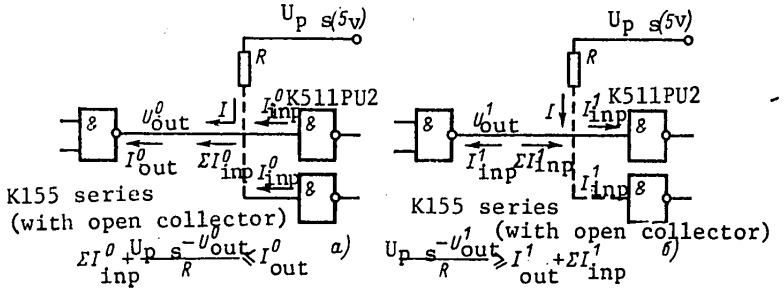


Figure 5-63. Matching the elements with the open collector output with other elements. a--For the U^0_{out} state; b--for the U^1_{out} state.

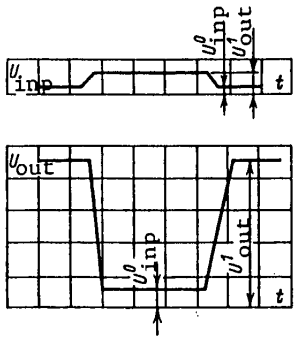


Figure 5-64. Input and output pulses for matching the K155 and K511 series for the K511PU2 microcircuit. U^0_{inp}--logical zero voltage at the input ($U^0_{inp} \leq 0.4$ volt); U^1_{inp}--logical one voltage at the input ($U^1_{inp} \geq 2.4$ volts); U^0_{out}--logical zero voltage at the output ($U^0_{out} \leq 1.5$ volt); U^1_{out}--logical one voltage at the output ($U^1_{out} \geq 12$ volts).

For transmission of signals over a long line the K511LI1 microcircuit is used, the high output current of the logical zero (I^0_{out} = 100 mA) of which ensures fast charging of the spurious capacitance of the cable, which leads to less stretching of the trailing edge of the pulse at the cable output.

The K511LA1, K511LA2, K511LA3, K511LA4, K511LA5, K511PU1, K511LI1 microcircuits can be used as the receiving circuits.

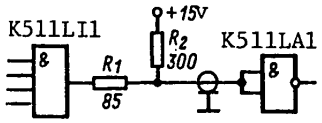


Figure 5-65. Matching circuit for transmission of a signal over a coaxial cable with wave impedance ρ = 100 ohms.

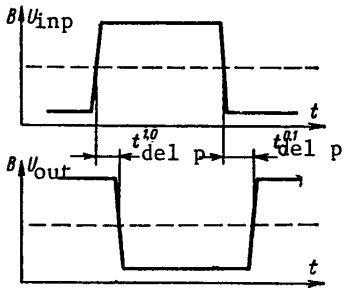


Figure 5-66. Input and output pulse diagrams for signal transmission over a coaxial cable ℓ = 200 m long with wave impedance ρ = 100 ohms.

On transmission of the signal over a coaxial cable with wave impedance ρ = 100 ohms, the resistor R_1 = 85 ohms is used for matching, which is installed at the output of the K511LI1 control circuit.

An example of matching with signal transmission over the coaxial cable with wave impedance ρ = 100 ohms and grounded braiding is presented in Figure 5-65. The input and output pulse diagrams for the given matching with coaxial cable length of ℓ = 200 m are presented in Figure 5-66.

The signal propagation delay time with respect to the pulse front $t^{1.0}_{del\ p}$ = 0.9 microsecond, with respect to decay $t^{0.1}_{del\ p}$ = 1.1 microseconds for pulse frequency f = 10 kilohertz.

On transmission of the signal over a coaxial cable with wave impedance ρ = 75 ohms, the resistor R_1 = 60 ohms is used for matching. An example of matching is presented in Figure 5-67. The signal propagation delay time for a cable length of ℓ = 100 m with respect to the pulse front $t^{1.0}_{del\ p}$ = 0.8 microsecond, with respect to decay $t^{0.1}_{del\ p}$ = 1.0 microsecond for a pulse frequency f = 10 kilohertz.

The noiseproofness of the given system when transmitting signals over a coaxial cable with wave impedance ρ = 100 ohms decreases as a result of a drop in logical one level (U^1_{out} = 11.2 volts) and a rise in logical zero level (U^0_{out} = 3.8 volts) as a result of the voltage drop on the matching resistors with power supply voltage $U_{p\ s}$ = 15 volts.

The noiseproofness with respect to positive interference with logical zero level at the input of the receiving circuit is: $\Delta U^{+}_{noise} = 6.5 - 3.8 = 2.7$ volts.

The noiseproofness with respect to negative interference with logical one level at the input of the receiving circuit is: $\Delta U^{-}_{noise} = 11.2 - 7.5 = 3.7$ volts.

When using the coaxial cable or ungrounded cabled pair for signal transmission over two channels in one direction (for example, over the central core and the braiding) sinusoidal oscillations arise in the lines connected with reflection of the cophasal wave, Figure 5-68. For matching the given system resistors are used, the magnitude of which is $R = \rho - R_{out}$, where ρ is the wave impedance of the line; $R_{out} = 15$ ohms is the output impedance of the VPL IC K511LI1 for logical zero at the output.

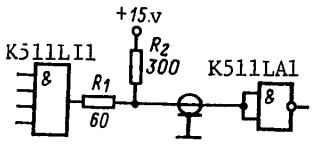


Figure 5-67. Matching circuit for signal transmission over a coaxial cable with wave impedance $\rho = 75$ ohms.

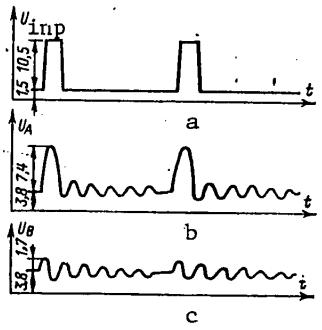


Figure 5-68. Diagrams of the input signal (a), the signal at point A of the transmitting line (b), crosstalk at point B (c) using a cable with $\rho = 100$ ohms, $\ell = 200$ m long.

An example of matching with signal transmission over the central core and the braiding of a coaxial cable of length $\ell = 300$ m with wave impedance $\rho = 100$ ohms is presented in Figure 5-69.

The signal propagation delay time with respect to the pulse front $t^{0.1}_{del\ p}$ = 200 nanoseconds, with respect to decay $t^{1.0}_{del\ p} = 3$ microseconds for a pulse frequency of $f = 10$ kilohertz.

When using a cabled pair for a multicore cable, the signals over the lines (cores) which are transmitted in the opposite directions must be considered as cophasal Z_{em} and differential Z_{dm} wave impedance. The differential wave impedance Z_{dm} is connected with the lines under equal but opposite potentials over

which an equal current flows, but in opposite directions. The impedance of the given system is denoted as Z_{00}. In the given case $Z_{dm} = 2Z_{00}$.

The method of matching the cophasal and differential wave impedances consists in the following:

1. The lines "A" and "B" over which the signals will be transmitted in opposite directions are matched with the cophasal wave impedance Z_{em} by the resistor equal to Z_{em}.

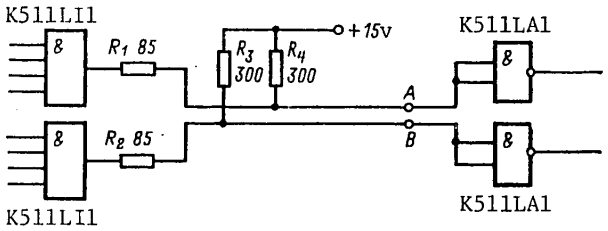


Figure 5-69. Matching circuit for tranmission of cophasal signals over a coaxial cable with wave impedance ρ = 100 ohms.

2. The line "A" is excited, and the magnitude of the crosstalk on the line "B" is measured.

3. Let us connect the cophasal impedance of the line Z_{oe} to the differential impedance:

$$Z_{00} = \frac{U_B}{U_A} = \frac{Z_{oe} - Z_{00}}{Z_{oe} + Z_{00}};$$

$$Z_{00} = \frac{U_A - U_B}{U_A + U_B} Z_{oe},$$

where U_A is the voltage on the line "A"; U_B is the voltage on the line "B."

4. Let us calculate the magnitude of the resistor matching the differential signal on parallel inclusion with $2Z_{em}$:

$$R = \frac{2Z_{dm}Z_{em}}{2Z_{em} - Z_{dm}},$$

where $Z_{dm} = 2Z_{00}$.

An example of matching a coaxial cable with wave impedance ρ = 100 ohms, length ℓ = 200 m, the signals over the central core and the braiding of which are transmitted in opposite directions, is presented in Figure 5-70. The cophasal signal is matched by the resistors $R_1 = R_5 = 85$ ohms.

The resistance of the resistor R_3 matching the differential signal is calculated by the method indicated above: a signal of 11.2 volts transmitted over the cable braiding induces crosstalk of 1.7 volts in the central core.

The differential impedance of the line is:

$$Z_{ou} = \frac{11,2 - 1,7}{11,2 + 1,7} \cdot 100 \approx 74 \text{ ohms}.$$

The resistance of the resistor matching the different signals is:

$$R_n = \frac{2 \cdot 2 \cdot 74 \cdot 100}{2 \cdot 100 - 2 \cdot 74} \approx 570 \text{ ohms}.$$

For transmission of signals over a long line the K511LA1, K511LA2, K511LA4 microcircuits can also be used. As the receiving circuits analogous microcircuits can be used: factors limiting the length of the transmission line are small output logical zero current of the given VPL IC (I^0_{out} = 12 mA) and cable capacitance which create long pulse delay with respect to the trailing edge at the transmission line output.

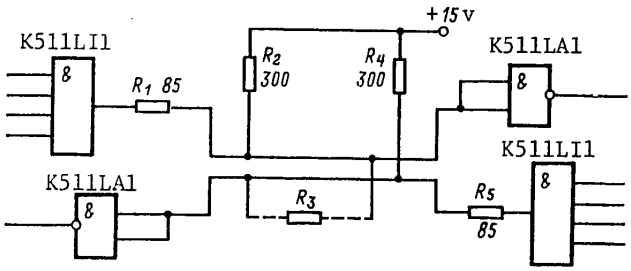


Figure 5-70. Matching circuit using a coaxial cable with ρ = 100 ohms for transmission of signals in opposite directions.

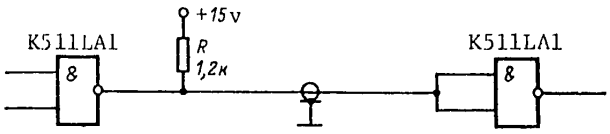


Figure 5-71. Matching circuit for signal transmission over a coaxial cable.

An example of signal transmission over a coaxial cable with wave impedance ρ = 75 ohms, length ℓ = 100 m is presented in Figure 5-71. The signal propagation delay time with respect to the pulse front $t^{0.1}_{del\ p}$ = 1 microsecond, the pulse decay delay $t^{1.0}_{del\ p}$ = 3 microseconds.

Increasing the Signal Propagation Delay. The signal propagation delay can be used to decrease the sensitivity of the circuit to dynamic (pulsed) interference.

Figure 5-72, a, gives the diagram of the use of an expanding input to increase the signal propagation delay time. The dependence of the propagation delay on the magnitude of the capacitance of the capacitor for the K511LA3, K511LA4 microcircuits is presented in Figure 5-72, b.

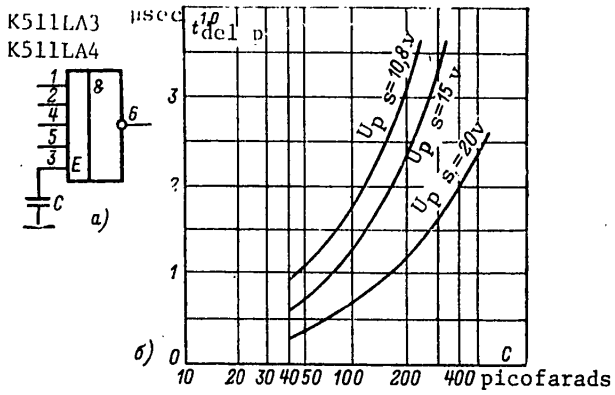


Figure 5-72. Example of the use of an expanding input to increase the signal inclusion time.

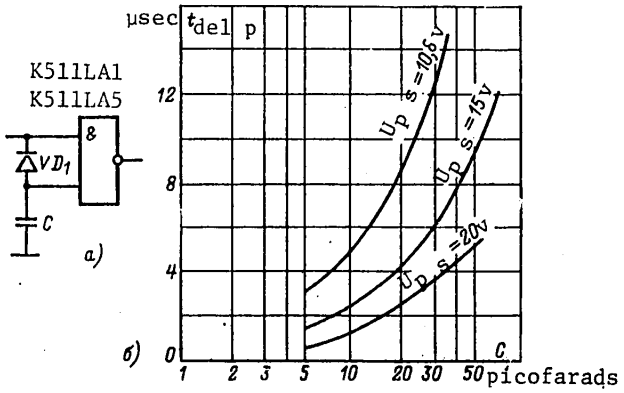


Figure 5-73. Example of the use of the inputs of the K511LA1 and K511LA5 microcircuits to increase the propagation delay time on inclusion.
VD_1--Semiconductor diode types KD521, KD522B.

The type of capacitor is not regulated.

In the absence of an expansion input for increasing the signal propagation delay time on connecting ($t^{1,0}_{del,\ p}$) the diagram presented in Figure 5-73, a can be used.

The dependence of the propagation delay for the K511LA1 microcircuit on the capacitance using the KD521A or KD522B diode is presented in Figure 5-73, b.

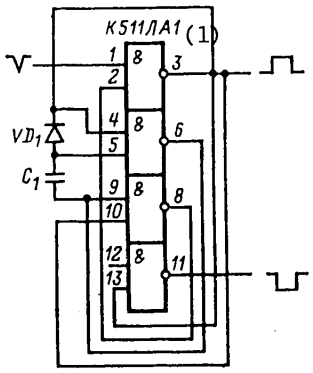


Figure 5-74. Diagram of functional enlargement of the pulse duration. VD_1 -- semiconductor diode types KD503, KD521A, KD522B.
Key:
1. K511LA1

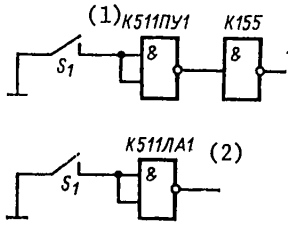


Figure 5-75. Circuit diagram for connecting the K511 series microcircuits to contact relays.
Key:
1. K511PU1
2. K511LA1

The pulse duration enlargement circuit is presented in Figure 5-74. The circuit is controlled by a signal of negative polarity

$$t_{del,\ p} = 400\ C,$$

where $t_{del,\ p}$ is the signal propagation delay, milliseconds; C is the capacitance of the capacitor, microfarads.

The K511 series microcircuits can be used in circuits with relays operating on 15 volts. In such circuits the signal from the relay can be transmitted a distance of up to 20 meters (Figure 5-75).

Operation of the K511LI1 Microcircuit as a Power Valve. Many areas of industrial application require the use of powerful valves such as, for example, the valve for operation (switching) with relatively high current levels and actuating tubes and relays. For this purpose the K511LI1 microcircuit can be used. It consists of two expansion valves with four inputs. In essence this circuit is identical to the base valve circuit with the same addition that a powerful inverting amplifier is added at the output.

The output transistor of the K511LI1 microcircuit provides for operation with high current level to 100 milliamps. With this current $U^0_{out} \leq 1.5$ volts as in

ordinary valves. At the same time this output device permits realization of the OR function at the output.

The circuit diagram for connecting the relay to the output of the microcircuit is presented in Figure 5-76.

Construction of the Functional Units of the Equipment. The realization of logical functions, except the AND-NOT function realized directly by the elements of the series K511 microcircuit is realized by combining the AND-NOT elements in the corresponding way.

Inasmuch as there are always several versions of realization of the function, when putting the circuit together it is necessary to select the version with the smallest number of elements in the circuit. In Table 5-6 examples are presented for the realization of various functions.

The AND-OR-NOT function is realized from the K511 series elements with passive collector input (K511LA3, K511LA5) by grouping the outputs of several elements. Here if up to 3 elements are grouped, the fan-out is equal to 10. On connecting each subsequent element the fan-out decreases by 2.5, that is, $K_{fan-out}=10-(K_{group,\ out}-3)2.5$, where $K_{group,\ out}$ is the number of grouped elements with respect to output. For organization of one function or another, elements of the series are selected with respect to the number of inputs corresponding to the realized function. If not all of the inputs are used in the element, the three inputs of the AND circuit must be grouped with one of the signal inputs within the limits of the load capacity of the controlling element or they are connected to a power supply or to the outputs of unused inverters (within the limits of the load capacity of the latter), the inputs of which are grounded.

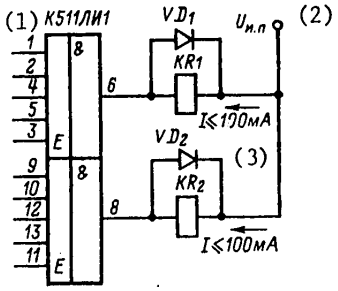


Figure 5-76. Control circuit for connecting the relay

Key:
1. K511LI1
2. $U_{p.s}$
3. I≤100 milliamps

Use of Expansion Inputs. In order to increase the number of inputs of microcircuits, expansion inputs are used which are available in the K511LA3, K511LA4, K511LI1, K511PU1 type circuits. It is possible to connect diodes and diode matrices to the expansion input (the D18, 2D502, D220, and KD522 diodes are recommended).

In addition, it is possible to increase the number of inputs, connecting the expansion input of two valves of the microcircuits.

In the absence of an expansion input, an increase in the load capacity with respect to the input is achieved on connecting the external diodes and auxiliary resistor R_{01} to any of the standard inputs of the circuit (Figure 5-77).

The magnitude of the resistor R_{01} must be determined in accordance with the required speed of the circuit. The magnitude of the signal propagation delay will increase with an increase in the value of R_{01}.

For given expansion of the load capacity with respect to input, noise resistance on the low level is reduced. As is obvious, the logical zero input voltage of the given circuit will be decreased as a result of the voltage drop on one diode. Therefore the noiseproofness on the low level will be approximately equal to the following: $U^0_{inp,\ max}-U_{VD}-U^0_{out}=6.0-0.8-1.5=3.7$ volts.

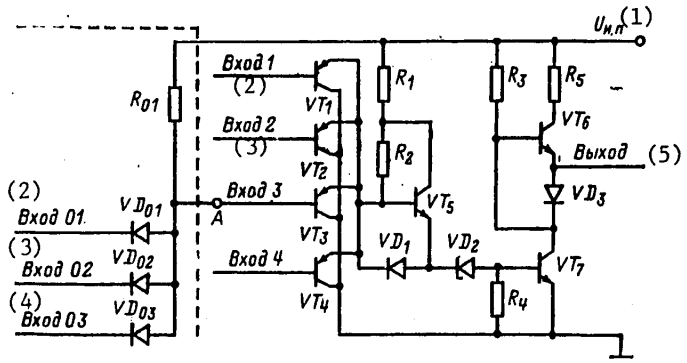


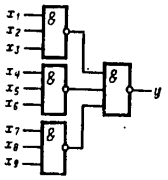
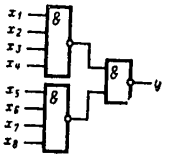
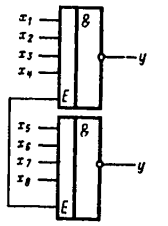
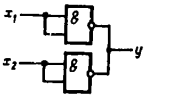
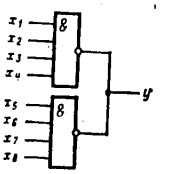
Figure 5-77. Diagram of the expansion of the load capacity with respect to input in the absence of expander input

Key:
1. $U_{p.s}$
2. Input 01
3. Input 02
4. Input 03
5. Output

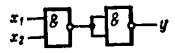
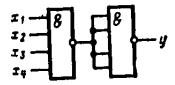
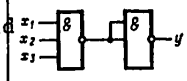
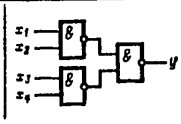
Examples of Constructing Triggers from K511 Series Elements. It is possible to construct a number of basic triggers used in integrated circuit engineering on the basis of the K511 series logical elements performing the AND-NOT function.

Figure 5-78 shows the construction of an asynchronous RS-trigger. The input $\overline{S}$ is the ones input, and the input $\overline{R}$ is the zero input, that is, the trigger is set to the state 1 (Q=1) by the signal $\overline{S}$=0, and to the state 0 (Q=0) by the signal $\overline{R}$=0. The combination of signals $\overline{R}=\overline{S}=0$ for the given trigger is forbidden.

Table 5-6. Realization of Various Functions on the Basis of Series K511 Integrated Circuits

Function	Type of microcircuit	Functional diagram
$y = x_1x_2x_3 + x_4x_5x_6 + x_7x_8x_9$	4/3 K511LA2	
$y = x_1x_2x_3x_4 + x_5x_6x_7x_8$	K511LA4 and 1/4 K511LA1	
$y = \overline{x_1x_2x_3x_4} \cdot \overline{x_5x_6x_7x_8}$	K511LA4 or K511LA3	
$y = \overline{x_1 + x_2}$	1/2 K511LA5	
$y = \overline{x_1x_2x_3x_4 + x_5x_6x_7x_8}$	K511LA3	

[Table 5-6, contd]

Function	Type of microcircuit	Functional diagram
$y = \overline{x_1 x_2}$	1/2 K511LA1 or 1/2 K511LA5	
$y = x_1 x_2 x_3 x_4$	K511LA4 or K511LA3	
$y = x_1 x_2 x_3$	1/3 K511LA2 and 1/4 K511LA1	
$y = x_1 x_2 + x_3 x_4$	3/4 K511LA1 or 3/4 K511LA5	

A synchronous RS-trigger is presented in Figure 5-79. In contrast to the asynchronous trigger, the cycled RS-trigger has additional comparison circuits at the input of each arm, the first inputs of which are grouped and are the cycle pulse inputs, and the second inputs of the comparison circuits are information inputs for writing "1" (S_c) and "0" (R_c). Thus, information coming to the inputs R_c and S_c can be transmitted to the trigger itself only on arrival of the cycling pulse. For a signal combination SC=1 the trigger is set to the state Q=1. On combining the signals RSC=1 the trigger has an undefined state, that is, the given combination of signals for the cycled RS-trigger is forbidden.

The realization of a D-type single-cycle trigger controlled by the cycle pulse level is illustrated in Figure 5-80. Here the input D is the information input, and the input C is the cycle input. For C=1 the information is always entered in the trigger which was at the input D before the arrival of the cycle pulse. For operating stability of the circuit it is necessary that the information at the input not change with time of effect of the cycle pulse.

Construction of Single-Cycle Triggers Based on the K511 Series Elements. The single-cycle triggers used in integrated circuit engineering are basically executed on the basis of the RS, D and JK type triggers having the properties of internal delay. In triggers of internal delay the new information is set at the trigger output only after completion of operation of the cycle pulse. This important property of triggers with internal delay makes it possible to use them as the basis for building high-speed digital information processing devices, for the information read and write process can be combined in one cycle (for example, the operating conditions of the address counter of a digital computer, and so on).

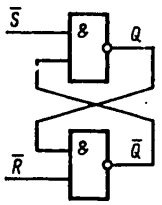


Figure 5-78. Functional diagram of asynchronous RS-trigger

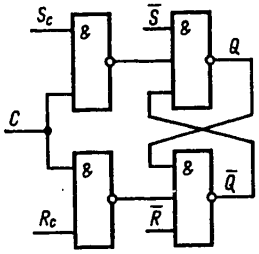


Figure 5-79. Functional diagram of synchronous RS-trigger

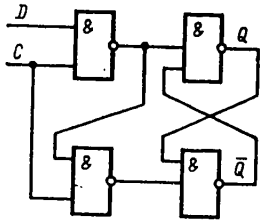


Figure 5-80. Functional diagram of cycled D-trigger

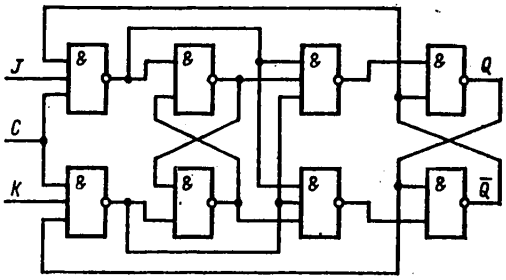


Figure 5-81. Functional diagram of the JK_t-trigger

Triggers having the properties of internal delay are denoted by the subscript t along with the notation of the type of trigger.

It is possible to isolate three basic systems of constructing single-cycle counting triggers:

The MS system;

A system of three triggers (basic and two commuting);

System using memory elements.

According to the MS system the trigger units are constructed, as a rule, on the basis of the RS and D-type triggers.

Figure 5-81 shows the construction of the JK_t-type trigger executed by MS system with forbidding couplings. The given circuit is realized on the basis of the RS-trigger units by connecting the outputs Q and $\overline{Q}$ to the inputs R and S, respectively, and adding two inputs J and K parallel to the inputs S and R. For C=0 the system is in the "0" state independently of the signal level at the inputs J and K.

For J=0 and C=K=1, the trigger is set to the state Q=0, and for J=C=1 and K=0, to the state Q=1.

The JK_t-type triggers are multifunctional triggers, for RS_t, D_t and T_t triggers can be built on the basis of them. The method of constructing other types of triggers based on JK_t-triggers is illustrated in Figure 5-82.

The D_t trigger executed by the three trigger system is illustrated in Figure 5-83. The elements D_5 and D_6 form the basic trigger, and the elements D_1, D_2 and D_3, D_4 form the right and left switching triggers, respectively.

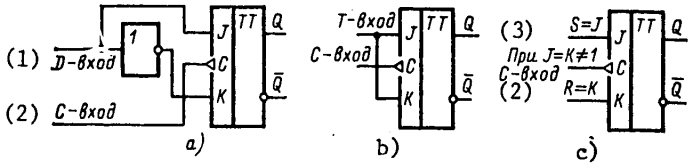


Figure 5-82. Functional diagrams of synchronous triggers executed on the basis of JK-triggers.
a -- D_t; b -- T_t; c -- RS_t.

Key:
1. D-input
2. C-input
3. For J=K≠1

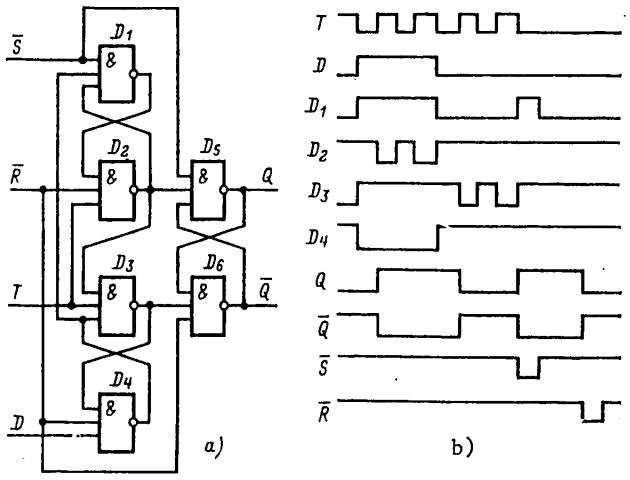


Figure 5-83. Functional diagram (a) and operating time diagram (b) of the D_t-trigger

In the absence of cycle pulses the trigger switches to the state corresponding to the information at the input. For D=1 the state at the output Q-1; for D=0 the state at the output Q=0.

For operation of the circuit in the T_t-trigger mode it is necessary to connect the output of the basic trigger $\overline{Q}$ to the input D, and to feed the count pulses to the input T. This type of T_t-trigger constructed on the basis of the D_t-trigger is presented in Figure 5-84.

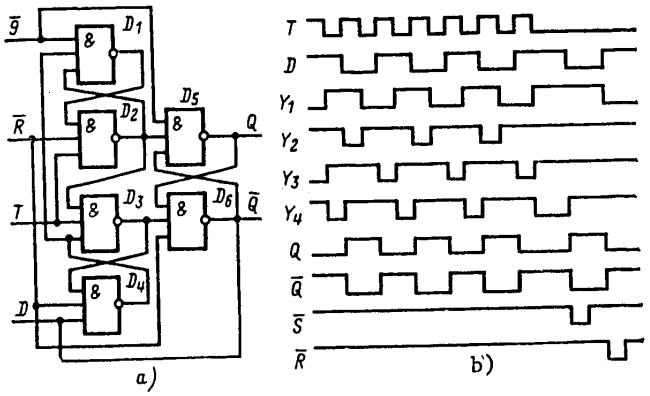


Figure 5-84. Functional diagram (a) and operating time diagram (b) of the T_t-trigger constructed on the basis of the D_t-trigger

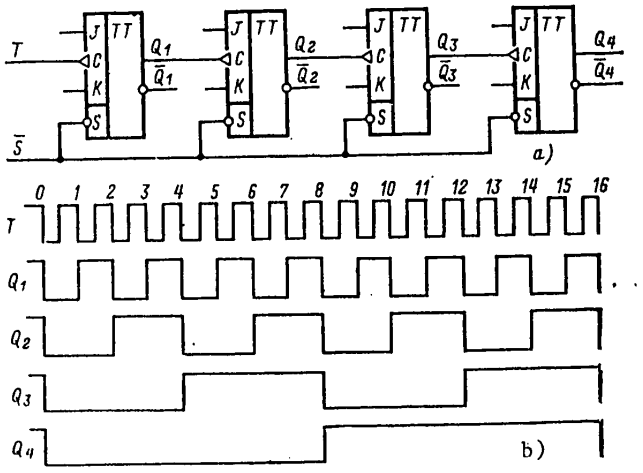


Figure 5-85. Functional diagram (a) and operating time diagram (b) of a binary counter based on JK_t-triggers

Construction of Counters Based on JK_t-Triggers. The counting trigger is the simplest counter realizing mod 2 counting of pulses. Connecting several counting triggers in a defined way it is possible to obtain a multibit counter circuit.

Figure 5-85 shows the functional diagram and the operating time diagram of a binary counter based on JK_t-triggers with direct coupling. The controlling signals for the high-order bits of the counter are the signal levels with information inputs of the low-order bits.

The maximum magnitude of the setup time $t_{setup,\ max}$ in the series type counters is determined by the total delay of the series transmission of the information from the low-order bit to the high-order bit of the counter $t_{setup,\ max}=N\tau_t$, where N is the number of bits of the counter; τ_t is the switching delay of the JK-trigger after completion of the counting pulse (τ_t=600 nanoseconds).

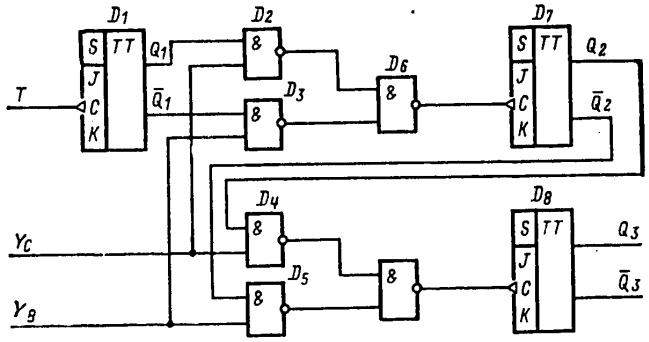


Figure 5-86. Functional diagram of a reversible series type counter

Considering the duration of the counting pulse we obtain:

$$T_{\text{сч}}=\tau_{\text{п}}+N\tau_t;\quad f_{\text{сч}}=\frac{1}{\tau_{\text{п}}+N\tau_t},$$

(1) (1)

Key: 1. count

where $\tau_{\text{п}}$ is the counting pulse duration; T_{count} is the counting pulse repetition period.

During operation of the series counter in the frequency divider mode, that is, when the information is picked up from the output of the high-order bit, the loading frequency of this operation will be determined by the limiting switching frequency of the counting trigger of the first bit, that is,

$$f_{\text{сч}}=\frac{1}{\tau_{\text{п}}+\tau_t}.$$

(1)

Key: 1. count

The diagram of a reversible counter based on counting triggers is presented in Figure 5-86.

This counter performs the operation of summation and subtraction of pulses depending on the resolving level on the controlling input. For the Y_C=1 state at the input summation of the pulses takes places; for the Y_B=1 state, subtraction of the pulses reaching the counting input takes place. The effect of the resolving levels is excluded simultaneously.

The circuit operates in the subtraction mode as follows: let the counter code correspond, for example, to the number 7≡111. The incoming counting pulse (T_{count}=1) sets the first bit to the state Q_1=0 (code 110). The "1" level from the output $\bar{Q}_1$ goes through the valve D_3 to the counting input of the second bit and prepares it for switching. The second counting pulse flips the first bit to the "1" state, and the second bit, to the "0" state (the code 101). The level Q_2=1 prepares the third bit of the counter for flipping, and so on.

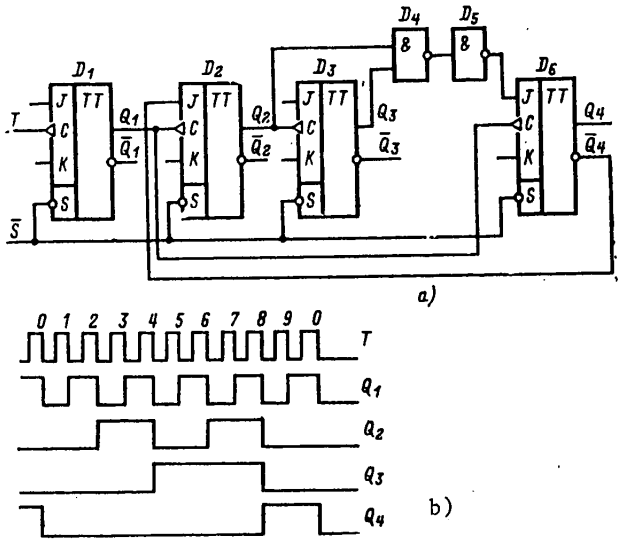


Figure 5-87. Functional diagram of a decimal counter based on JK_t-trigger (a) and operating time diagram (b)

Counters with Arbitrary Counting Factor. The above-investigated counters had a scaling factor of 2^N, where N is the bit number of the counter. The construction principle of the counters with $K_{count} \neq 2^N$ (K_{count}=3, 10, and so on) consists in excluding the "excess" stable states of the counter with K_{count}=2, that is, organizational of circuits preventing certain states.

The number of forbidden states for any counter can be determined from the following expression: $M=2^N-K_{count}$, where M is the number of forbidden states, K_{count} is the required counting factor; 2^N is the number of stable states of the binary counter.

Figure 5-87 shows the structure of a decimal counter based on JK_t-triggers. The pulses are counted to the ninth, inclusively in the corresponding counting order

0000, 0001, 0010, ..., 1001 exactly as in a binary countery (see Figure 5-85). After completion of the eighth counting pulse, the 1000 code is fixed in the counter, which leads to closure of the valve D_4 by the level $Q_3=0$ and setting a zero at the input of the J-trigger of the D_6 level.

After completion of the 9-th pulse, the code 1001 is established in the counter. After completion of the 10th pulse the trigger D_1 goes from state "1" to "0" and switches the trigger D_6 to the state "0"; as a result, after completion of the 10th pulse the counter is initialized (zeroed).

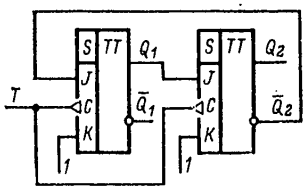


Figure 5-88. Diagram of a mod 3 counter based on JK-triggers

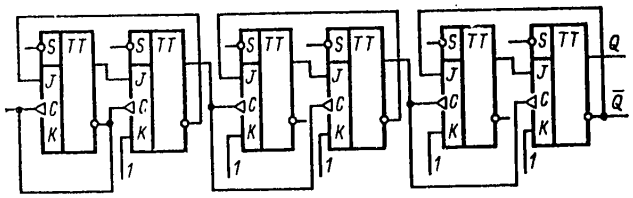


Figure 5-89. Functional diagram of a valveless counter using six JK-triggers with $K_{count}=27$

Structure of Counters Without Using Additional Elements. The basis for the construction of such counters is the principle of organizing the counting by an arbitrary modulus based on mod 2^N+1 counters, that is, counters permitting the counting modulus to be increased by one.

Let us consider the method of increasing the counting modulus by 1 in the example of the diagram in Figure 5-88 where a mod 3 counter based on JK_t-triggers is shown.

The initial state of the counter is the zero state ($Q_1=Q_2=0$). As a result, the first bit with respect to the input $J=\bar{Q}_2=1$ is prepared for switching to the state 1, and the second with respect to the input K=1, to confirmation of the zero state. After completion of the first counting pulse, the code 01 is set in the counter ($Q_1=1$; $Q_2=0$).

After completion of the second pulse the code 10 is set in the counter ($Q_1=0$; $Q_2=1$), inasmuch both JK_t-triggers will operate in the T-trigger mode. Before the arrival of the third counting pulse at the inputs J of both triggers a level

zero is present, and at the input K, a level 1. As a result, after completion of the third pulse both triggers are set to zero at the inputs (K=1).

For construction of the counter with $K_{count} \neq 2$, the required K_{count} must be represented in the form of a product of cofactors (groups), each of which consists of numbers that are a power of 2 or a power of 2 and additional units. For example, the number 27 can be represented in the form of the product of three cofactors, each of which is a power of 2 plus 1: $27=(2+1)(2+1)(2+1)$.

A diagram of the counter with $K_{count}=27$ constructed on the basis of the counte- with $K_{count}=3$ is presented in Figure 5-89.

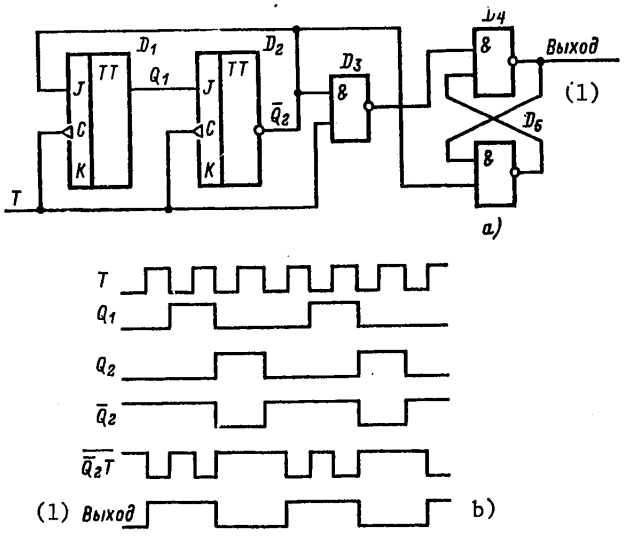


Figure 5-90. Functional diagram of the counter with scaling factor $K_{count}=3$ based on JK_t=triggers (a) and operating time diagram (b)

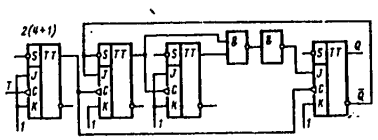
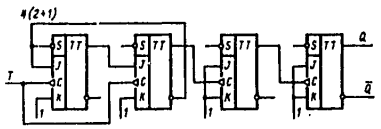
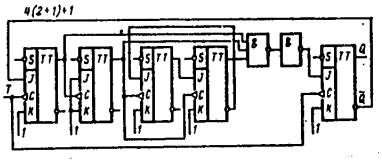
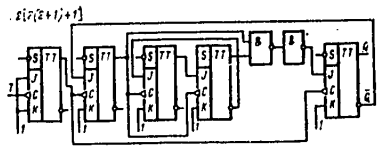
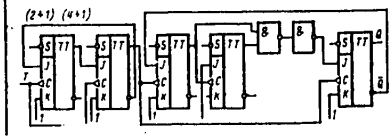
Key:
1. output

In Table 5-7, five counter circuits with K_{count} from 10 to 15, inclusively, are presented as an example. In column 4 we have the method of breakdown of each counter into groups.

In Figure 5-90 we have an example of the construction and the operating time diagram of a counter with scaling factor $K_{count}=3$ and shaping of a signal with duty factor 2 (meander) at the output based on the series K511 microcircuits.

If the unit trigger is used to increase the counting factor of several series-included groups and individual binary triggers by one, each of which in this case can be provisionally considered an individual group, then for a unit trigger the number of J-inputs must be equal to the number of all preceding groups, and it is necessary to connect the input 0 of all preceding groups of the counter to these inputs.

Table 5-7. Construction of Counters with Counting Factor 10, 12-15 Based on JK-Triggers

(1) Коэффициент счета	(2) Число триггеров в безвентильном счетчике, шт.	(3) Число триггеров в двоичном счетчике, шт.	(4) Функциональная схема
10	4	4	
12	4	4	
13	5	4	
14	5	4	
15	5	4	

Key:
1. Counting factor
2. No of triggers in the valveless counter, pieces
3. No of triggers in a binary countery, pieces
4. Functional diagram

Since in the K511 series JK-trigger there is a total of one input J, the signals from the preceding groups are fed to the J-input of the trigger through two series-included valves which in this case realize the AND function.

Construction of Multistable Triggers Based on K511 Series Microcircuits. Multistable triggers are used in different areas of digital engineering: as scaling circuits, frequency dividers, reversible counters, signal distributors, control units, and so on.

The three-stable trigger based on the AND-NOT elements is presented in Figure 5-91. The trigger is switched to any of three states 011, 101, 110 by the signal $y_i=0$, where i=1,2,3.

For example, the trigger is in the 011 state; in order to switch it to the 101 state it is necessary to feed a combination of signals $y_2=0$; $y_1=y_3=1$. The signal $y_2=0$ forms a 1 at the output Q_1 and simultaneously confirms the 1 at the output Q_2. Here the "0" level is formed at the Q_3 output. When this level reaches the inputs of the elements D_1 and D_2 it will maintain them in the "1" state now independently of the signal $y_2=0$. As a result, after removal of the control signal (that is, for $y_2=1$) the trigger remains in the "101" state. On arrival at the controlling signal at the input y_3 ($y_3=0$; $y_1=y_2=1$) the trigger goes to the third state 110.

For construction of multistable triggers with cycled input the additional valves are connected in series to the controlling inputs (Figure 5-92).

Construction of Registers Based on the Series K511 JK-Triggers. A four-bit, paraphase, single-cycle shift register is presented in Figure 5-93.

All the bits of the register are connected in series, and the cycling inputs of all of the bits are connected to the common bus which is the cycling input of the register.

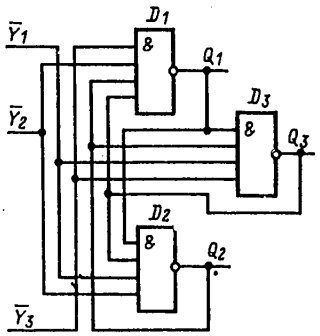


Figure 5-91. Functional diagram of a three-stable trigger

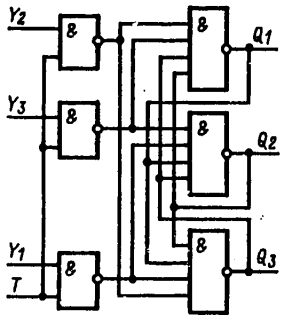


Figure 5-92. Functional diagram of cycled three-stable trigger

Each bit of the number reaches the register by two inputs: A and $\bar{A}$. Each incoming cycle pulse provides a shift of the number code in the register by one bit to the right, that is, for entering a bit code, four cycle pulses are required. The diagram of a reversible shift register based on series K511 JK-triggers is presented in Figure 5-94.

The register has 4 inputs for recording information (A, B, C, D). The cycle inputs of the valves of the 2d, 3d and 4th bits serving for direct series transmission of information in the register from the high-order bitsto the low-order bits are grouped and form the forward shift cycling input (T_{fs}).

The cycling inputs of the valves of the 1st, 2d and 3d bits used for reverse series transmission of the information in the register from the low-order bits to the high-order bits are grouped and form the cycling input of the reverse shift

(T_{rs}). The information is copied from the triggers of the high-order bits to the low-order bits on arrival of cycling signals at the inputs T_{fs} and T_1. The information is copied from the triggers of the low-order bits to the high-order bits on arrival of the cycle pulses at the inputs T_{rs} and T_1.

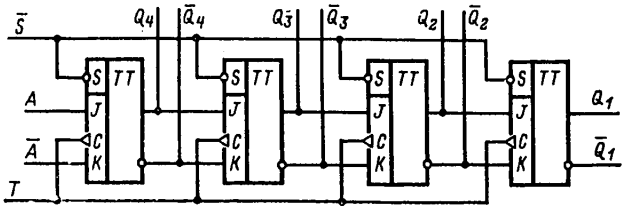


Figure 5-93. Functional diagram of a four-bit, paraphase single-cycle shift register

The code can be entered in the register by two methods:

1. Successive entering of the code of the number for which the bits of the code of the number are successively fed through the AND-NOT valve to the input of the S-trigger of the low-order or high-order bit, and the information is shifted, respectively, in the reverse or forward order by assuming a series of cycle pulses.

2. By parallel entering of the number code for which the corresponding bits of the number code are fed to the inputs of the S-triggers of the register through the valves simultaneously.

Before entering the number code in the register, the register must be initialized; for this purpose a logical zero is fed to the cycle inputs T_{fs} and T_{rs}, and a logical one to the cycle pulses of the triggers. On conversion of the signal at the input T_1 from the logical one state to the logical zero state the register is initialized, for levels of zero and one, respectively, will occur at the inputs J and K of the JK-triggers.

Construction of Distributors Based on the K511 Series Microcircuits. Figure 5-95 illustrates an eight-channel level distributor executed from a two-bit register with cross coupling and one JK-trigger operating in the counting trigger mode and its time diagram. The trigger is cycled by signals from the output Q of the low-order bit of the register. The level decoder is constructed on the basis of the three-input circuits.

The switching pulse successively includes the channels y_1-y_4($\bar{Q}_T$=1), and then series includes the channels y_5-y_8 (for Q_t=1).

For initialization of the distributor, it is necessary to feed the pulse $\bar{S}$=0 to the input $\bar{S}$ of the distributor, and after this, two cycle pulse to the input T_π; the setting pulse duration must satisfy the inequality $\tau_{p.set} \geq t_{del.set}$, where $t_{del.set}$ is the switching delay of the bit trigger. By this signal the triggers are set to the state 1 (Q_1=Q_2=Q_T=1). After feeding two cycle pulses to the input T_π the register converts to the "0" state (Q_1=Q_2=Q_T=0).

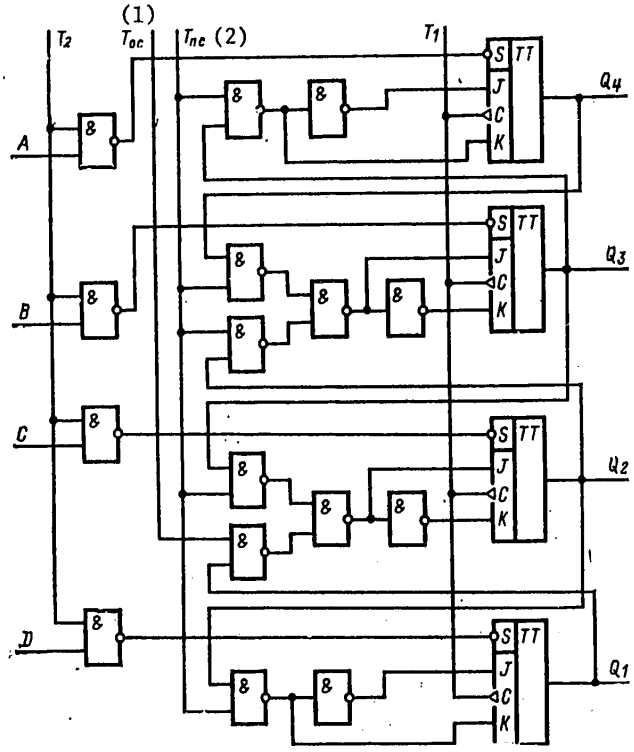


Figure 5-94. Functional diagram of reversible shift register

Key:
1. T_{fs}
2. T_{rs}

When constructing the pulse distributors, the decoders are executed from four-input AND circuits in which the fourth input is connected to the distributor pulse switching bus.

The diagram of the level distributor for eight channels constructed on the basis of two T_t-triggers with carry and borrow is illustrated in Figure 5-96.

This circuit operates when switching pulses of the "meander" type are fed to its input.

When the signals reach the input of the distributor with switching frequency f_{switch} the time of effect of the levels on each of the potential outputs will be $(1/2)f_{switch}$. The pulse duration corresponds to the switching pulse duration.

The carry output П and the borrow output З are the outputs of the two-channel pulse distributor.

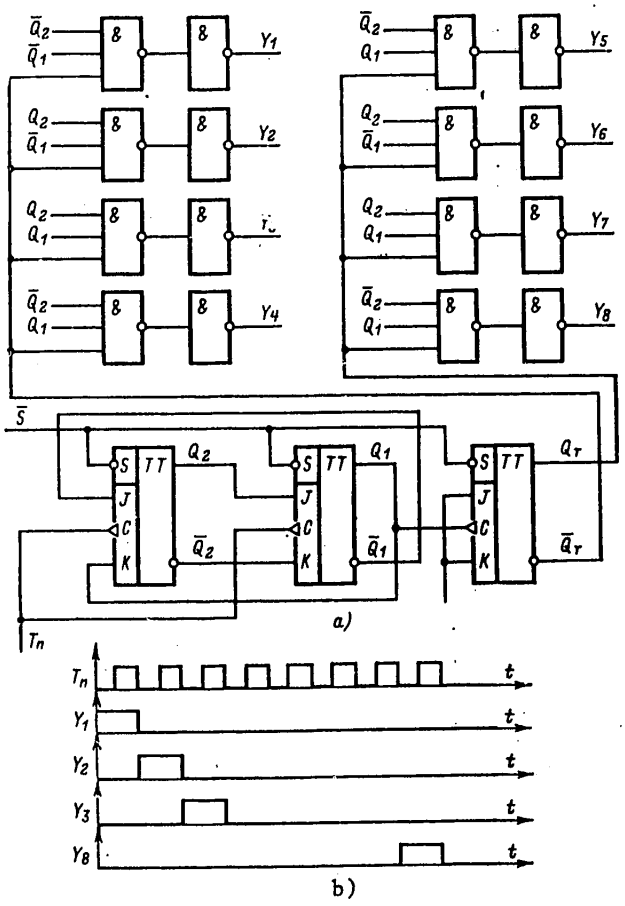


Figure 5-95. Functional diagram of an eight-channel distributor (a) and operating time diagram (b)

The structure of the distributors for an arbitrary number of outputs is realized using counters with arbitrary counting factor. The shaping of the channel signals is provided as a result of connection of comparison circuits to the counter, the number of which is equal to the number of states of the counter.

Construction of Decoders. Figures 5-97 and 5-98 present diagrams of the functional Johnson code to decimal code and "1248" code to decimal code converters. The initial state of all of the outputs is a logical one. The inputs are connected to the outputs of the corresponding bits of the counter. The operation of the converter consists in varying the state of one of the switches under the condition that all its inputs are converted to state 1 when fed a binary-decimal code.

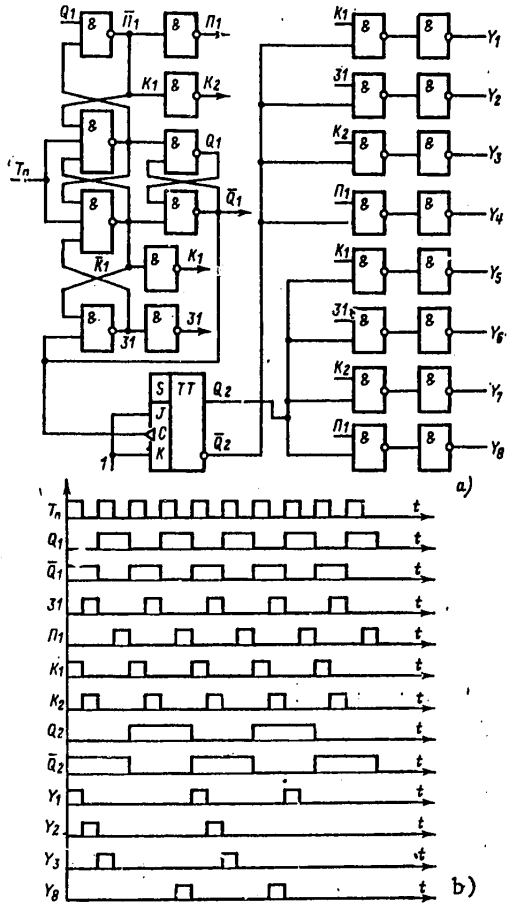
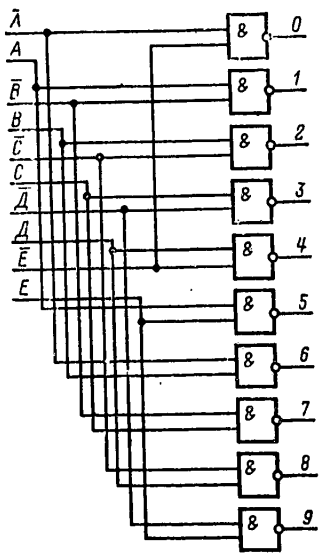


Figure 5-96. Functional diagram of a combined type distributor (a) and operating time diagram (b)

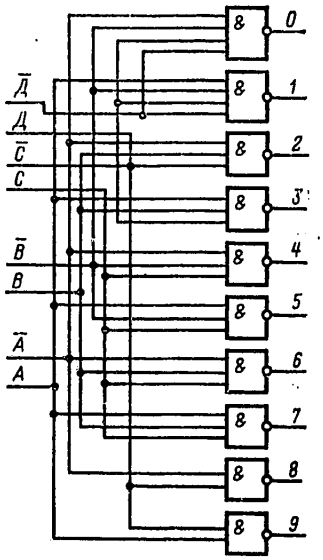
The functional diagram of a three-bit decoder is presented in Figure 5-99.

The construction of a decoder for 16 outputs based on two series K511 decoders is illustrated in Figure 5-100. The outputs of the linear decoder for 16 outputs will be the outputs 0-7 of the first VPL IC and the outputs 0(8)-7(15) of the second VPL IC. The outputs 8 and 9 of the first VPL PC repeat the state of the outputs 0, 1 of the second VPL IC, and the outputs 8 and 9 of the second VPL IC -- the state of the outputs 0, 1 of the first VPL IC.



(1) Входы					(2) Единица счета
E	Д	C	B	A	
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	1	1	3
0	1	1	1	1	4
1	1	1	1	1	5
1	1	1	1	0	6
1	1	1	0	0	7
1	1	0	0	0	8
1	0	0	0	0	9

Figure 5-97. Functional diagram of a Johnson to decimal code converter
Key:
1. inputs
2. counting unit



Входы (1)				(2) Единица счета
Д	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Figure 5-98. Functional diagram of a "1248" to decimal code converter
Key:
1. inputs
2. counting unit

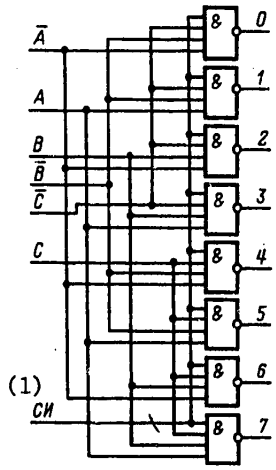


Figure 5-99. Functional diagram of a three-bit decoder

Key:
1. SI

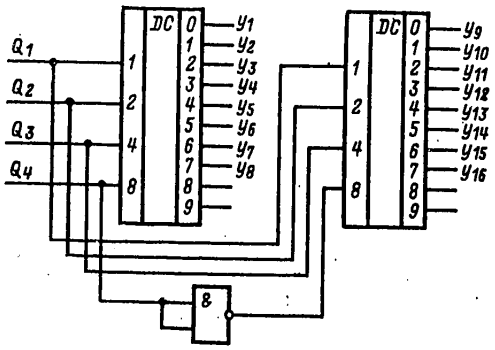


Figure 5-100. Functional diagram of a decoder for 16 outputs

Construction of Adders. The functional diagram of a single-bit adder is presented in Figure 5-101, a. The functions of summation (S) and carry (P) are realized in accordance with the expression S=ABC+P(A+B+C); P=AB+AC+BC.

In the given diagram for realizing the function P elements are used with passive collector output (K511LA5), the outputs of which can be grouped for organization of the OR function. The inputs A, B and C are single-phase. The sum formation delay is $3t_{del,p,mean}$.

The functional diagram of a single-bit adder is presented in Figure 5-101, b.

The adder is based on nine valves; it has paraphase inputs and sum shaping and carry delay equal to $5t_{del,p,mean}$.

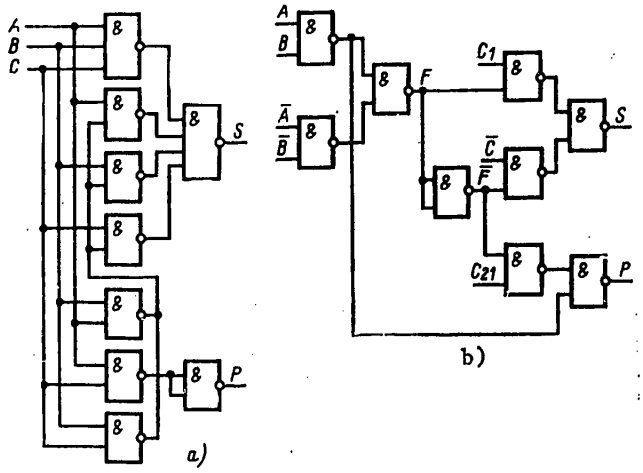


Figure 5-101. Functional diagram of a single-bit adder

Square Pulse Generators. On the basis of the VPL IC of the K511 series it is possible to construct a number of generators which generate square pulses lasting from several microseconds to several seconds.

In Figure 5-102 we have the diagram of a square pulse generator and its time diagram. The general can be executed from the K511LA1 microcircuit. The pulse duration is defined by the equation

$$\tau = kC,$$

where τ is the pulse duration, milliseconds; C is the capacitance of the capacitor, microfarads; k is 1 millisecond/microfarad, coefficient.

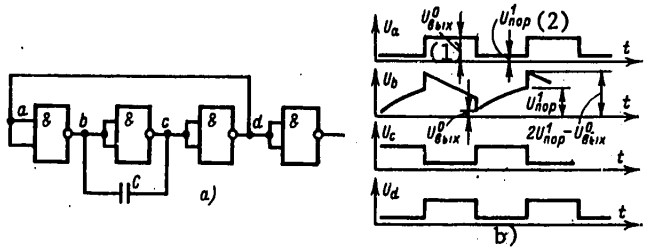


Figure 5-102. Functional diagram of a square pulse generator (a) and operating time diagram (b)

Key:
1. out
2. threshold

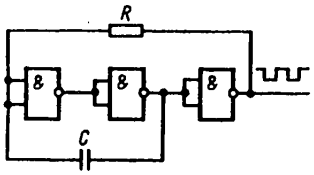


Figure 5-103. Functional diagram of a square pulse generator with one time master circuit

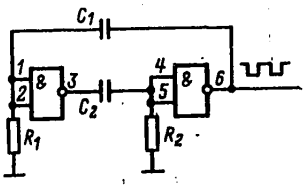


Figure 5-104. Functional diagram of a square pulse generator

Figure 5-103 shows the diagram of a square pulse generator with one time master circuit. The pulse duration is given by the capacitance of the capacitor and the resistor. For R=15 kilohms the pulse duration is defined by the formula

$$\tau = kC, \text{ where } k = 12 \text{ milliseconds/microfarad.}$$

For C=300 picofarads the pulse duration is defined by the expression

$$\tau = 0.4R,$$

where τ is the pulse duration, microseconds; R is the resistance of the resistor, kilohms.

Figure 5-104 shows the diagram of a square pulse generator in which the pulse duration is given by the capacitances C_1 and C_2, and it is regulated by the resistor R_2, the duty factor is regulated by the resistor R_1. For C_1=0.1 microfarad, C_2=0.5 microfarad; R_1=15 kilohms, R_2=45 kilohms; the pulse duration is 5 microseconds.

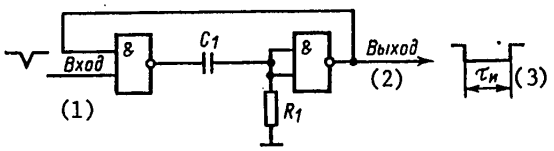


Figure 5-105. Functional diagram of a univibrator

Key:
1. input
2. output
3. τ_{pulse}

Figure 5-105 shows the diagram of a univibrator controlled by pulses of negative polarity. The posulation at the output of the univibrator is given by the capacitances and regulated by the resistor R_1.

The graph of the pulse duration as a function of the resistance of the resistor is shown in Figure 5-106.

Figure 5-107 represents the frequency divider circuit based on a univibrator.

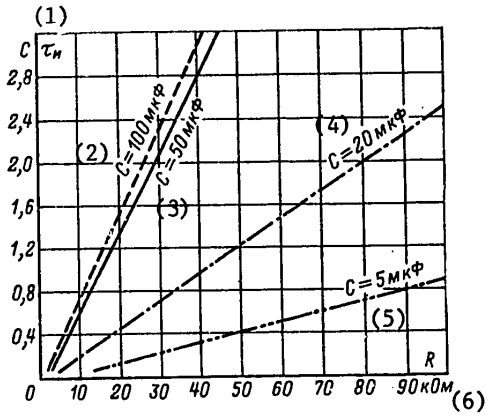


Figure 5-106. Graph of the pulse τ_{imp} as a function of the resistor resistance for different capacitances

Key:
1. τ_{pulse}
2. C=100 microfarads
3. C=50 microfarads
4. C=20 microfarads
5. C=5 microfarads
6. kilohms

K176 Series Microcircuits

General Recommendations. The K176 series microcircuits are circuits with very low intake power levels in the static mode (on the order of several microwatts), and their application is especially effective in the equipment operating predominantly in the weighting mode or in devices with ready redundancy.

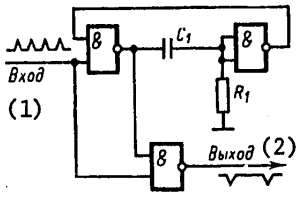


Figure 5-107. Functional diagram of a frequency divider based on a univibrator
Key: 1. input; 2. output

In order to estimate the intake power of the microcircuits a graph is presented in Figure 5-108 for the dynamic intake current by one inverter of the K176LA7 microcircuit as a function of the capacitive load on different switching frequencies.

Table 5-8 presents the statistical values of the input capacitance C_{inp} as a function of the number of grouped inputs for the K176LYe5, K176TM1 microcircuits.

The power intake by the inverter in the dynamic mode, $P_{int\ dyn}$ is directly proportional to the sum of the load capacitance C_{load}, the output capacitance of the inverter C_{out} and the inverter switching frequency C_i. This power can be

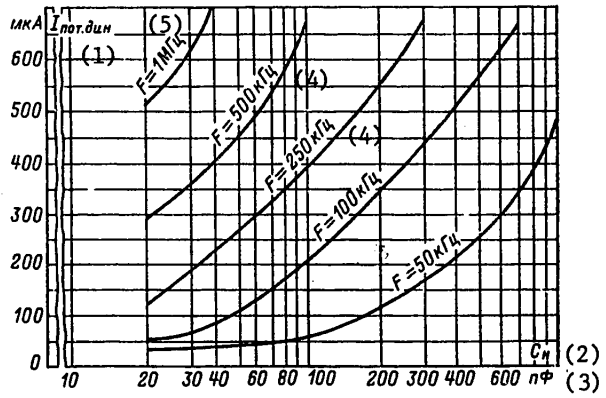


Figure 5-108. Dynamic intake current by one inverter of the K176LA7 microcircuit as a function of the capacity of load on different switching frequencies ($U_{p.s}$=9 volts, t°=+25°C)

Key:
1. $I_{int.dyn}$
2. C_{load}
3. picofarads
4. kilohertz
5. megahertz

estimated by the following formula with accuracy sufficient for practical application:

$$P_{int.dyn} = (C_{load} + C_{out})U^2_{p.s}f,$$

where $C_{load} = C_{wire} + C_{inp}K_{fan-out}$ is the load capacitance, picofarads; C_{wire} is the wiring capacitance, picofarads; C_{inp} is the capacitance of one input of the load microcircuit, picofarads; $K_{fan-out}$ is the number of connected inputs of the load microcircuits; $C_{out} \leq 30$ picofarads; f is the operating frequency, millihertz; $P_{int\ dyn}$ is the power intake of the dynamic mode, microwatts.

Table 5-8

K176LYe5		K176TM1	
Номера входов (1)	Входная емкость (2) $C_{вх}$, пФ	Номера входов (1)	Входная емкость (2) $C_{вх}$, пФ
1	7—10,3	3	11,0—15,0
1 и 2	14—21,3	3 и 4	21,0—27,5
5	7,2—10,3	3, 4 и 5	28,0—37,5
5 и 6	13,7—20,5	9	7,5—11,0
8	7,0—10,9	9 и 10	18,5—24,0
8 и 9	15,8—20,7	9, 10 и 11	31,5—39,0
12	8,0—11,2		
12 и 13	15,3—21,2		

Key:
1. Input numbers
2. Input capacitance C_{inp}, picofarads

Requirements on the Input Signal Front and Decay. During operation of microcircuits from other radio elements the input signal front and decay duration should not exceed 15 microseconds (except the 176LP1 microcircuit on connecting the external load resistance). Here the time parameters for the microcircuits are not regulated.

The direct mode current of the powerful inverter presented in Figure 5-109, c must not exceed 2 milliamps. Here the voltages U^0_{out} and U^1_{out} for the K176LP1 microcircuits are not regulated.

During operation of the series K176 microcircuits it is necessary to consider that the dangerous value of the electrostatic potential must not exceed 30 volts.

When designing the equipment for the series K176 IC it is necessary also to consider that the power supply voltage must be fed to the input signal voltage, and the free information inputs of the microcircuits must be connected to one of the feed buses ($U_{p.s}$ or "common") considering the functional peculiarities of one microcircuit or another.

Diagrams of the Application of the K176 Series Microcircuits. Examples of the realization of various logical functions by the K176LP1 microcircuit are presented in Figure 5-109.

Registers. An example of the construction of a single-cycle series shift register is presented in Figure 5-110. The four-bit register is executed on the basis of two K176TM2 microcircuits.

Figure 5-111 shows an example of the realization of a universal register. Each bit of the register consists of a T-trigger and a distributing device. The four-bit universal register is executed from two K176TM2 microcircuits, two K176LA7 microcircuits and one K176LA9 microcircuit. The presence of a distributing device at the input of each bit increases the functional possibilities of the register circuitry, making it universal.

For example, in order that a series left to right shift register be realized on the basis of the given universal register, it is necessary to feed a low voltage level to the control input Ynp, and to use the input Bx_1 as the information input. For realization of the right-to-left shift it is necessary to feed a high voltage level to the input Ynp, and to use the input Bx_4 as the information input. The inputs Bx_1, Bx_2, Bx_3, Bx_4 can be used to convert the parallel code to series.

A bit of a two-cycle shift register constructed on the basis of two single-cycle D-triggers of the K176TM2 microcircuit and its operating time diagram are presented in Figure 5-112.

For proper functioning of the devices executed from D-triggers, the null-setting signal R or the one setting signal S is realized by a high-voltage level, the duration of the setting signal must be no less than the time of transition of the D-trigger with respect to the inputs R, S (no less than 1 microsecond).

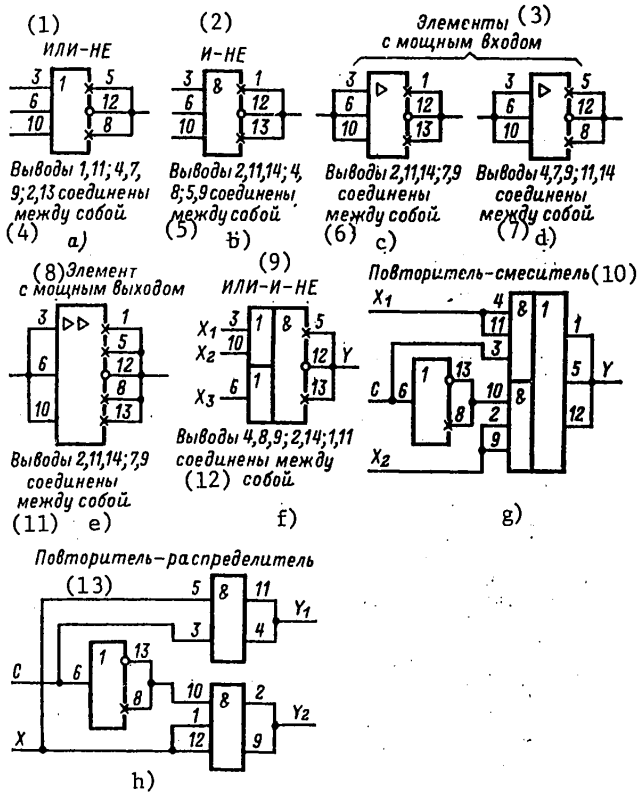


Figure 5-109. Realization of logical functions by the K176LP1 microcircuit

Key:

1. OR-NOT
2. AND-NOT
3. Elements with power volt input
4. Terminals 1,11; 4, 7, 9; 2, 13 are connected to each other
5. Terminals 2, 11, 14; 4, 8; 5, 9 are connected to each other
6. Terminals 2, 11, 14; 7, 9 are connected to each other
7. Terminals 4, 7, 9; 11, 14 are connected to each other
8. Element with powerful output
9. OR-AND-NOT
10. Repeater-mixer
11. Terminals 2, 11, 14; 7, 9 are connected to each other
12. Terminals 4, 8, 9; 2, 14; 1, 11 are connected to each other
13. Repeater-distributor

The setting signal must be removed on satisfaction of one of the conditions:

A high-voltage level is applied to the input C; the setting signal is removed at the time of changing the voltage at the input C from high level to low;

A low-voltage level is applied to the input C, the duration of which after removal of the setting signal must be sufficient to enter the information in the reception trigger with respect to the input D (no less than 1 microsecond).

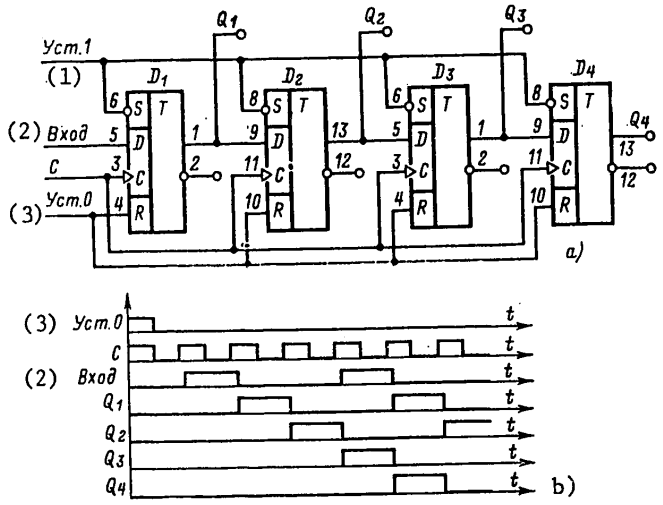


Figure 5-110. Functional diagram of a single-cycle, four-bit shift register (a) and operating time diagram (b).
D_1-D_4 -- K176TM2 microcircuits; Ycm.1 -- constant logical zero level

Key:
1. Set 1
2. Input
3. Set 0

Frequency Dividers. The single-cycle frequency dividers with series carry are the simplest with respect to the circuit engineering execution. They are executed from D-triggers by connecting the outputs of the preceding bits to the inputs of the subsequent bits. The division coefficient of such a divider is $K_{div}=2^n$, where n is the number of bits of the divider.

The diagram of a single-cycle frequency divider by 2 and the operating time diagram for it are illustrated in Figure 5-113, the divider is executed from the K176TM2 microcircuit.

A single-cycle frequency divider by 8 with series carry and its operating time diagram are presented in Figure 5-114; the divider is executed from 3/2 K176TM2 microcircuits.

Dividers with Group Carry. In the dividers with group carry the input pulses go to the common bus for all bits. The arrival of the input pulses and the bit inputs of the given group is determined by the state of the controlling output of the preceding group of bits. It is most expedient to build dividers with

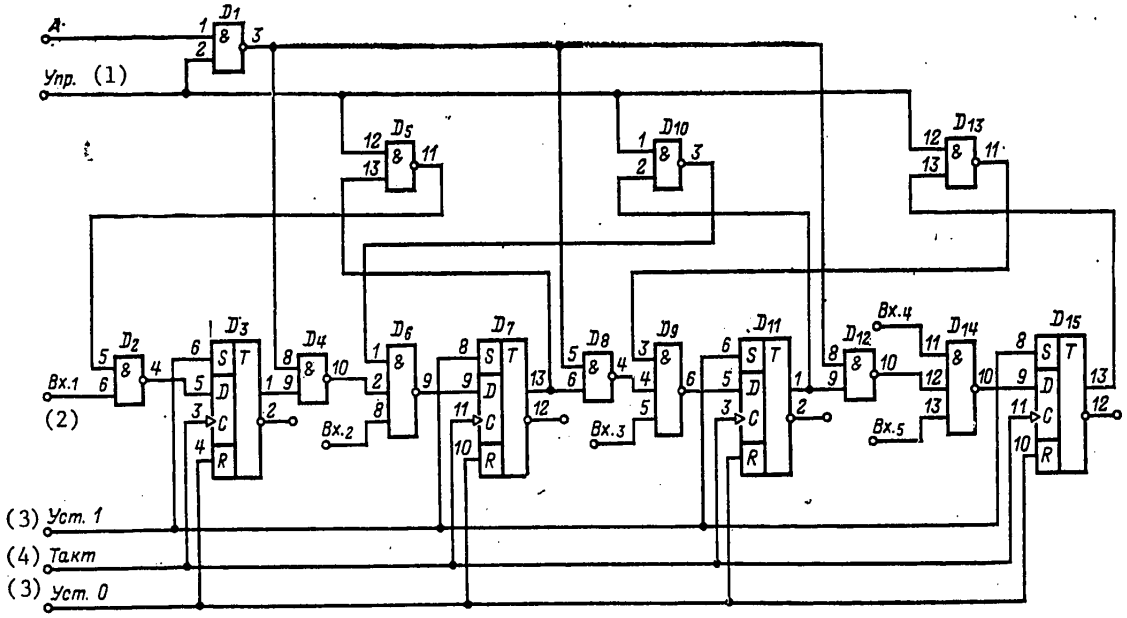


Figure 5-111. Functional diagram of a universal shift register D_1, D_2, D_4, D_5, D_8, D_{10}, D_{12}, D_{13} -- K176LA7 microcircuits; D_6, D_9, D_{14} -- K176LA9 microcircuit; D_3, D_7, D_{11}, D_{15} -- K176TM2 microcircuits; circuit A -- constant level of logical one

Key:
1. Control
2. Input ...
3. Set
4. Cycle

group carry with small division factors (from 4 to 10) based on the shift register circuitry with cross connections using the K176 series microcircuits.

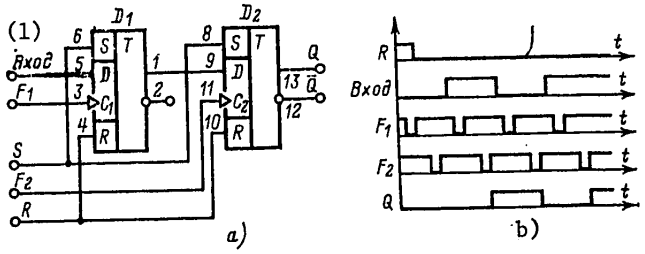


Figure 5-112. Functional diagram of the bit of a two-cycle register based on the K176TM2 microcircuit (a) and the operating time diagram (b).

Key:
1. input

An example of a divider by 6 with group carry in a register with cross connection executed from K176TM2 microcircuit and the operating time diagram of the divider are presented in Figure 5-115.

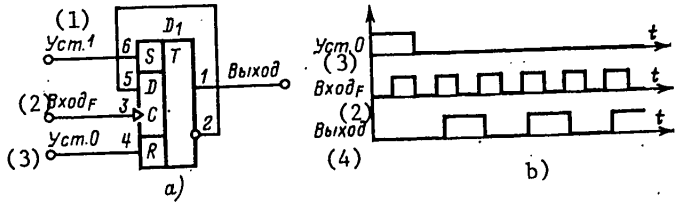


Figure 5-113. Functional diagram of a single-cycle divider by 2 (a) and operating time diagram (b).
Ycm. 1 -- constant level of logical zero

Key:
1. Set 1
2. Input
3. Set 0
4. Output

The circuit has six stable states and under the effect of the pulses reaching its input it makes the transition successively from one state to the other, insuring division of the input pulses by 6.

The dividers based on registers with cross coupling have an even division factor $K_{div}=2n$, where is the number of bits.

An odd division factor $K_{div}=2n-1$ is obtained as a result of introducing additional feedback from the forward output of the high-order bit to the null setting input of the low-order bit.

The diagram of a divider with group carry by 5 executed from K176TM2 microcircuit and the operating time diagram of the divider are presented in Figure 5-116.

Reversible Counter. The diagram of a reversible counter by 5 is presented in Figure 5-117.

It is designed for calculating the difference in the number of pulses of two trains with respect to the inputs Bx_1 and Bx_2.

The reversible counter consists of the input device (D_1-D_5), frequency divider (D_6-D_{19}), the control unit (D_{22}-D_{26}), the forward and return counting channel analyzers (D_{21}, D_{24}), the initial state analyzer (D_{20}, D_{27}) and the initializing circuit (D_9, D_{13}).

The input unit, which is a mod 2 addition circuit is designed to forbid the feeding of pulses to the counter input and forbid transmission of information to the output of the forward and return counting channel analyzers if simultaneous arrival of the counting pulses on both channels occurs.

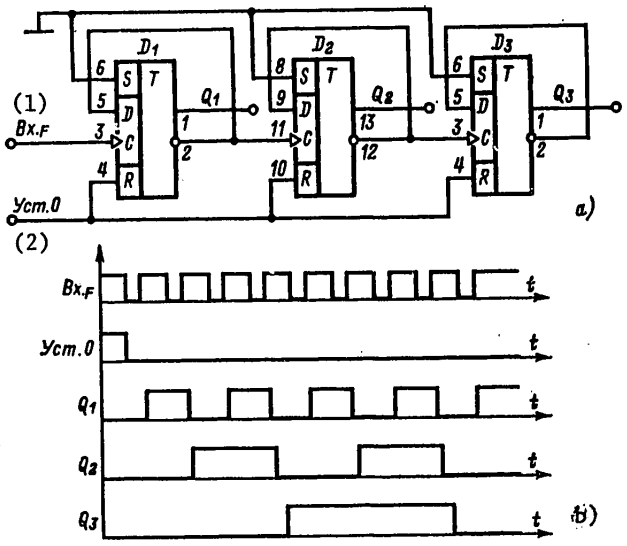


Figure 5-114. Functional diagram of a single-cycle divider by 8 (a) and time diagram (b)

Key:
1. Input ...
2. Set

For initialization of the counter it is necessary to send a logical one voltage level to the "set 0" input.

The frequency divider is a circuit executed on the basis of a divider by 6 with cross couplings by introducing a controlled reversing circuit.

The control unit is designed to exclude the appearance of pulsed signals at the outputs of the counter in case of response of the channel analyzer on which no counting is taking place.

The forward and return counting channel analyzers are tuned to the corresponding combinations of counting and are connected through an OR circuit to the initialization circuit which forces initialization of the divider.

Adder. Figure 5-118 gives an example of the realization of a series adder with carry memory based on three K176LA7 microcircuits and one K176TM2 microcircuit. The numbers in the sum S and the carry P are formed by the following boolean relations:

$$S=\bar{X}_1\bar{X}_2P_{i-1}+\bar{X}_1X_2\bar{P}_{i-1}+X_1\bar{X}_2\bar{P}_{i-1}+X_1X_2P_{i-1};$$
$$P_i=X_1X_2+X_1\bar{X}_2P_{i-1}+\bar{X}_1X_2P_{i-1},$$

where P_i is the carry formed in the given cycle; P_{i-1} is the carry formed in the preceding cycle.

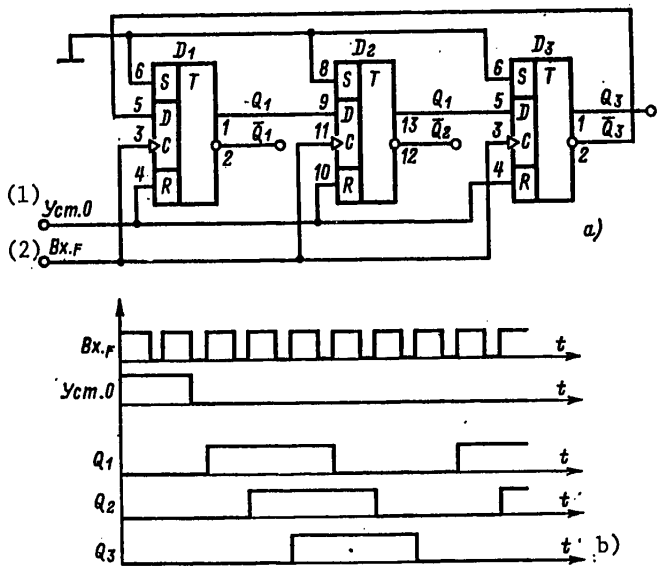


Figure 5-115. Functional diagram of a divider by 6 with group carry (a) and operating time diagram (b)

Key:
1. Set
2. Input

The numbers in the carry in the given addition cycle are stored in the trigger, from the output of which the carry signal is picked up in the following addition cycle.

Pulse Distributor. The pulse distributor is designed for use in multicycle electronic devices, and it is an input pulse train distributor to four output buses.

The distributor is constructed from K176LA7, K176LA9, K176TM2, and K176LYe5 microcircuits, and it is presented in Figure 5-119. The operating time diagram is presented in Figure 5-120. On feeding a logical one voltage to the "clear" input, the inverters D_3 and D_6 are closed, and the input pulse train cannot be transmitted to the distributor; in this case the signal level at the terminal 6 of the microcircuit D_2 and the terminal 9 of microcircuit D_3 corresponds to the logical one voltage. The circuit assembled from D_6 and D_7 elements "stores" this state and through the feedback circuit to the element D_1 prepares the input part of the circuit for the next operating cycle.

On feeding a logical zero voltage to the "clear" input, the elements D_3 and D_6 are fed a permitting logical one voltage signal and the next input pulse, passing through the D_2 or D_3 element, to two inputs of which the signals U^1_{inp} were fed in the preceding cycle, changes the output signal of the corresponding element (D_2 or D_3). This information is stored by the circuit D_6, D_7 for preparing the input part of the circuit for the next cycle, and so on. The output signals from

the elements D_2 and D_3 control the state of the triggers D_8 and D_9 and together with the output signals of these triggers control the output elements D_{10}, D_{11}, D_{12}, D_{13}, providing for the generation of the output pulses.

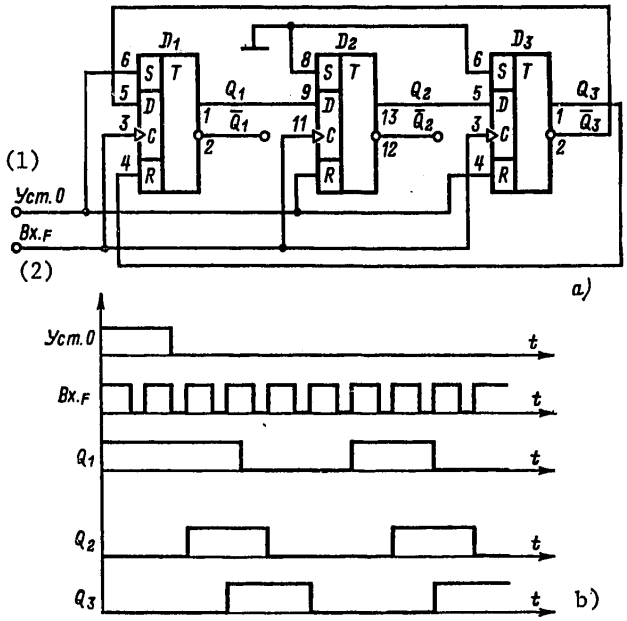


Figure 5-116. Functional diagram of a divider by 5 with group carry (a) and operating time diagram (b)

Key:
1. Set
2. Input

The synchronization of the operation of the digital data processing units is realized as a result of introducing a cycle generator which provides for formation of the cycle pulse trains and their multiplication on breakdown of the synchronizable memory elements (EP) into groups. The number of EP in each group is determined by the fan-out of the cycle pulse amplifiers of the multiplication circuit.

A powerful inverter diagram presented in Figure 5-109 assembled on the basis of the K176LP1 microcircuit can be used as the cycle pulse amplifier.

The fan-out $K_{\text{fan-out, dyn}}$ of this inverter is defined by the formula

$$K_{\text{fan-out, dyn}} = \frac{\frac{K_{\text{group}} \cdot 0.29 P_{\text{perm}}}{U^2_{\text{p.s}} F} - C_{\text{wire}}}{C_{\text{inp}}},$$

where K_{group} is the number of grouped elements of the microcircuit; P_{perm} is the maximum admissible power for one logical element, microwatts; $U_{\text{p.s}}$ is the feed voltage, volts; F is the operating frequency, millihertz; C_{wire} is the wiring

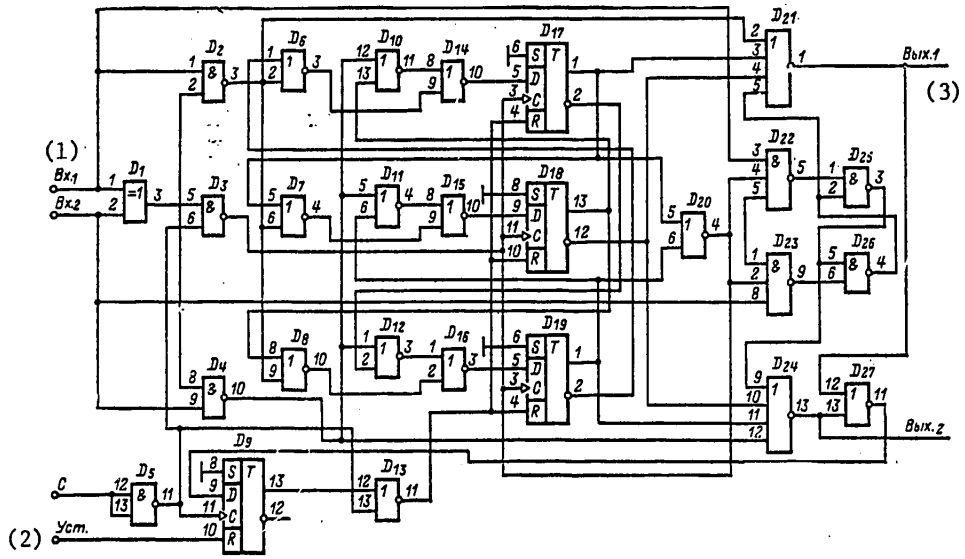


Figure 5-117. Functional diagram of the reversible counter by 5.
D_1 -- K176LP2; D_{21}, D_{24} -- K176LYe6 microcircuit; D_2-D_5 -- K176LA7 microcircuit; D_{22}, D_{23} -- K176LA9 microcircuit; D_6-D_{16}; D_{20}, D_{27} -- K176LYe5 microcircuit; D_{26}, D_{25} -- K176LA7 microcircuit; D_{17}-D_{19} -- K176TM2 microcircuit

Key:
1. Input
2. Set
3. Output

capacitance, picofarads; C_{inp} is the maximum capacitance of one input of the microcircuit, picofarads.

The total capacitance of the amplifier load when using it as the cycle pulse amplifier and for K_{group} no less than 3 must be no more than 450 picofarads (for C_{wire}=50 picofarads this corresponds to $K_{fan-out, dyn} \leq 50$) when insuring a value of the maximum admissible $I_{int, dyn}$ of no more than 2 milliamps.

The synchronization of the single-pulse circuits can be realized by the following procedures: series, parallel, combined.

The diagram of the organization of the cycle feed for series synchronization is presented in Figure 5-121. The initial cycle frequency is fed to the input of n series-included power amplifiers, the outputs of which are connected to the synchronizing inputs of the memory elements (EP) in such a way that the output of the first power amplifier is connected to the inputs of the n-th group of the EP, the output of the second power amplifier to the inputs n-1, and so on, and the output of the n-th power amplifier, to the inputs of the first group of the EP. The EP must be broken down into groups in accordance with the direction of the information transmission.

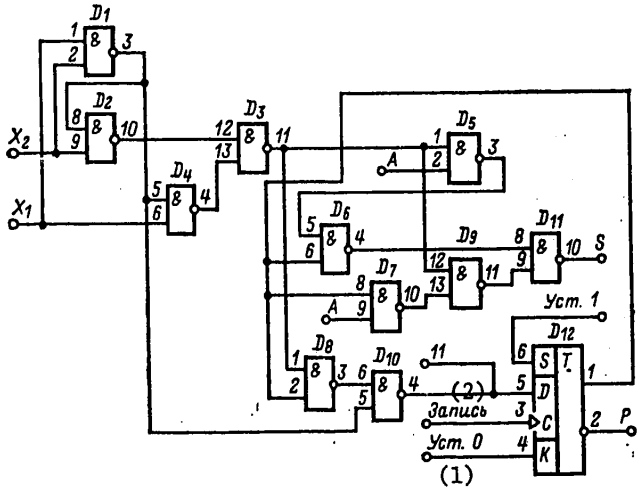


Figure 5-118. Electrical functional diagram of a series adder. D_1-D_{11} -- K176LA7 microcircuit; D_{12} -- K176TM2 microcircuit; Circuit A -- constant logical one level; Ycm.1 -- constant logical zero level

Key:
1. Set
2. Write

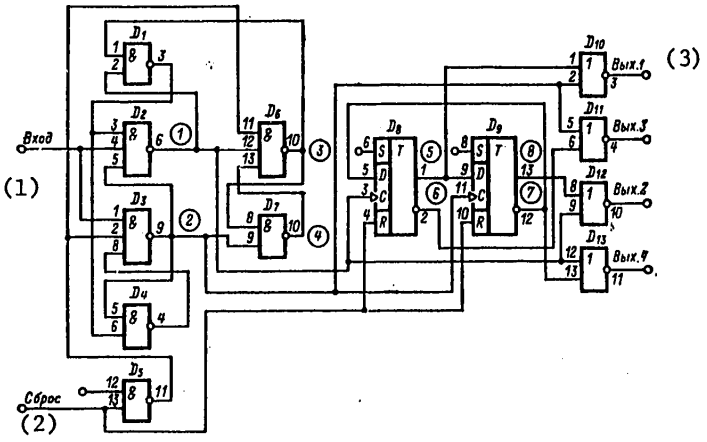


Figure 5-119. Functional diagram of a pulse distributor. D_1, D_4, D_5, D_7 -- K178LA7 microcircuit; D_2, D_3, D_6 -- K176LA9 microcircuit; D_8, D_9 -- K176TM1 microcircuit; D_{10}-D_{13} -- K176LA7 microcircuit

Key:
1. Input
2. Clear
3. Output

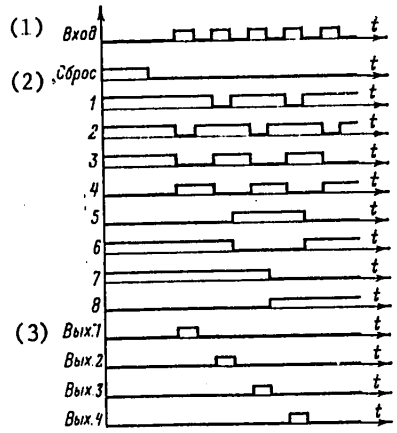


Figure 5-120. Time diagram of the pulse distributor

Key:
1. Input
2. Clear
3. Output ...

In the presence of feedback between the subsequent and preceding groups ahead of the EP, to the inputs of which the feedback comes, it is necessary to install matching elements which are triggers controlled by the logical one level. The matching element must be synchronized by the cycle frequency of the EP group to which the feedback is fed.

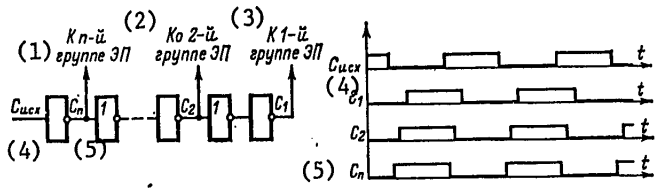


Figure 5-121. Cycle feed circuit with series synchronization

Key:
1. to the n-th EP group
2. to the 2d EP group
3. to the 1st EP group
4. C_{init}
5. C_n

For the parallel synchronization procedure the initial cycle frequency is fed to the power amplifier input, the output of which is connected to the inputs of n power amplifiers, the outputs of the latter are connected in turn also to the inputs of the power amplifier and so on.

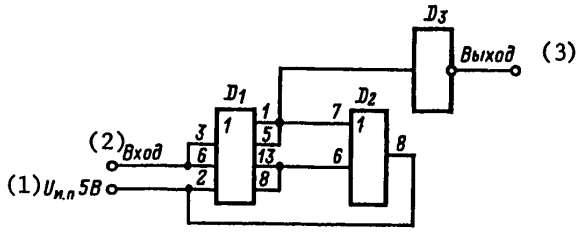


Figure 5-122. Diagram of the level conversion for coupling K176 series microcircuits to the TTL type microcircuit. D_1, D_2 -- K176LP1 microcircuits, terminals 4, 7, 9 of the microcircuit D_1 are connected to the "ground" bus, terminal 14 of microcircuit D_1 is connected to the $U_{p.s}$=9 volts; D3 is the K134 series microcircuits

Key:
1. $U_{p.s}$ 5 volts
2. Input
3. Output

The number of stages of the cycle pulse multiplication circuit is determined by the number of synchronized EP and the fan-out coefficient $K_{fan-out}$ of the power amplifiers.

For the parallel method of synchronization any output amplifier can synchronize any group of EP, but in this case it is necessary to install matching elements at the input of each EP, the information to which comes from other groups.

For the combined method of synchronizing the EP are divided into groups inside which the synchronization is done by the series procedure, and between groups, by the parallel procedure.

Coupling IC of the K176 Series to Other Series. The K176 series microcircuits can be coupled to TTL type microcircuits, for example, series K134, through the level conversion circuit presented in Figure 5-122 and executed from two K176LP1 microcircuits. The output of each level conversion circuit can be loaded by no more than one logical element of the K134LA2 type microcircuits.

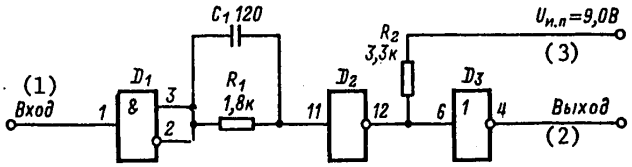


Figure 5-123. Functional diagram of the coupling of K134 and K176 series microcircuits

Key:
1. Input
2. Output
3. $U_{p.s}$=9.0 volts

The K176 series microcircuits are coupled to the K155 and K158 series microcircuits to a conversion circuit and K134 series microcircuit presented in Figure 5-122.

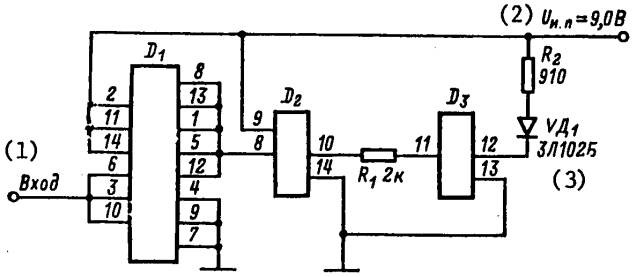


Figure 5-124. Functional diagram of the coupling of microcircuits on the K176 series and the K149 series operating in the display amplifier mode.
D_1 -- K176LP1 microcircuit; D_2, D_3 -- K149KT1V microcircuit

Key:
1. Input
2. $U_{p.s}$=9.0 volts
3. 3L102B

The output of the K134LA1 microcircuit can be loaded by no more than one input of the K155LA1, K155LA7, and K155LA8 microcircuits and by no more than four inputs of the K158LA1 microcircuit.

The series K134 microcircuit can be coupled to the series K176 microcircuits through the K149KT1V microcircuit according to the diagram presented in Figure 5-123.

Figure 5-124 contains a diagram for coupling a powerful inverter based on the K176LP1 to the K149KT1V microcircuit operating in the display amplifier mode.

The operating diagram of the K149KT1V microcircuit on an incandescent tube type SMN6,3-20 is presented in Figure 5-125. The K149KT1V microcircuit is controlled on a powerful inverter based on the K176LP1 microcircuit.

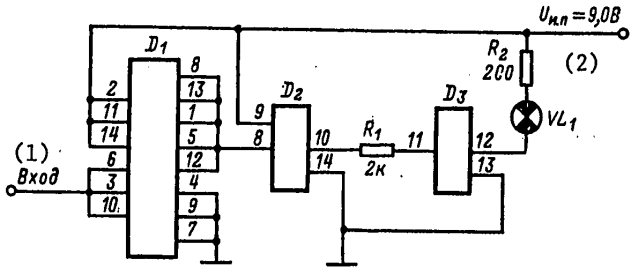


Figure 5-125. Functional diagram of the coupling of the K176 series microcircuits to the K149 series microcircuits operating on an incandescent tube.
D_1 -- K176LP1 microcircuit; D_2, D_3 -- K149KT1V microcircuit

Key: 1 -- input; 2 -- $U_{p.s}$=9.0 volts

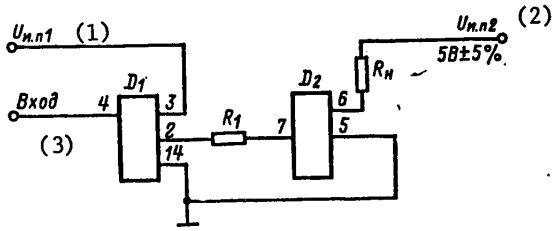


Figure 5-126. Coupling diagram for coupling the K176 series microcircuits to the K149 series microcircuits
D_1-D_2 -- K149KT1V microcircuit

Key:
1. $U_{p.s}$1
2. $U_{p.s}$2
3. Input

For operation of the K176 series microcircuits on powerful elements it is expedient to use the diagram presented in Figure 5-126 executed from the K149 series microcircuits. The circuit is started from a powerful inverter formed by parallel connection of thee inverters of the K176LP1 microcircuit. The feed voltage $U_{p.s}$=9.0 volts±5%.

The output current of the circuit must not exceed 75 milliamps; the resistance of the resistor R required to insure the output current is determined from the expression

$$I_{н(1)} = \frac{50}{R+0{,}15},$$

Key: 1. load

where I_{load} of no more than 75 milliamps is the load current; R no less than 0.45 kilohms is the resistance of the resistor R_1.

The dissipation power of the resistor R_1 must be no less than 0.25 watts with a resistor resistance to 600 ohms and no less than 0.125 watts for a resistor resistance of more than 600 ohms. The admissible deviation of the resistance R from the rated value must be no more than ±5%.

The diagram presented in Figure 5-126 can be used to start the relay.

It provides for tripping the relay with current parameters no more than 75 milliamps and voltage parameters of no more than 15 volts considering the admissible deviation of the feed voltage.

When selecting the type of relay it is necessary to consider the variation in resistance of the relay winding as a function of temperature.

The presented diagram, for example, provides for triggering the RES-44 type relay. The relay is included in place of the load resistance R_{load} depicted in the diagram in Figure 5-126. The feed voltage of the output transistor from the

relay voltage overloads must be shunted by the 2D509A type diode. The feed voltage $U_{p.s2}$ must be 12 volts±10%.

Instructions for Constructing Communication Lines Between Microcircuits. When designing the equipment based on the K176 series microcircuits it is necessary to consider that the coupling capacitance between the conductors connecting the information transmission microcircuits to the information receiving microcircuits is the load capacitance for the microcircuits transmitting information, the increase in which leads to an increase in the dynamic current intake by the microcircuit and must not exceed 100 picofarads to exclude the effect of the cross talk between individual wires in asynchronous devices.

When designing the equipment based on K176 series microcircuits it is necessary to provide for protection against pulsed interference on terminals 7 and 14 of the microcircuits, for which it is recommended that decoupling capacitors, low and high frequency, simultaneously, be installed in the feed circuits. The types of capacitors and their capacitances are selected as a function of the structural design of the equipment.

The capacitances of the capacitors can be approximately selected calculating the following: low frequency, 2.2 microfarads for every 50 microcircuits; high frequency, 0.68 microfarads also for every 50 microcircuits.

It is recommended that the decoupling capacitors be installed uniformly over the area of the printed circuit board and also near the plugs.

The electric communication lines between the microcircuits inside the modules can be made by printed circuitry and point-to-point wiring.

In the case of mixed wiring (printed and point-to-point) it is recommended that the wires be run perpendicular to the printed wires on the printed circuit board.

The system of ground and feed buses must have minimum possible resistances and inductances (with maximum possible capacitance between them).

The cycle pulse conductors more than 30 cm long in the bunched conductors must be shielded (each individually). The length of the conductor is selected beginning with the maximum admissible load capacitance for the cycle pulse amplifier by the formula

$$C_{wire} = \frac{0.29 P_{ad} K_{group}}{U^2_{p.s} F} - C_{inp} K_{fan\text{-}out,\ dyn}.$$

The length of the wires between the microcircuits is selected beginning with the maximum admissible load capacitance:

$$C_{wire} = \frac{0.34 P_{ad}}{U^2_{p.s} F} - C_{inp} K_{fan\text{-}out,\ dyn}.$$

In the single-cycle synchronous devices and modules, it is permissible to make the information circuits using unshielded wires in the bunched conductor communication lines containing information and cycle circuits.

The transition from the D-triggers to the bunched conductor consisting of wires more than 30 cm long must be made through the inverter of the K176LP1 microcircuit.

If the capacitance of the wires in the bunched conductor or cable exceeds the maximum admissible capacitance of the load of a single inverter, it is necessary to make the junction from the D-trigger to the communications line through the amplifier, the diagram of which is presented in Figure 5-109, c.

In all cases the capacitance of the communication lines must not exceed the maximum admissible load capacitance for the element from which the junction to the communication line is realized.

Series K131, K155, and K158 Microcircuits

Recommendations for Connecting Unused Inputs. In order to insure maximum speed and noiseproofness, the unused inputs must be under constant attention. This permits exclusion of overcharging of the capacitance of the open emitter of the input transistor with respect to the circuit leads which increases the signal delay.

There are entire series of methods of including the unused inputs.

The feed voltage limited to a value of 4.5 volts permits connection of the unused inputs directly to the power supply.

If the voltage of the power supply exceeds 4.5 volts, then as a result of danger of breakdown of the input it is necessary to limit the current by a resistance of more than 1 kilohm. In this case up to 20 inputs can be connected to one resistor.

It is possible to connect the unused inputs to the used input of the same logical element if the load capacity is not exceeded for an output voltage corresponding to the logical one level.

The unused input can be connected to the output of the unused inverting microcircuit, to the input of which the logical zero voltage is fed. When necessary, a logical zero voltage is fed to the individual unused inputs of the K155 series microcircuits, which is determined by the truth table of the corresponding microcircuit.

If in the microcircuits performing the AND-OR-NOT functions one of the AND circuits is not used, its inputs must be grounded. The unused inputs for connecting the expanders remain inactivated.

Recommendations with Respect to Admissible Values of the Input Signal Front and Decay. The signals which reach the input of the microcircuit must satisfy defined requirements, for otherwise fail-safe operation of the elements cannot be insured.

In particular, this pertains to the case where the IC are controlled from external sources. In the given case the durations of the input signal front and decay are especially critical.

For the K131, K155 series IC, the admissible duration of the input signal front and decay must not exceed 150 nanoseconds (except the PC K155LA7, K155LA8). For the K155LA7 and K155LA8 microcircuits the duration of the input signal front and decay is not critical.

However, when starting the K131 and K155 series IC from the PC K155LA7, K155LA8, the duration of the output signal front and decay of the latter, which depends on the duration of the input signal front and decay, must not exceed 150 nanoseconds.

For the series K158 microcircuits the maximum duration of the input signal front and decay is as follows: for the triggers, 150 nanoseconds; for logical elements, 500 nanoseconds.

Recommendations with Respect to Insurance of the Fan-Out Factors. In order to insure fitness of the logical microcircuits of different series under the condition of maintaining the parameters of the microcircuit stipulated in the technical specifications for them, it is necessary to satisfy the following requirements for all operating conditions.

a) The output voltages of the microcircuit generators in the open and closed state for a defined current (depends on the number of loads) must correspond to the input threshold voltages of the closed and open state of the load microcircuit considering the magnitude of the interference voltage, that is,

$$U^0_{\text{out g}} \leqslant U^0_{\text{threshold}} - U^0_{\text{interference}};$$
$$U^1_{\text{out g}} \geqslant U^1_{\text{threshold}} + U^1_{\text{interference}},$$

where $U^0_{\text{out.g}}$ and $U^1_{\text{out.g}}$ are the output voltages of the generator microcircuit in the open and closed state, respectively; U^0_{thresh} and U^1_{thresh} are the unblocking and blocking thresholds, respectively, with respect to the voltage of the load microcircuit; U^0_{int} and U^1_{int} are the admissible interference voltage for unblocking and blocking the load microcircuit, respectively.

b) The value of the total currents of all the load microcircuits connected to the output of the generator microcircuit must not exceed the values of the output current of the generator microcircuit in the open and closed states:

$$I^0_{\text{вых. г}} \geqslant \sum_{i=1}^{K_{\text{раз}}} I^0_{\text{вх. н}i}; \quad (1) \quad (2)$$
$$I^1_{\text{вых. г}} \geqslant \sum_{i=1}^{K_{\text{раз}}} I^1_{\text{вх. н}i}, \quad (3)$$

Key: 1. out.g; 2. fan-out; 3. inp. load i

where $I^0_{out.g}$ and $I^1_{out.g}$ are the output currents of the generator microcircuit in the open and closed states, respectively; $I^1_{inp.\ load\ i}$ and $I^0_{inp.load\ i}$ are the input currents of the load microcircuit in the closed and open states, respectively, for one logical input; $K_{fan-out}$ is the number of logical inputs of the load microcircuits connected to the output of the generator microcircuit.

c) The value of the total capacitance of the inputs of the load microcircuits (considering the wiring capacitance) for which the time parameters are regulated, that is,

$$C_{н.г} \geqslant \sum_{i=1}^{K_{раз}} C_{вх.нi} + \sum_{i=1}^{K_{раз}} C_{мi}$$

(1) (2)

Key: 1. load.g; 2. wire

where $C_{load.g}$ is the load capacitance of the generator microcircuit for which the time parameters are guaranteed (15 picofarads); $C_{inp.load\ i}$ is the maximum capacitance of the load microcircuit input (approximately 3 picofarads); $C_{wire\ i}$ is the capacitance of the wiring of one input of the load microcircuit with respect to the output of the generator microcircuit.

When necessary th total load capacitance of the PC-generator can reach a maximum load capacitance of 200 picofarads, but the dynamic parameters in this case are not regulated.

The fan-out of the generator microcircuit during joint operation of the logical microcircuits on each other is determined by the smaller number of the values of $K^0_{fan-out}$, $K^1_{fan-out}$ in accordance with the expressions:

$$K^0_{раз} = \frac{I^0_{вых.г}}{I^0_{вх.н}}; \quad (2)$$

(1)

$$K^1_{раз} = \frac{I^1_{вых.г}}{I^1_{вх.н}}; \quad (3)$$

$$K_C = \frac{C_{н}(4) - C_м}{C_{вх.н}}, \quad (5)$$

Key: 1. fan-out; 2. out. g; 3. inp. load; 4. load.g; 5. wire

where $K^0_{fan-out}$, $K^1_{fan-out}$ are the load capacities with respect to current of the generator microcircuit in the open and closed states; K_C is the capacitive load capacity of the generator microcircuit.

When grouping several inputs of one logical AND element, the current I^0_{inp} remains unchanged, and the current I^1_{inp} increases proportionally to the number of grouped inputs.

The inputs and outputs of the K131, K155, and K158 series microcircuits can be connected to any elements or circuits based on discrete components, including, for example, transistors, diodes, transformers, resistors, relay contacts, and so on if the magnitude and shape of the voltage and current at the input and output

of the PC satisfy the requirements of the technical specifications. In order to observe the requirements of the technical specifications for the input and output signals of the K131, K155 and K158 microcircuits it is necessary to design the circuits on the basis of discrete components in such a way as to exclude the appearance of voltage and current surges exceeding the admissible values at the inputs and outputs of the IC and also the requirements on the pulse front and decay.

The values of the fan-outs during operation IC of different series are presented in Tables 5-8 to 5-13.

Recommendations for Grouping the Microcircuits with Respect to Output. The grouping diagram for the K155LA8 microcircuit with respect to output is presented in Figure 5-127.

When connecting the resistance R_1 to the elements of the microcircuit K155LA8, the AND-NOT function is realized, and when grouping several elements with respect to output the AND-OR-NOT function is realized.

Table 5-9

(1) Номер нагружаемой серии	(2) Тип микросхемы	(3) Тип нагрузки — входы МС серии К155												
		К155ЛА1, К155ЛА2, К155ЛА3, К155ЛА4, К155ЛА6, К155ЛР1, К155ЛР3, К155ЛР4, К155КП7, К155ИЕ6, К155ИЕ7, К155ЛН1, К155ИД3, К155КП5, (4) К155Л115	К155ТВ1		К155ТЕ2			К155ТЕ4			К155ТЕ5		К155ТР1	
			3, 4, 5, 9, 10, 11	2, 12, 13	2, 3, 6, 7	14	1	6, 7	14	1	2, 3	1, 14	1, 2, 3, 4, 5, 8, 9	6
К155	К155ЛА1, К155ЛА2, К155ЛА3, К155ЛА4, К155ЛР1, К155ЛР3, К155ТВ1, К155ТЕ2, К155ТЕ4, К155ТЕ5, К155ТР1, К155ТМ5, К155ТМ7, К155ТЕ6, К155ТЕ7, К155ТЕ8, К155ТМ2	10	10	5	10	5	2	10	5	2	10	5	10	5
	К155ЛА6	30	30	15	30	15	7	30	15	7	30	15	30	15
	К155КР7	10	10	5	10	5	2	10	5	2	10	5	10	5
	К155ИМ1, out. 4, 5, 6	5 10	5 10	2 5	5 10	2 5	1 2	5 10	2 5	1 2	5 10	2 5	5 10	2 5
	К155ИМ2, out. 10 1, 12	5 10	5 10	2 5	5 10	2 5	1 2	5 10	2 5	1 2	5 10	2 5	5 10	2 5
	К155ИМ3, out. 14 2, 6, 9, 15	5 10	5 10	2 5	5 10	2 5	1 2	5 10	2 5	1 2	5 10	2 5	5 10	2 5
	К155ЛИ, К155ЛР5, К155КР5, К155ИД3	10	10	5	10	5	2	10	5	2	10	5	10	5

Key:

1. Loaded series No
2. Microcircuit type
3. Load type -- inputs of the K155 series IC
4. K155LA1, K155LA2, K155LA3, K155LA4, K155LA6, K155LR1, K155LR3, K155LR4, K155KP7, K55Iye6, K155IYe7, K155LI1, K155ID3, K155KP5, K155LP5

Table 5-10

(1) Номер нагружаемой серии	(2) Тип микросхемы	(3) Тип нагрузки — входы МС серии К155															
		К155ТМ5		К155ТМ7		К155ИМ1		К155ИМ2		К155ИМ3		К155ИЕ8		К155ТМ2			
		1, 2, 5, 6	3, 12	2, 3, 6, 7	4, 13	2, 8, 9, 11, 12, 13	3	13, 14	2, 3, 5	1, 7, 8, 16	3, 4, 10, 11, 13	1, 2, 3, 4, 10, 11, 12, 13, 14, 15	9	2, 12	3, 11	4, 10	1, 13
К155	К155ЛА1, К155ЛА2, К155ЛА3, К155ЛА4, К155ЛР1, К155ЛР3, К155ЛР4, К155ТВ1, К155ИЕ2, К155ИЕ4, К155ИЕ5, К155ИР1, К155ТМ5, К155ТМ7, К155ИЕ6, К155ИЕ7, К155ИЕ8, К155ТМ2	5	2	5	2	10	2	10	2	10	2	10	5	10	5	5	3
	К155ЛА6	15	7	15	7	30	6	30	7	30	7	30	15	30	15	15	10
	К155КП7	5	2	5	2	10	2	10	2	10	2	10	5	10	5	10	5
	К155ИМ1, out 4 5, 6	2 5	1 2	2 5	1 2	5 10	1 2	5 10	1 2	5 10	1 2	5 10	2 5	5 10	2 5	2 5	1 3
	К155ИМ2, out. 10 1, 12	2 5	1 2	2 5	1 2	5 10	1 2	5 10	1 2	5 10	1 2	5 10	2 5	5 10	2 5	2 5	1 3
	К155ИМ3, out. 14 2, 6, 9, 15	2 5	1 2	2 5	1 2	5 10	1 2	5 10	1 2	5 10	1 2	5 10	2 5	5 10	2 5	2 5	1 3
	К155ЛИ1, К155КП5, К155ЛР5, К155ИД3	5	2	5	2	10	2	10	2	10	2	10	5	10	5	10	5

Key:
1. No of loaded series
2. Type of microcircuit
3. Load type -- inputs of the K155 series IC

The value of a resistor R_1 is selected as a function of a required output grouping factor K_{group} and the number of loads $K_{fan-out}$ in accordance with the formula

$$\frac{U_{p.s.max}-U^0_{out}}{I^0_{out}-I^0_{inp}K_{fan-out}} \leq R_1 \leq \frac{U_{p.s.min}-U^1_{out}}{I^1_{inp}K_{fan-out}+I^1_{out}K_{group}},$$

where $K_{fan-out}$ is the actual fan-out; K_{group} is the output grouping factor; I^0_{inp}, I^1_{inp}, K^0_{out}, I^1_{out} are the input and output currents, milliamps; R_1 is the resistor, kilohms.

The resistance of the resistor R_1 is selected so that for the logical one voltage at the output the leakage currents of the output transistors and the input currents of the next input emitters of the transistors create a voltage drop on the resistor $U_{R_1} \leq 2.35$ volts, so that under any conditions a logical one voltage will be insured at the input of the microcircuits. In addition, the magnitude of the resistor R_1 must be such that for a logical zero voltage at the output of the cell the current through the resistor R_1 and the load current from the inputs of the load microcircuits will not exceed the maximum admissible magnitude of the collector current 16 milliamps.

Table 5-11

Номер нагружаемой серии (1)	Тип микросхемы (2)	(3) Тип нагрузки — входы МС серии К155: К155ЛА1, К155ЛА2, К155ЛА3, К155ЛА4, К155ЛА6, К155ЛР1, К155ЛР3, К155ЛР4, К155КП7, К155ИЕ6, И155ИЕ7, К155ЛИ1, К155ИД3, К155КП5, (4) К155ЛП5	К155ТВ1		К155ИЕ2			К155ИЕ4			К155ИЕ5		К155ЛР1	
			3, 4, 5, 9, 10, 11	2, 12, 13	2, 3, 6, 7	14	1	6, 7	14	1	2, 3	1, 14	1, 2, 3, 4, 5, 8, 9	6
К131	К131ЛА1, К131ЛА2, К131ЛР1, К131ЛР3, К131ЛР4, К131ЛА3, К131ЛА4	12	12	6	12	6	3	12	6	3	12	6	12	6
	К131ЛА6	28	28	14	28	14	7	28	14	7	28	14	28	14
	К131ТВ1	14	14	7	14	7	3	14	7	3	14	7	14	7
	К131ЛН1, К131ТМ2	12	12	6	12	6	3	12	6	3	12	6	12	6
К158	All types	2	2	1	2	1	—	2	1	—	2	1	2	1

Key:
1. No of loaded series
2. Type of microcircuit
3. Load type -- inputs of the K155 series IC
4. K155LA1, K155LA2, K155LA3, K155LA4, K155LA6, K155LR1, K155LR3, K155LR4, K155KP7, K155IYe6, K155IYe7, K155LI1, K155ID3, K155KP5, K155LP5

The values of the resistors calculated by the above-presented formula as a function of $K_{fan-out}$ and K_{group} are presented in Table 5-15.

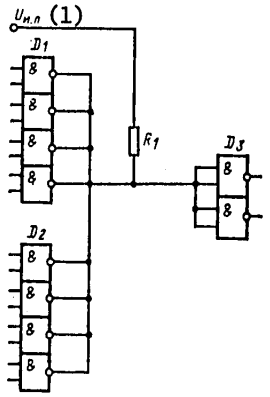


Figure 5-127. Grouping diagram for K155LA8 microcircuit with respect to output
D_1, D_2 -- K155LA8 microcircuit; D_3 -- K155LA3 microcircuit
Key: 1. $U_{p.s}$

Table 5-12

Номер нагружаемой серии (1)	Тип микросхемы (2)	(3) Тип нагрузки — входы МС серии К155																	
		К155ТМ5		К155ТМ7		К155ИМ1		К155ИМ2		К155ИМ3		К155ЛЕ8		К155ТМ2				К155ТЛ1	
		1, 2, 5, 6	3, 12	2, 3, 6, 7	4, 13	2, 8, 9, 11, 12, 13	3	13, 14	2, 3, 5	1, 7, 8, 16	3, 4, 10, 11, 13	1, 2, 3, 4, 10, 12, 13, 14	9	2, 12	3, 11	4, 10	1, 13	3	4, 6, 7
К131	К131ЛА1, К131ЛА2, К131ЛР1, К131ЛР3, К131ЛР4, К131ЛА3, К131ЛА4	6	3	6	3	14	2	12	3	12	3	12	6	12	6	6	4	12	6
	К131ЛА6	14	7	14	7	28	5	28	7	28	7	28	14	28	14	17	11	28	14
	К131ТВ1	7	3	7	3	14	2	14	3	14	3	14	7	14	7	8	5	14	7
	К131ЛН1, К131ТМ2	6	3	6	3	12	2	12	3	12	3	12	6	12	6	6	4	12	6
К158	All types	1	—	1	—	2	—	2	—	2	—	2	1	2	1	2	1	2	1

Key:
1. No of loaded series
2. Type of microcircuit
3. Load type -- inputs of the K155 series IC

On connecting the inputs of the series K158 microcircuit to the output of the K155LA8 microcircuit, the value of R_1 selected in accordance with Table 5-14 must be doubled, and on connecting the inputs of the K131 series microcircuits, it must be cut in half.

When loading the K155RU1 microcircuit for other types of microcircuits of the K155 series, a resistor must be connected between the output terminal of the K155RU1 microcircuit and the power supply, the magnitude of which is also determined by the above-presented formula.

The maximum number of groupings with respect to the "wired OR" circuit without considering negative effects on the dynamic parameters of the microcircuit is determined by the values of the output and input parameters, and it is calculated by the formula

$$K = \frac{\frac{U_{p.s} - U^1_{inp}}{R_{load.min}} - I^1_{inp} K_{fan-out}}{I^1_{out}}$$

Table 5-13

(1) Номер нагружаемой серии	(2) Тип микросхемы	(3) Тип нагрузки — входы МС серии К131								(4) Тип нагрузки — входы МС серии К158							
		К131ЛА1, К131ЛА2, К131ЛР1, К131ЛР3, К131ЛР4, К131ЛА3, К131ЛА4	К131ЛН1	К131ТВ1			К131ТМ2				К158ЛА1, К158ЛА2, К158ЛА3, К158ЛА4, К158ЛР1, К158ЛР3, К158ЛР4, К158ЛН1	К158ТВ1	К158ТМ2				К158ТР1	
				3, 4, 5, 9, 10, 11	2, 3	12	1, 13	2, 12	3, 11	4, 10		3, 4, 5, 9, 10, 11	2, 12, 13	2, 12	4, 10	3, 11	1, 13	2, 12, 13	3, 4, 5, 9, 10, 11
К155	К155ЛА1, К155ЛА2, К155ЛА3, К155ЛА4, К155ЛР1, К155ЛР3, К155ЛР4, К155ТВ1, К155ИЕ2, К155ИЕ4, К155ИЕ5, К155ИР1, К155ИЕ6, К155ИЕ7, К155ИЕ8, К155ТМ2	4	4	4	2	2	1	4	2	2	20	6	20	10	10	6	10	10
	К155ЛА6*	12	12	12	6	6	4	12	6	6	60	60	20	60	30	30	20	22	30
	К155КП7	6	8	6	3	5	3	8	4	5	40	40	16	40	25	20	16	13	25
	К155ИМ1, out. 4 5, 6	2 4	2 4	2 4	1 2	1 2	— 1	2 4	1 2	1 2	10 20	10 20	3 6	10 20	5 10	5 10	3 6	5 10	5 10
	К155ИМ2, out. 10 1, 12	2 4	2 4	2 4	1 2	1 2	— 1	2 4	1 2	1 2	10 20	10 20	3 6	10 20	5 10	5 10	3 6	5 10	5 10
	К155ИМ3, out. 14 2, 6, 9, 15	2 4	2 4	2 4	1 2	1 2	— 1	2 4	1 2	1 2	10 20	10 20	3 6	10 20	5 10	5 10	3 6	5 10	5 10
	К155ЛИ1, К155ЛР5, К155КП5	6	8	6	3	4	2	8	4	4	40	40	13	40	20	20	13	13	20
	К155ИД3	6	8	6	3	4	2	8	4	4	40	40	13	40	20	20	13	13	20

Key:
1. No of loaded series
2. Type of microcircuit
3. Load type -- inputs of the K131 series IC
4. Load type -- inputs of the K158 series IC

where K is the maximum number of groupings; $R_{load.min}$ is the minimum value of the load resistance connected to the circuit made up of the power supply and the collector of the output transistor of the read amplifier of the K155RU1 microcircuits:

$$R_{load.min} = \frac{U_{p.s} - U^0_{out}}{I^0_{out} - I^0_{inp} K_{fan-out}}.$$

For a large number of IC outputs grouped with the help of the "wired OR" it is necessary to consider the dependence of the dynamic parameters of the IC on the capacitance of the IC themselves and the wiring capacitance.

In order to increase the load capacity of the IC, it is permissible to combine the inputs and outputs of two logical elements of the IC in one case. Here the load capacity increases by 1.9 times. The application diagrams are presented in Figure 5-128, a, b.

Table 5-14

(1) Номер нагружаемой схемы	(2) Тип микросхемы	(3) Тип нагрузки — входы МС серии К131									(4) Тип нагрузки — входы МС серии К158								
		К131LA1 К131LA2 К131LR1 К131LR3 К131LR4 К131LA3 К131LA4	К131LN1	К131TV1			К131TM2				К158LA1 К158LA2 К158LA3 К158LA4 К158LR1 К158LR3 L158LR4 К158LN1	К158TV1		К158TM2				К158TR1	
				3, 4, 5, 9, 10, 11	2, 13	12	1, 13	2, 13	3, 11	4, 10	3, 4, 5, 9, 10, 11	2, 12, 13		2, 12	4, 10	3, 11	1, 13	2, 12, 13	3, 4, 5, 9, 10, 11
К131	К131LA1, К131LA2, К131LR1, К131LR3, К131LR4, К131LA3, К131LA4	10	10	5	2	2	1	5	2	2	25	25	8	25	12	12	8	12	25
	К131LA6*	20	20	20	10	10	6	20	10	10	70	70	23	70	35	35	23	27	50
	К131TV1	10	10	7	3	3	2	7	3	3	35	35	11	35	17	17	11	17	25
	К131LN1, К131TM2	8	10	5	2	2	1	5	2	2	25	25	8	25	12	12	8	12	25
К158	All types	1	2	1	—	1	—	2	1	1	10	10	3	10	5	5	3	3	5

(5) *Коэффициент разветвления выбирается не более указанного в таблице с учетом обеспечения $C_{\Sigma н} = C_{н.\,max}$, без учета емкости монтажных проводников $C_м$.

Key:

1. No of loaded series
2. Type of microcircuit
3. Load type -- inputs of the K131 series IC
4. Load type -- inputs of the K158 series IC
5. *The fan-out is selected no more than that indicated in the table considering the insurance of $C_{\Sigma load} = C_{load.max}$ without considering the capacitance of the wiring C_{wire}.

In order to construct memory circuits with a number of bits in the information word of more than one for the K155RU1 microcircuit the address and control inputs of the IC are grouped within the limits of the load capacity of the controlling elements.

Operation of the IC on the Delay Line. For operation on the delay line it is recommended that the K155LA8 microcircuit be used in accordance with the diagram presented in Figure 5-129.

The recommended delay lines are types MLZ and LZT with wave impedance of 600 ohms and delay time of no more than 1 microsecond.

The input pulse duration must be:

No less than 0.5 microsecond for a delay time of more than 0.5 microsecond;

Table 5-15.

(1) Число нагрузок логических элементов серии К155 $K_{раз}$	(2) Сопротивление нагрузочного резистора (кОм) при объединении K выходов ($K_{об.вых}$) МС типа К155ЛА8										
	(3) Максимальное										(4) Минимальное 1—10
	1	2	3	4	5	6	7	8	9	10	
1	7,24	3,89	2,66	2,02	1,62	1,36	1,17	1,030	0,917	0,827	0,354
2	6,37	3,62	2,53	1,94	1,58	1,33	1,15	1,010	0,901	0,814	0,398
3	5,68	3,39	2,41	1,87	1,53	1,29	1,12	0,990	0,887	0,802	0,455
4	5,12	3,18	2,31	1,81	1,49	1,26	1,10	0,972	0,872	0,790	0,532
5	4,67	3,00	2,21	1,75	1,45	1,23	1,07	0,955	0,857	0,778	0,638
6	4,28	2,84	2,12	1,69	1,41	1,20	1,05	0,937	0,843	—	0,797
7	3,96	2,69	2,04	1,64	1,37	1,18	—	—	—	—	1,060
8	3,68	2,56	1,96	—	—	—	—	—	—	—	1,600
9	3,44	—	—	—	—	—	—	—	—	—	3,190

Key:
1. No of loads of logical elements of the K155 series $K_{fan-out}$
2. Resistance of the load resistor (kilohms) when grouping K outputs ($K_{group.out}$) of the IC type K155LA8
3. Maximum
4. Minimum 1-10

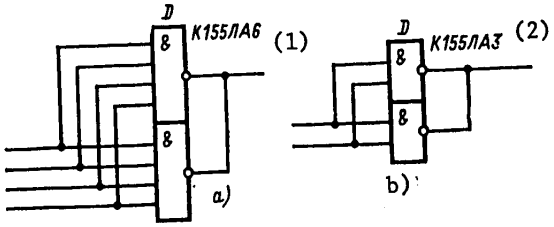


Figure 5-128. Operating diagram of parallel-included elements

Key:
1. K155LA6
2. K155LA3

No less than 0.3 microsecond for a delay time from 0.1 to 0.5 microsecond;

No less than 0.15 microsecond for a delay time less than 0.1 microsecond.

When it is necessary to have a delay time of more than 1 microsecond it is recommended that several delay lines be included by the diagram presented in Figure 5-130.

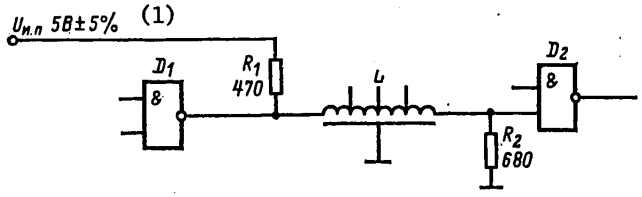


Figure 5-129. Circuit diagram of a delay line at the output of a K155LA8 element.
D_1 -- K155LA8 microcircuit; D_2 -- K155LA3 microcircuit;
L -- MLZ-1-600 delay line

Key:
1. $U_{p.s}$ 5 volts±5%

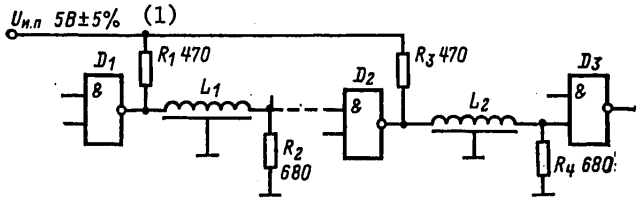


Figure 5-130. Staged circuit diagram of delay lines.
D_1, D_2 -- K155LA8 microcircuit; D_3 -- K155LA3 microcircuit;
L_1, L_2 -- MLZ-1-600 delay line

Key:
1. $U_{p.s}$ 5 volts±5%

It is permissible to connect only one input of the K155 series microcircuit at the delay line output.

It is permissible to connect one input of any microcircuit of the K155 series to any tap of the delay line; here the matching resistor is installed at the end of the line. It is recommended that the signal be picked up from one tap of the line or from only the end of the delay line. It is necessary to transmit the signal through the delay line by low level.

Operation of the IC on a Relay. The matching circuit of the K155LA7 microcircuit with the type RES-64A relay is presented in Figure 5-131.

The matching circuit of the K155LA8 microcircuit with the type RES-48 relay is presented in Figure 5-132.

Operation of the IC on Display Elements. It is recommended that the NSM6,3-20 type incandescent tube be used as the logical signal display elements. The recommended circuit diagram is presented in Figure 5-133. The lamp burns in the presence of high voltage levels at the inputs of the K155LA7 microcircuit. The recommended matching circuit for the K155LA7 microcircuit with the IV-9 incandescent display is presented in Figure 5-134.

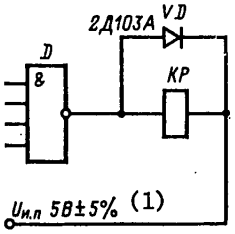


Figure 5-131. Matching circuit of the K155LA7 microcircuit with the RES64A type relay
Key:
1. $U_{p.s}$ 5 volts±5%

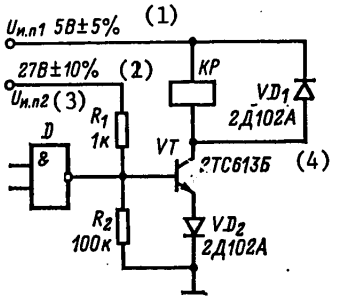


Figure 5-132. Matching circuit of the K155LA8 microcircuit with the RES48 type relay
Key:
1. $U_{p.s}$1 5 volts±5%
2. 27 volts±10%
3. $U_{p.s}$2
4. 2TS613B

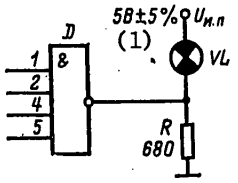


Figure 5-133. Matching circuit of the K155LA7 microcircuit with an incandescent tube
Key:
1. 5 volts±5% $U_{p.s}$

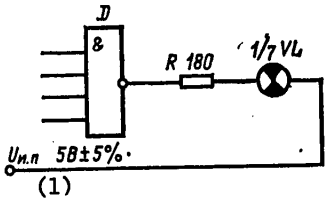


Figure 5-134. Matching circuit of the K155LA7 microcircuit with the IV-9 incandescent display
Key:
1. $U_{p.s}$ 5 volts±5%

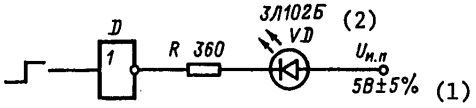


Figure 5-135. Display circuit using a light diode switched on from a high voltage level.
D -- K155LA8 microcircuit or K155LA7 microcircuit
Key:
1. $U_{p.s}$ 5 volts±5%
2. 3L102B

In cases where the red glow of the display is satisfactory and high restrictions are not imposed on its brightness characteristics, it is recommended that the light diode 3L102B be used as the logical signal display element.

The display circuit using a light diode with switch-on from a high voltage level is presented in Figure 5-135. In this circuit it is also possible to use the K155LA1, K155LA2, K155LA3, K155LA4, K155LA6 microcircuits.

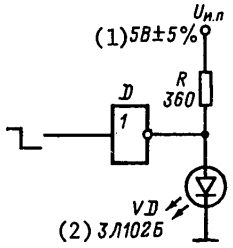


Figure 5-136. Display circuit using a light diode with switch-on from a low voltage level.
D -- K155LA8 microcircuit or K155LA7 microcircuit
Key:
1. $U_{p.s}$ 5 volts±5%
2. 3L102B

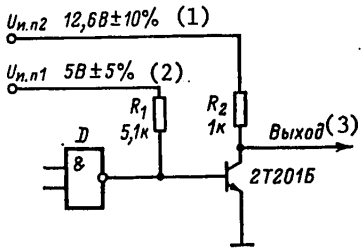


Figure 5-137. Circuit diagram for connecting the K155LA8 microcircuit to a switching transistor stage
Key:
1. $U_{p.s2}$ 12.6 volts±10%
2. $U_{p.s1}$ 5 volts±5%
3. Output

The display circuit using a light diode with switch-on from a low voltage level is presented in Figure 5-136.

The matching circuits of the K155LA8, K155LA7 microcircuits with the switching transistor stages are presented in Figures 5-137 and 5-138.

The input pulse expansion circuit to a given value and the diagram explaining the operating principle of the circuit are presented in Figure 5-139.

In Figure 5-140 we have the short pulse shaping circuit with respect to the input signal decay executed from K155LA7 and K155LA8 microcircuits. The circuit is designed for shaping pulses with a duration of 0.9 to 1 microsecond by the input signal decay. The pulses are generated as a result of the introduction of the capacitance C into the circuit insuring a signal propagation delay by the indicated time.

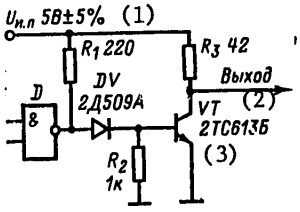


Figure 5-138. Diagram of the coupling of the K155LA7 microcircuit to a switching transistor stage
Key:
1. $U_{p.s}$ 5 volts±5%; 2. Output; 3. 2TS613B

The short pulse shaping circuit and diagram explaining the operating principle of this circuit are presented in Figure 5-141.

The pulse shaper circuit with respect to the input signal front and decay and also the operating time diagram are presented in Figure 5-142.

In Figures 5-143 and 5-144 we have the diagrams of square pulse generators and the diagram explaining the operating principle of these circuits.

The diagram of a single pulse generator and the diagram explaining the operating principle of this circuit executed from K155LA3 and K155LR1 microcircuits are presented in Figures 5-145 and 5-146.

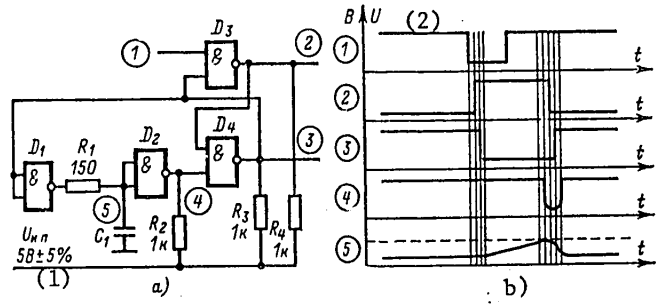


Figure 5-139. Input pulse broadening unit. The input pulse broadening circuit (a) and time diagram (b).
C_1 -- selected as a function of the output pulse duration;
D_1-D_4 -- K155LA8 microcircuit.

Key:
1. $U_{p.s}$ 5 volts±5%
2. U, volts

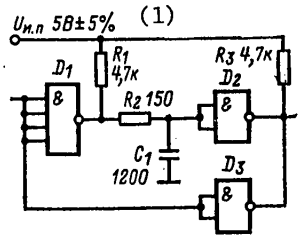


Figure 5-140. Diagram of a short pulse shaper with respect to input signal decay.
D_1 -- K155LA7 microcircuit; D_2-D_3 -- K155LA8 microcircuit

Key:
1. $U_{p.s}$ 5 volts±5%

In Figure 5-147 we have the circuit for elimination of the jarring of the contacts executed from a K155LA3 microcircuit.

For transmission of the information between the units with significant spacing between them it is recommended that the K109LI1 (A, B) be used which operates directly from the K155 series microcircuits and can be loaded on the K155 series microcircuits through a coaxial cable with 75 ohm wave impedance.

In order to facilitate the operating conditions of the K109LI1 microcircuit during operation on a cable it is recommended that the information be transmitted by a high signal level. When using the circuit depicted in Figure 5-148, a the pulse duration must be no less than 200 nanoseconds; when using the circuit in Figure 5-148, b the pulse duration is no less than 1 microsecond.

During operation of the IC on a matching cable with wave impedance of 75 ohms by the diagram in Figure 5-148, a, it is permissible to connect no more than four IC inputs series K155 to the cable output, and by the diagram in Figure 5-148, b, one input.

The maximum cable length according to the diagram in Figure 5-148, a is selected in such a way that the voltage drop on the cable does not exceed 50 millivolts.

The maximum cable length with respect to the diagram in Figure 5-148, b is no more than 100 meters.

The unused inputs of the K109LI1 microcircuit can be connected to the +5 volts±10%.

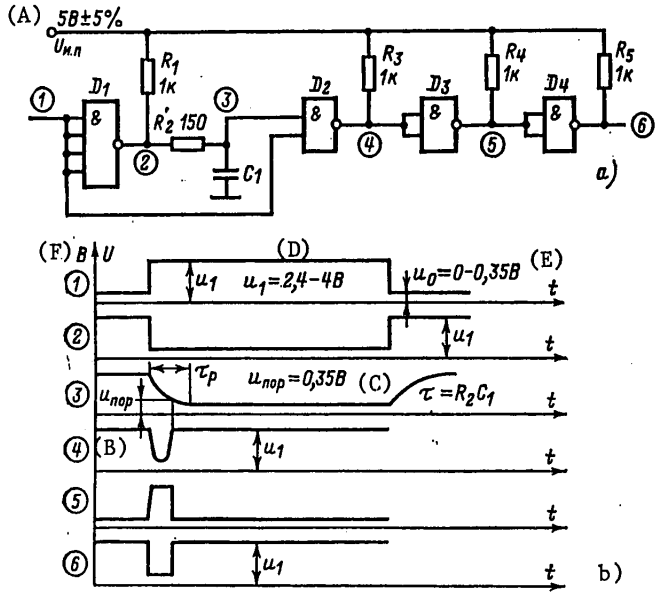


Figure 5-141. Diagram of a short pulse shaper (a) and operating time diagram (b).

C_1 -- the capacitor is selected as a function of the output pulse duration; D_1 -- K155LA7 microcircuit; D_2-D_4 -- K155LA8 microcircuit

Key: A. 5 volts±5% $U_{p.s}$; B. U_{thresh}; C. U_{thresh}=0.35 volts; D. u_1=2.4-4 volts E. u_0=0-0.35 volts; F. U, volts

The K109LI1 microcircuit can be loaded on the series K155 IC through a MGShVE type shielded conductor. It is permissible to connect no more than two inputs of the K155 series IC to the output of the shielded conductor with a conductor length of 5 meters and is no more than one input with a conductor length to 30 meters.

The circuit diagram is presented in Figure 5-149, a, b.

Recommendations with Respect to Insuring Noiseproofness During the Structural Design of Equipment. The feed voltage of the units and modules executed from the series K155 IC (the "ground" and "feed" buses) must be distributed by wires with the lowest possible resistance.

When using multilayer printed circuit boards it is recommended that the "feed" buses be laid out in one layer, and the "ground" buses in another adjacent layer; the buses should be located one above the other. In the presence of a free area in the layer it is recommended that it be used to enlarge the surface of the "ground" bus.

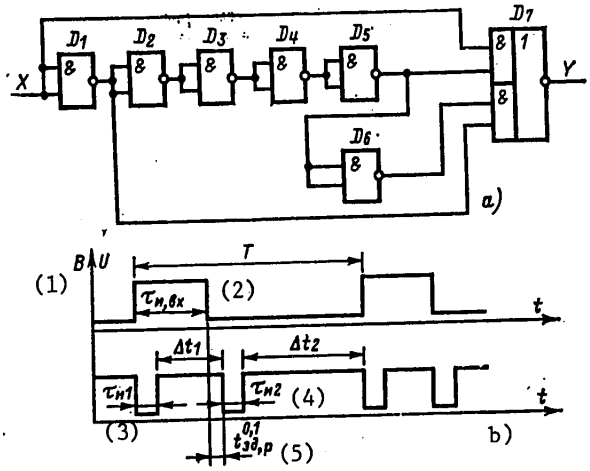


Figure 5-142. Diagram of a pulse shaper with respect to input signal front and decay (a) and operating time diagram (b).
D_1-D_6 -- K155LA3 microcircuit; D_7 -- K155LR1 microcircuit;
$\Delta t_1=\tau_{i.inp}-\tau_i+t^{0,1}_{del,p}$; $\Delta t_2=T\cdot\tau_{load.inp}-\tau_{i2}-t^{0,1}_{del,p}$; $\tau_{load\ 1}\tilde{}\tau_{load\ 2}=nt^{1,0}_{del,p}$ + $(n-1)t^{1,0}_{del,p}$; n is an even number of elements participating in the signal delay

Key:
1. U, volts
2. $\tau_{i,\ inp}$
3. τ_{i1}
4. τ_{i2}
5. $t_{del,\ p}$

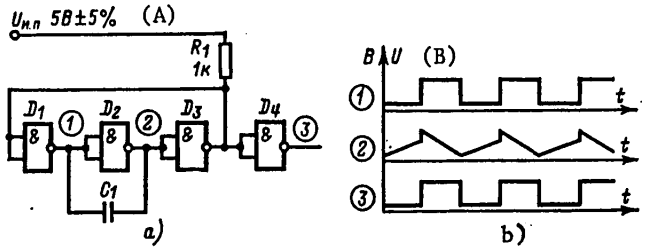


Figure 5-143. Diagram of a square pulse generator (version I) (a) and operating time diagram (b).
D_1-D_3 -- K155LA8 microcircuit; D_4 -- K155LA3 microcircuit;
C_1 -- the capacitor is selected as a function of the output pulse duration (no more than 0.003 microfarads)

Key:
A. $U_{p.s}$ 5 volts±5%
B. U, volts

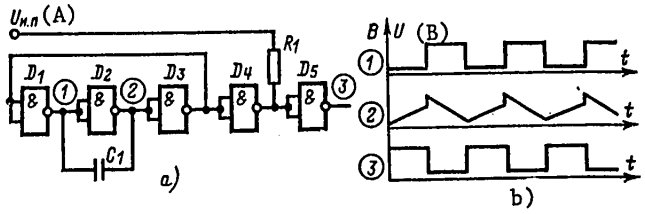


Figure 5-144. Diagram of a square pulse generator (version II) (a) and operating time diagram (b).
C_1 -- the capacitor is selected as a function of the output pulse duration (no more than 1 microfarad); D_1-D_4 -- K155LA8 microcircuit; D_5 -- K155LA3 microcircuit; R_1 -- resistor 1 kilohm ± 10%; $U_{p.s}$ -- power supply +5 volts±5%

Key:
A. $U_{p.s}$
B. U, volts

The low-frequency interference penetrating to the system by the feed buses must be blocked using a capacitor with a capacitance of 0.1 microfarad for the IC connected between the "feed" and "ground" terminals directly to the locations of the beginning of the printed circuit wiring.

The decoupling capacitances with respect to high frequency must be uniformly distributed over the entire area of the printed circuit board with respect to the IC calculating one capacitor for a group of no more than 10 microcircuits, a capacitance no less than 0.002 microfarads per microcircuit.

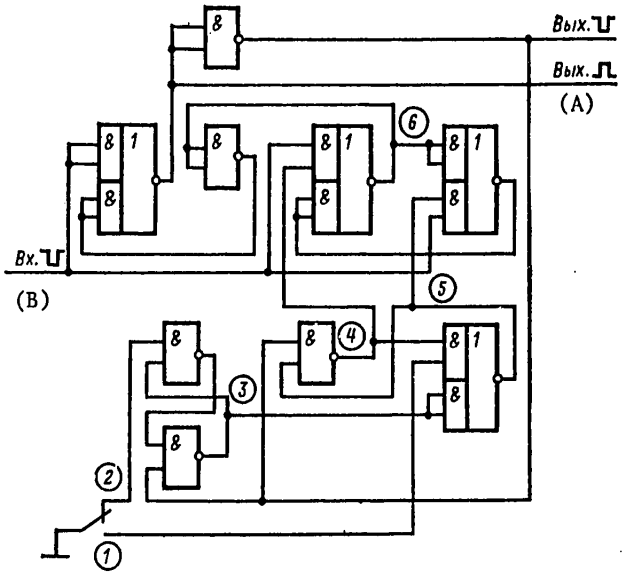


Figure 5-145. Diagram of a single pulse generator

Key:
A. out
B. input

The decoupling capacitor installed in direct proximity to the microcircuit forms a circuit with low resistance to high frequencies.

The capacitors are installed on the same side of the board that the IC are located on in direct proximity to them. For blocking the high-frequency pulsations it is necessary to use inductionless capacitors.

In the presence of K155LA6, K109LI1 and other IC of the K155 series with increased degree of integration on the printed circuit board, the capacitors for each of these microcircuits with a capacitance of 0.1 microfarad are installed if necessary in direct proximity to the IC.

The microcircuit with increased degree of integration of series K155 must be installed on the boards as close as possible to the plugs and directly on the "ground" buses.

In order to supply the feed voltage and connect the "ground" bus it is recommended that the edge contacts of the plug be used.

Recommendations with Respect to Electric Communications Lines. In accordance with the purpose, the electric communication lines are divided into lines for transmitting information, for synchronization, for display, for commutation and the "feed" and "ground" buses.

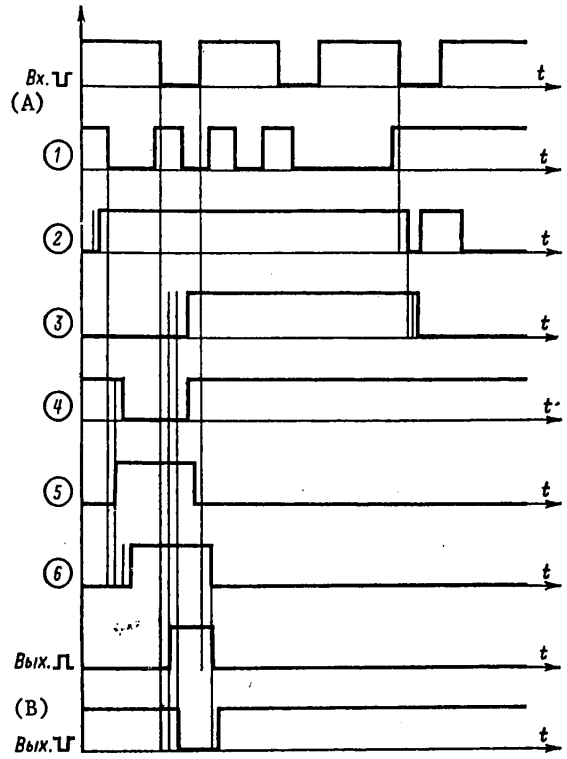


Figure 5-146. Operating time diagram of a single pulse generator

Key:
A. input
B. output

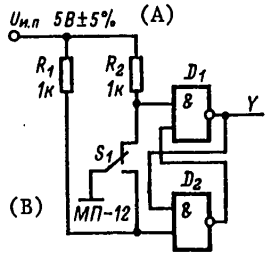


Figure 5-147. Circuit for eliminating jarring of the contacts

Key:
A. $U_{p.s}$ 5 volts±5%
B. MP-12

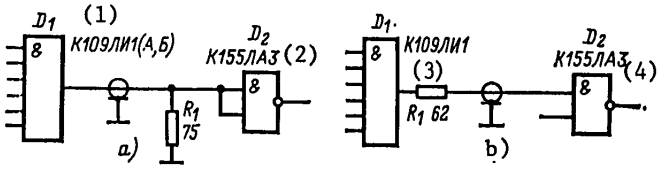


Figure 5-148. Circuit diagram of a matched cable RK-75 to the output of the K1091I1 (A, B) element.
a -- parallel matching; b -- series matching

Key:
1. K109LI1(A, B)
2. K155LA3
3. K109LI1
4. K155LA3

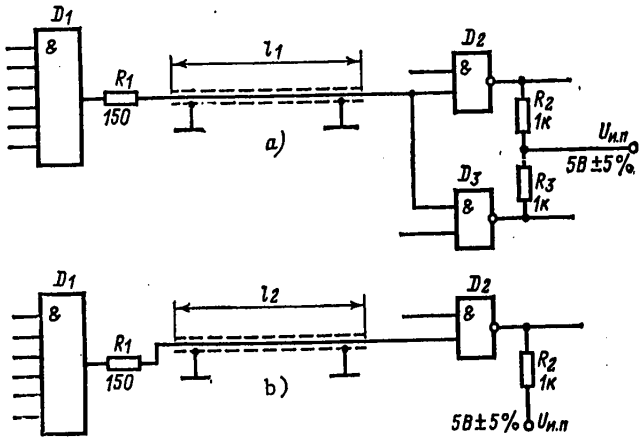


Figure 5-149. Matching circuit of the K109LI1 microcircuit with the communication line and the K155LA8 microcircuit.
D_1 -- K109LI1 microcircuit; D_2 -- K155LA8 microcircuit; ℓ_1 -- conductor MGShVE-0.35 mm^2 to 5 meters; ℓ_2 -- conductor MGShVE-0.35 mm^2 to 30 meters

The information communication lines are designed to transmit information signals. Within the limits of the printed circuit board it is recommended that these lines be made using printed circuitry.

The wires on different sides of the board or in adjacent layers must cross at an angle of 45 or 90°. The wires must be as short as possible. The maximum admissible length of printed parallel wires located on one side of the board or in one layer with a printed wire width of 0.5-1.5 mm must not exceed the values presented in Table 5-16 (the length of the printed wires is presented in millimeters).

Table 5-16

(1) Количество параллельных проводников	(2) Интервалы между печатными проводниками, мм				
	0,5	1,0	1,5	3,0	5,0
2	100	120	130	150	170
3	60	70	75	90	100
4	50	60	65	75	80
5	40	50	60	65	70

Key:
1. No of parallel wires
2. Intervals between printed wires, mm

Note. The admissible length of the printed wires not going beyond the limits of the printed circuit board can be increased by 40% with respect to the values indicated in the table.

It is recommended that the information communication lines between boards be realized using panel mounting which can be structurally in the form of a printed circuit board or panel having a shielding coating on the wiring side. The shielding must be connected to the "ground" bus of the printed circuit boards.

The length of the communication lines on the panel mounting when executing them by panel mounting is defined as the difference of the length obtained according to Table 5-15 considering the note and the length of the communication lines on the board.

If the length of the information communication lines exceeds 20 cm, it is recommended that they be made using dense-packed point-to-point wiring. The communication lines up to 20 cm long for asynchronous devices and up to 30 cm for synchronous devices are made from single wires.

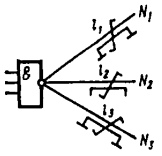
It is permissible to connect up to 5 radial lines with a total length of no more than 50 cm to the output of one transmitting element.

The communication lines from 0.2 to 1 meter long within the limits of the panel are made using unmatched cabled pairs. It is permissible to connect no more than 3 cabled pairs with a total length of no more than 2 meters to the output of one transmitting element.

When organizing the connections using unmatched cabled pairs the delay time of the signals increases and can be determined by Table 5-17.

The return wires of the cabled pairs must be "grounded" on the transmitting and receiving ends. The length of a separate part of a cabled pair must be no more than 3 cm. It is permissible to connect no more than 3 return wires of the cabled pairs to one contact of the plug.

Table 5-17

Coupling diagram	Recommendations with respect to application	Delay increment at the output of the transmitting element		Delay increment at the output of the communication line	
		$\Delta t^{0,1}_{del}$, nanoseconds	$\Delta t^{1,0}_{del}$, nanoseconds	$\Delta t^{0,1}_{del}$, nanoseconds	$\Delta t^{1,0}_{del}$, nanoseconds
 ℓ_i -- cabled pair or cable with wave impedance of 100 ohms	For the radial layout method the load is concentrated at the end of a communication line For the combined layout method the load is distributed arbitrarily along the length of the communications line $\ell_\Sigma=\ell_1+\ell_2+\ell_3\leq 2$ meters Length of each communication line no more than 1 meter	$8\ell_\Sigma$	$6\ell_\Sigma$	$8\ell_\Sigma+5\ell_i$	$6\ell_\Sigma+6\ell_i$

It is permissible to separate the taps from the unmatched cabled pair by a single wire within the limits of the load capacity of the transmitting IC; here the total length of the taps must not exceed 0.2 meter.

In the communication line laid by a cabled pair, separate sections can be run by a single wire; here the total length of the single wires in the given communication line must not exceed 0.2 meter, and the length of the entire communication line is no more than 1 meter.

When laying out communication lines it is necessary to arrange them in such a way as to permit simplification of the communication line and insure maximum length of it.

Communication lines from 1 to 3 meters not going beyond the limits of the device must be made as matched cabled pairs. The matched communication lines more than 3 meters long and also communication lines going beyond the limits of the device must be made using a coaxial cable with wave impedance of 100 ohms. The communication lines are matched using the 82 ohm resistor with admissible deviation of the resistance by $\pm 5\%$. The resistor must be installed directly at the output of the transmitting IC according to Table 5-17.

The length of a coaxial cable and number of inputs connected directly to the output of the transmitting element and also at the output of the communication line must not exceed the values indicated in Table 5-17. When determining the increment of the propagation delay Δt_{del} (Table 5-18) the length ℓ of the communication line must be taken in meters.

The load N_1 is connected by a single wire no more than 0.2 m long or a cabled pair no more than 0.5 meter long.

It is permissible to transmit information signals within the limits of the device using a shielded conductor with mandatory sending of a gating signal over the coaxial cable. The gating signal must be delayed with respect to the information signal by the time of effect of the transient processes, and the pulse duration of the information signal must be selected from the condition

$$\tau_i > t_{del.gate} + t_{switch},$$

where $t_{del.gate}$ is the delay time of the gating signal with respect to the information signal; t_{switch} is the switching time of the circuit receiving the information.

The communication lines for transmitting synchronization signals with printed circuitry must be removed from the information lines and from the synchronization lines of another phase by a distance of no more than 2.5 mm or shielded by a "grounded" printed wire connected to the common "ground" at one point. The width of the printed shielded wire must be 2 or 3 times greater than the width of the synchronization circuit wire. The length of the communication lines within the limits of the printed circuit board is selected considering the data in Table 5-17.

The communication lines for the synchronization signals within the limits of the panel can be laid out using a cabled pair to 35 cm long or a single wire to 10 cm long. From the cabled pair it is permissible to make taps by a single wire to 10 cm long, where the total length of the single wire must not exceed 20 cm.

The synchronization signal communication lines within the limits of the device with a length of more than 35 cm can be executed using a matched or unmatched coaxial cable with a length of no more than 50 cm.

It is recommended that the communication lines from the output of the IC to the display elements be made by single wires which can be laid in a bunched conductor. The length of the communication lines in this case will be determined from the conditions of insuring maximum admissible voltage applied to the output of the IC (5.25 volts for K155LA8, 7 volts for K155LA7, 60 volts for K155ID1).

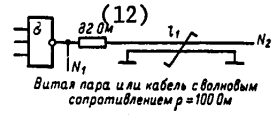
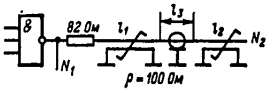
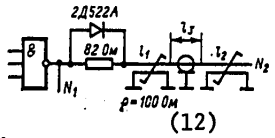
It is recommended that the commutation communication lines (the lines between switches, toggle switches, relay contacts and microcircuit) be made with shielded conductor.

The application of single wires to 0.3 meter long and cabled pairs to 3 meters is permissible.

It is not permissible to lay information, commutation and display communication lines in one bunched conductor.

Single wires cannot be laid in bunched conductors either separately or with cabled pairs. Unmatched and matched cabled pairs can be laid in bunched conductors or groups of conductors without a tie and also in stubs.

Table 5-18

(1) Схема связи	(2) Количество элементов нагрузки N_1	N_2	(3) Приращение задержки срабатывания передающего элемента $\Delta t^{0,1}_{зд}$, нс (4)	$\Delta t^{1,0}_{зд}$, нс (5)	(6) Приращение задержки на выходе линии связи $\Delta t^{1,0}_{зд}$, нс (4)	$\Delta t^{1,0}_{зд}$, нс (5)	(7) Длина участков линии связи, м (8) одиночная связь	(9) Жгут	(10) Тип передающего элемента
(12)  Витая пара или кабель с волновым сопротивлением ρ = 100 Ом (11)	5 2	1 2	8	6	8+5l	6+5l	$l_1 \leqslant 3$	—	(13) Любой логический элемент с нагрузочной способностью $K_{раз} \geqslant 10$
	5 2	1 2	8+10l	6	8+15l	6+5l	—	$l_1 \leqslant 3$	
	17 6	1 2	8	6	8+5l	6+5l	$l_1 \leqslant 3$		Только К155ЛА6 (14)
	17 6	1 2	8	6	8+5l	6+5l	$l_1+l_2 \leqslant 3$ $\Sigma l \leqslant 10$		Только К155ЛА6 (14)
 (12)	0	2	8+2l	6	8+5l	6+5l	$l_1 \leqslant 0.5$ $l_2 \leqslant 0.5$ $l_3 \leqslant 30$		Только К155ЛА6 (14)

Key:

1. Coupling diagram
2. No of load elements
3. Increment of the response delay of the transmitting element
4. $\Delta t^{0,1}_{del}$, nanoseconds
5. $\Delta t^{1,0}_{del}$, nanoseconds
6. Delay increment at the output of the communication line
7. Length of the communication line segments, meters
8. Single coupling
9. Bunched conductor
10. Type of transmitting element
11. Cabled pair or cable with wave impedance ρ=100 ohms
12. ohms
13. Any logical element with load capacity $K_{fan-out} \geq 10$
14. Only K155LA6

When expanding the logical possibilities of K155LA1, K155LR1, K155LR3, K155LR4 microcircuits using expander microcircuits, the length of the communication lines between the IC and the expanders must not exceed 4 cm. Here the total length of the communication lines must not exceed 12 cm.

The terminals 7 of the K155LD1 and K155LD3 microcircuits must be "grounded."

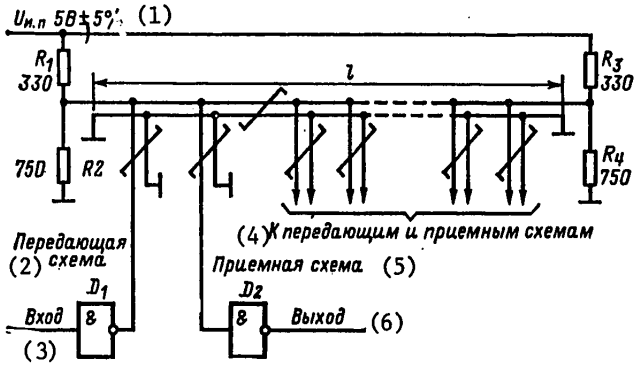


Figure 5-150. Diagram of the organization of an intrainstrument code main.
D_1 -- K155LA7 microcircuit; D_2 -- K155LA3 microcircuit; cabled pair $l \leq 3$ meters

Key:
1. $U_{p.s}$ 5 volts±5%
2. Transmitting circuit
3. Input
4. To the transmitting and receiving circuit
5. Receiving circuit
6. Output

The functional diagram of the organization of an intrainstrument code main executed from cabled pairs is presented in Figure 5-150.

The maximum coupling length from the transmitting circuit to the receiving circuit must not exceed 3 meters. The K155LA7 microcircuit (to 8 circuits) is used as the transmitting circuits, and the series K131, K155, and K158 microcircuits, as the receiving circuits. Here it is necessary to consider the increased load on the transmitting circuit. The transmitting and receiving circuits can be connected at any point of the main.

The duration of the pulses transmitted over the main must be no less than 0.4 microsecond.

The length of the communication lines during joint operation of the K131, K155 and K158 series microcircuits must be decreased by 1.5 times if the transmitting elements are the K131 series microcircuits, and it can be increased by 1.5 times if the K158 series microcircuits are used as the transmitting element by comparison with the recommendations presented for the K155 series microcircuits.

The recommendations presented in the present section for insurance of noiseproofness do not describe all the possible cases of protection against interference; therefore in order to create the optimal structural design additional studies are necessary in each specific case.

Examples of Constructing Functional Units of Equipment. Some circuit engineering principles of the implementation of complex logical functions and the construction of the functional units based on the series K131, K155 and K158 microcircuits are presented below.

The functional diagram of an asymmetric counting trigger based on six AND-NOT elements is presented in Figure 5-151. Its operating time diagrams are presented in Figure 5-152. The trigger is set to the logical zero state on simultaneous feed of the logical zero voltage to the inputs of the elements D_4 and D_6 independently of the voltage level on the counting input C. For a logical zero voltage on the counting input the trigger can be set to logical zero on feeding a logical one voltage on the counting input to the input of the element D_6.

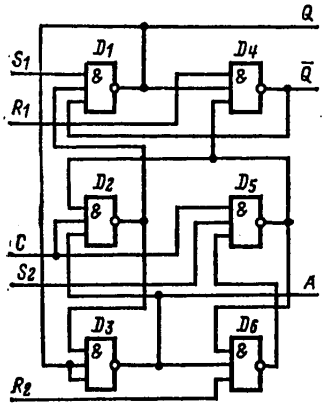


Figure 5-151. Functional diagram of a counting trigger

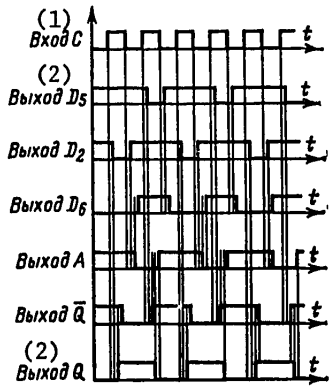


Figure 5-152. Time diagram of a counting trigger
Key:
1. Input C
2. Output ...

The trigger is set to the logical one state with logical zero voltage on the counting input by feeding a logical zero voltage to the input of the element D_1; with a logical one voltage on the counting input and the "set 0" inputs (R_1, R_2), by feeding the logical zero voltage to the input of the element D_5.

With simultaneous feed of zero potential to the inputs of the elements D_1 and D_5, the logical one state is set independently of the potential of the counting input. Therefore on entering an arbitrary code counter and when setting the reversible counters to the logical "0" state it is necessary to feed the setting pulses to both "set 1" inputs S_1, S_2 simultaneously or separately depending on the type of operation.

When constructing the summing counter, signals are fed to the inputs of the subsequent bits from the "0" output (the elements D_4 of the preceding trigger), and when constructing the subtracting counter, from the "1" output (the elements D_1 of the preceding triggers). At the output of the element D_3 the input pulses of negative polarity with frequency $f_{inp}/2$ are repeated.

The minimum setting pulse duration for the trigger in the

$$\tau_{i.set,min}=t^{0,1}_{del.p.max}+t^{1,0}_{del.p.max}.$$

The minimum operating cycle duration of a single trigger

$$t_{min}=3t^{0,1}_{зд.p}+2t^{1,0}_{зд.p}.$$
(1) (1)

Key: 1. del.p

The signal propagation delay by one bit when constructing a series counter

$$t^{(1)}_{зд.p1p}=t^{0,1}_{зд.p}+t^{1,0}_{зд.p}.$$
(2)

Key: 1. del, p 1 bit; 2. del, p

The duration of the input pulses of negative polarity

$$\tau_{и}>t^{0,1}_{зд.p}+t^{1,0}_{зд.p}.$$
(1) (2)

Key: 1. i; 2. del, p

The duration of the input pulses of positive polarity:

$$\tau_{и}>2t^{0,1}_{зд.p}+t^{1,0}_{зд.p}.$$

If the signal is picked up from the output of the elements D_3, the minimum operating cycle of a single trigger and the minimum durations of the input pulses are:

$$t_{и}=3t^{0,1}_{зд.p}+3t^{1,0}_{зд.p};$$
$$\tau_{и}>2t^{0,1}_{зд.p}+t^{1,0}_{зд.p};$$
$$\tau_{и}>2t^{1,0}_{зд.p}+t^{0,1}_{зд.p}.$$

The circuits executed from JK and D-triggers of the K131, K155 and K158 series are set to the "0" state by a negative pulse fed to the input $\overline{R}$. The code is entered in two cycles: first setting to "0," then entering "1" in the corresponding bit.

When executing circuits from a K155TV1 microcircuit and using preliminary setting and clearing it is necessary to feed the logical "0" voltage level to the synchronization input.

Code Converters. The functional diagram of the 2421 code to 7-position code converter constructed from logical AND-NOT elements is presented in Figure 5-153.

The speed of the circuit is determined by the delay of the two AND-NOT logical elements.

The conversion of the 8421 code to binary-decimal code is used for data input and processing and to control the display elements. The functional diagram of the

8421 code to 7-position binary-decimal code converter constructed from AND-NOT logical elements is presented in Figure 5-154. The speed of the circuit is determined by the delay of the four logical AND-NOT elements.

The functional diagram of the 8421 code to 2421 code converter constructed from the AND-NOT logical element is illustrated in Figure 5-155.

The speed of the 8421 code to 2421 code converter is determined by the delay of the three AND-NOT logical elements.

The functional diagram of the 2421 code to the 8421 code converter constructed from the AND-NOT logical element is presented in Figure 5-156.

The speed of the 2421 code to 8421 code converter is determined by the total delay of the two AND-NOT logical elements.

The functional diagram of the Johnson code to 8421 code converter constructed on the basis of the AND-NOT logical element is presented in Figure 5-157.

The functional diagram of the decimal-to-8421 binary-decimal code converter constructed from AND-NOT logical elements is presented in Figure 5-158.

The functional diagram of the 8421 code to decimal code converter constructed from AND-NOT logical elements is presented in Figure 5-159.

The functional diagram of the Grey code to 8421 code converter constructed from AND-NOT, AND-OR-NOT logical elements is presented in Figure 5-160.

The functional diagram of the decimal code to Johnson code converter constructed from AND-NOT logical elements is presented in Figure 5-161.

The functional diagram of the Johnson code to decimal code converter constructed from AND-NOT logical elements is presented in Figure 5-162.

The functional diagram of the four-bit Grey code to binary four-bit code using the K155IM1 microcircuit is presented in Figure 5-163.

It is possible to execute the series-parallel converters from the K155IR1 type IC (Figure 5-164). The positive start pulse at the input A and the input cycle at the input C_2 set the register to the 0000000 state. Then in the shift cycle (input C_1) the information is entered in 7-bit words. The information in the form of a "1" which was first entered in the first bit of the register is shifted to the end of the register in this case. After the set of cycle pulse the "operating mode" input (V_2 input) of the register is switched through the K155LR1 microcircuit (OR cell), after which the output triggers can again be initialized to 0000000.

As a result of the possibility of parallel input, the K155IR1 type shift register can be used as a parallel-series converter. Figure 5-165 shows a converter for 7-bit words. If the register is first filled, then it is necessary to feed logical zero voltage to the input A ("start") of the converter to set the K155IR1 microcircuit to parallel input.

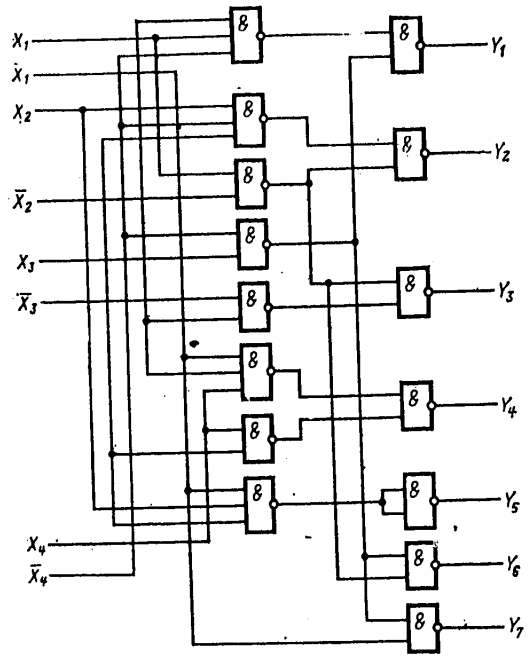


Figure 5-153. 2421 code to 7-position binary-decimal code converter

(1) Десятичная цифра	(2) Код 2421				(3) Семипозиционный двоично-десятичный код						
	x_4	x_3	x_2	x_1	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	1	1	1	0	0	1	1
2	0	0	1	0	0	1	0	0	1	0	0
3	0	0	1	1	0	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0	0	1	1
5	1	0	1	1	0	0	0	1	0	0	1
6	1	1	0	0	0	0	0	1	0	0	0
7	1	1	0	1	0	1	1	0	0	1	1
8	1	1	1	0	0	0	0	0	0	0	0
9	1	1	1	1	0	0	0	0	0	0	1

Key:
1. Decimal number
2. 2421 code
3. 7-position binary-decimal code

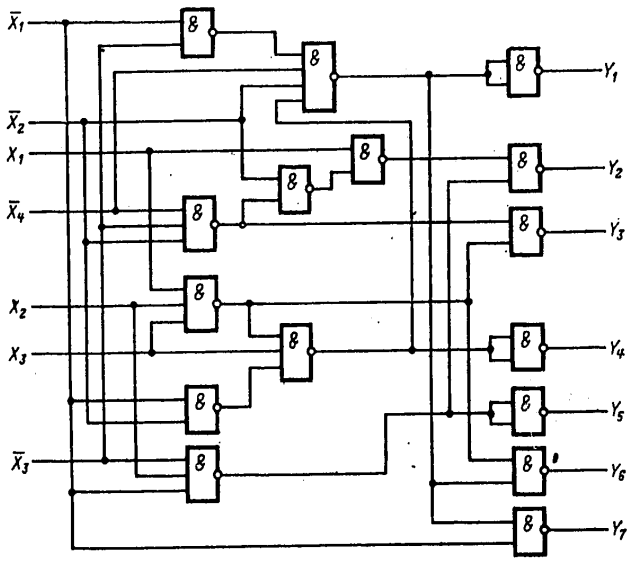


Figure 5-154. 8421 code to 7-position binary-decimal code converter

(1) Десятичная цифра	(2) Код 8421				(3) Семипозиционный двоично-десятичный код						
	x_4	x_3	x_2	x_1	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	0	0	0	0	1	0	0	0	0
1	0	0	0	1	1	1	1	0	0	1	1
2	0	0	1	0	0	1	0	0	1	0	0
3	0	0	1	1	0	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0	0	1	1
5	0	1	0	1	0	0	0	1	0	0	1
6	0	1	1	0	0	0	0	1	0	0	0
7	0	1	1	1	0	1	1	0	0	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	0	0	1

Key:
1. Decimal number
2. 8421 code
3. 7-position binary-decimal code

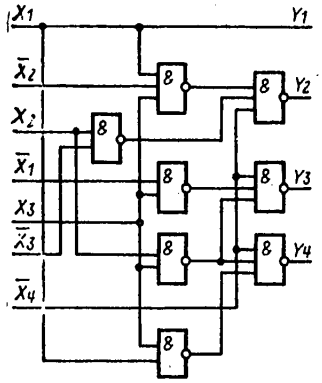


Figure 5-155. 8421 code to 2421 code converter

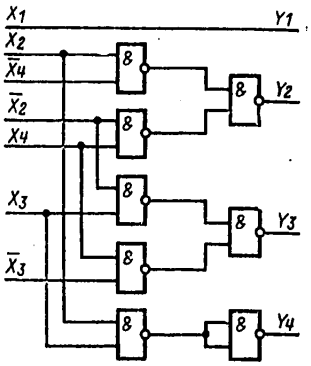


Figure 5-156. 2421 code to 8421 code converter

(1) Десятичная цифра	(2) Код 8421				(3) Код 2421			
	x_4	x_3	x_2	x_1	y_4	y_3	y_2	y_1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	1	0	0
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1

Key:
1. Decimal number
2. 8421 code
3. 2421 code

(1) Десятичная цифра	(2) Код 2421				(3) Код 8421			
	x_4	x_3	x_2	x_1	y_4	y_3	y_2	y_1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	1	0	1	1	0	1	0	1
6	1	1	0	0	0	1	1	0
7	1	1	0	1	0	1	1	1
8	1	1	1	0	1	0	0	0
9	1	1	1	1	1	0	0	1

Key:
1. Decimal number
2. 2421 code
3. 8421 code

Here the logical zero level is entered simultaneously in the first bit of the register. Then it is possible to produce a series shift of the information in which the freed bits of the register are filled with logical one, the K155LA2 microcircuit responds which switches the register from the "shift" mode to the "input" mode, as a result of which the register can take new information on the next cycle pulse.

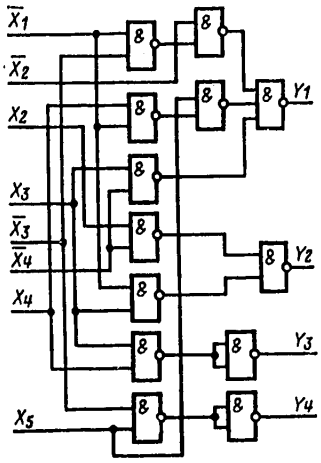


Figure 5-157. Johnson code to 8421 code converter

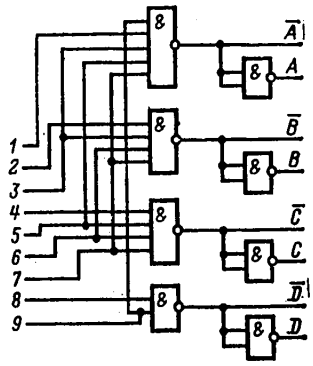


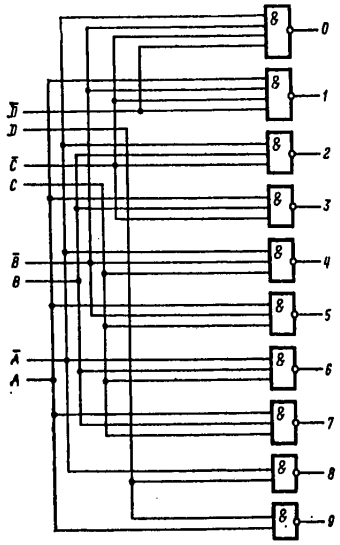
Figure 5-158. Decimal code to binary-decimal 8421 code converter

(1) Десятичная цифра	(2) Код Джонсона					(3) Код 8421			
	x_5	x_4	x_3	x_2	x_1	y_4	y_3	y_2	y_1
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	1
2	0	0	0	1	1	0	0	1	0
3	0	0	1	1	1	0	0	1	1
4	0	1	1	1	1	0	1	0	0
5	1	1	1	1	1	0	1	0	1
6	1	1	1	1	0	0	1	1	0
7	1	1	1	0	0	0	1	1	1
8	1	1	0	0	0	1	0	0	0
9	1	0	0	0	0	1	0	0	1

Key:
1. Decimal number
2. Johnson code
3. 8421 code

(1) Код десятичный	$\overline{D}$	$\overline{C}$	$\overline{B}$	$\overline{A}$
	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Key:
1. Decimal code



(1)

Код десятичный	D	C	B	A
	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Figure 5-159. 8421 code-to-decimal code converter

Key:
1. Decimal code

Counters. The functional diagram of a four-bit counter (Figure 5-166) is constructed on the basis of a memory element with four stable states and RS-trigger. The initial state is set by feeding a logical one signal to the bus R at T=0. The functioning of the four-bit counter is explained by the truth table presented in the figure.

The duration of the count pulse of the initializing signal and the interval between count pulses must not be less than $2t_{del,p,mean}$.

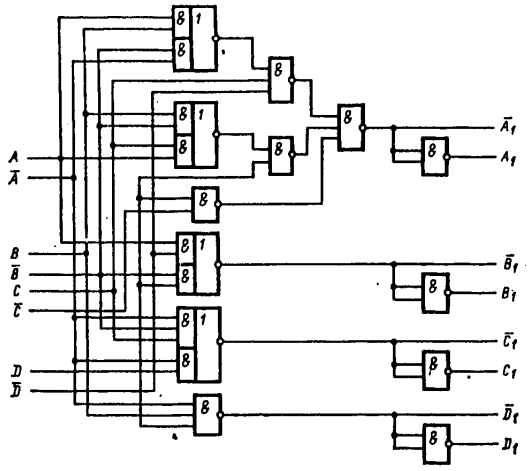
The functional diagram of a four-bit counter with Grey code is depicted in Figure 5-167.

The variation of the output signals of the counter takes place by the count pulse (T=1). It is necessary to initialize by feeding the logical zero signal to the bus R ("set 0").

The duration of the count pulses, the intervals between count pulses and initialization must not be less than $2t_{del,p,mean}$. The operation of the counter is described by the truth table (Figure 5-167).

The functional diagram of an 8-bit counter with Johnson code constructed on the basis of the AND-OR-NOT PC is presented in Figure 5-168.

The functional diagram of an n-bit counter with Grey code converter based on half-adders constructed from K155TM2 and K155LP5 microcircuits is presented in Figure 5-169.



D	C	B	A
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0

$\overline{D}_1$	$\overline{C}_1$	$\overline{B}_1$	$\overline{A}_1$
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Figure 5-160. Grey code to 8421 binary-decimal code converter

The functional diagram for the connection of the K155IYe6 and K155IYe7 microcircuits with an increase in word length of the counters is presented in Fig 5-170. If the counter circuit is used as a frequency divider without parallel entering of the information, the inputs D_1, D_2, D_4 and D_8 must be "grounded," and a logical one voltage fed to the input C.

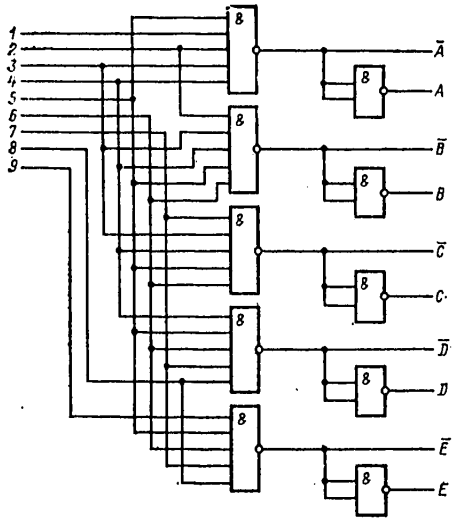
The functional diagrams of asynchronous summing counters based on JK and D-triggers and their operating time diagram are presented in Figures 5-171 to 5-174. If the counting inputs of the triggers after subsequent bits are connected to the outputs of the Q preceding bits for the counters based on JK-triggers and with output Q for the counters based on D-triggers, subtracting counters are obtained.

If the counter state is read after each input pulse, the maximum count frequency for the series counter is determined by the smallest number of the values of $t_{count,\ max}$ in accordance with the expressions:

$$f_{count,\ max} = F_{count,\ max};$$

$$f_{count,\ max} = \frac{1}{(n-1)t_{del,p}+t_{resp}},$$

where $F_{count,\ max}$ is the maximum count frequency of the trigger; n is the number of bits of the counter; $t_{del,\ p}$ is the propagation delay time on connection for counters based on JK-triggers and disconnection for counters based on D-triggers; t_{resp} is the response time of the external read circuit.



	$\bar{E}$	$\bar{D}$	$\bar{C}$	$\bar{B}$	$\bar{A}$
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	1
3	0	0	1	1	1
4	0	1	1	1	1
5	1	1	1	1	1
6	1	1	1	1	0
7	1	1	1	0	0
8	1	1	0	0	0
9	1	0	0	0	0

Figure 5-161. Decimal code to Johnson code converter

As a result of nonsimultaneous switching of the triggers of the counter with series carry on interrogation of its states false signals appear at the decoder output; therefore a gating signal must be fed to the decoder input.

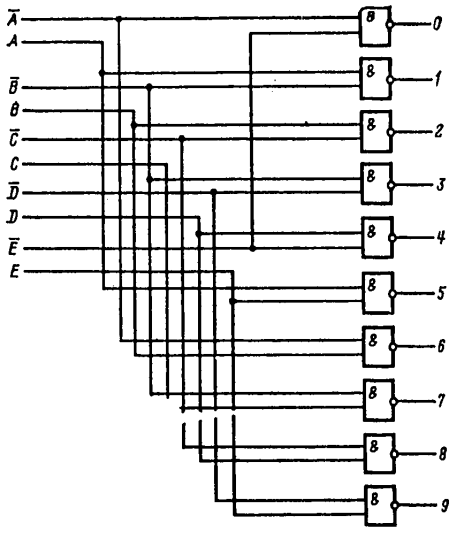
The construction of an asynchronous counter based on JK-triggers is unreasonable in a number of cases, for the counters based on JK-triggers by comparison with the counters based on D-triggers have large equipment losses and slow speed.

In order to vary the count factor of asynchronous counters it is possible to use the inputs of the $\overline{R}$ and $\overline{S}$ triggers. The functional diagram and the operating time diagram of a mod 10 asynchronous counter are presented in Figures 5-175 and 5-176.

In the general case in order to obtain a mod K counter signals are fed to the IC input from the Q-bit outputs in the logical one state on the count K-1. The output D_5 is connected to the input $\overline{S}$ of the remaining bits.

The functional diagram and the operating time diagram of an asynchronous mod 20 counter are presented in Figures 5-177, 5-178. The trigger based on the microcircuits D_6, D_8 is introduced to increase the negative pulse duration of the input of the $\overline{R}$-triggers.

In order to obtain a mod K counter, the outputs Q of the bits in the logical one state on the count K are connected to the inputs of the microcircuit D_7, and a signal is fed to the input $\overline{R}$ of these bits from the output of the microcircuit D_6.



	E	D	C	B	A
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	1
3	0	0	1	1	1
4	0	1	1	1	1
5	1	1	1	1	1
6	1	1	1	1	0
7	1	1	1	0	0
8	1	1	0	0	0
9	1	0	0	0	0

Figure 5-162. Johnson code to decimal code converter

The functional diagram and operating time diagram of a mod 12 counter are presented in Figure 5-179. When the 1100 state is reached the counter halts. For a repeat count cycle it must be set to "0."

The functional diagram of a synchronous counter with natural halt on a selected number is presented in Figure 5-180. The inverse code of the number on which the counter must half is fed to the inputs of the microcircuit D_3, D_4, D_6, D_8.

Functional diagrams and operating time diagrams of asynchronous scale-of-ten counters are presented in Figures 5-181 to 5-186.

The functional diagram of an asynchronous reversible scale-of-ten counter based on K155TV1 and K158TV1 trigger microcircuits is presented in Figure 5-187.

On addition, a logical zero voltage is fed to the "addition" +1 input, and a logical one voltage is fed to the "subtraction" -1 input. On subtraction the logical levels on the "addition" and "subtraction" inputs are switched to the opposite. On variation of the count voltage, a logical zero voltage must be fed to the controlling input V, and during operation, a logical one voltage.

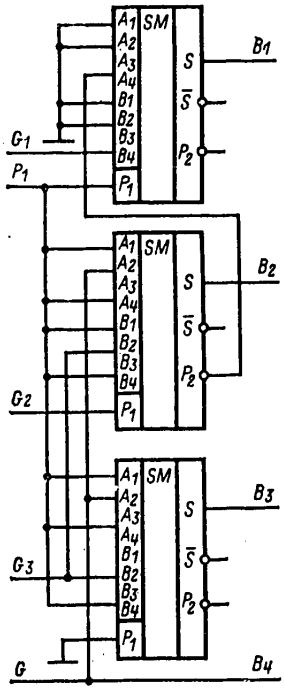


Figure 5-163. Grey code to binary code converter

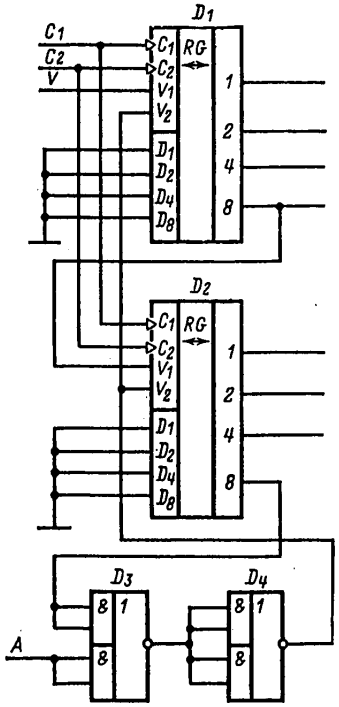


Figure 5-164. Series-parallel converter

In devices where high speed is required, it is recommended that synchronous counters with parallel carry be used.

For the construction of such counters it is recommended that JK-triggers be used. In connection with the limited number of inputs J and K of the JK-triggers the counters with parallel carry without additional logic can contain only four bits. Therefore with a large number of bits the counter is divided into groups of four bits each.

The functional diagram of one such group with group carry element is presented in Figure 5-188; the operating time diagram is presented in Figure 5-189.

The maximum count frequency of one group of bits without removal of information is determined by the maximum count frequency of an individual JK-trigger.

The functional diagram of a summing group counter constructed from identical groups is presented in Figure 5-190. A characteristic feature of the structure of the counter is the use of parallel carry from the first group to the rest and ripple-through carry between the high-order bits, beginning with the second.

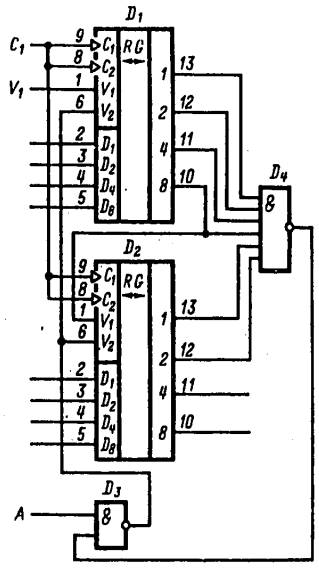


Figure 5-165. Parallel-series converter.
D_1, D_2 -- K155IR1 microcircuit; D_3 -- K155LA3 microcircuit;
D_4 -- K155LA2 microcircuit

When implementing the group counter (Figure 5-190) for n>10 additional elements for the formation of parallel carry are needed which must be connected as illustrated by the dotted lines.

The functional diagram and the operating time diagram of asynchronous reversible counter with parallel carry are presented in Figures 5-191 and 5-192. The count direction is determined by the logical level of the controlling input V, the logical zero level prepares the shaping circuit of the carry from the output $\overline{Q}$ of the triggers for realization of summation, and the logical one level, from the outputs of the Q-trigger for subtraction of the incoming pulses. For exclusion of failures on reversal of the counter constructed from JK-triggers of the K131 series, the signals on the controlling input must be varied with low level at the input C. The number of bits in the reversible counter is increased by connecting four-bit groups analogous to Figure 5-190.

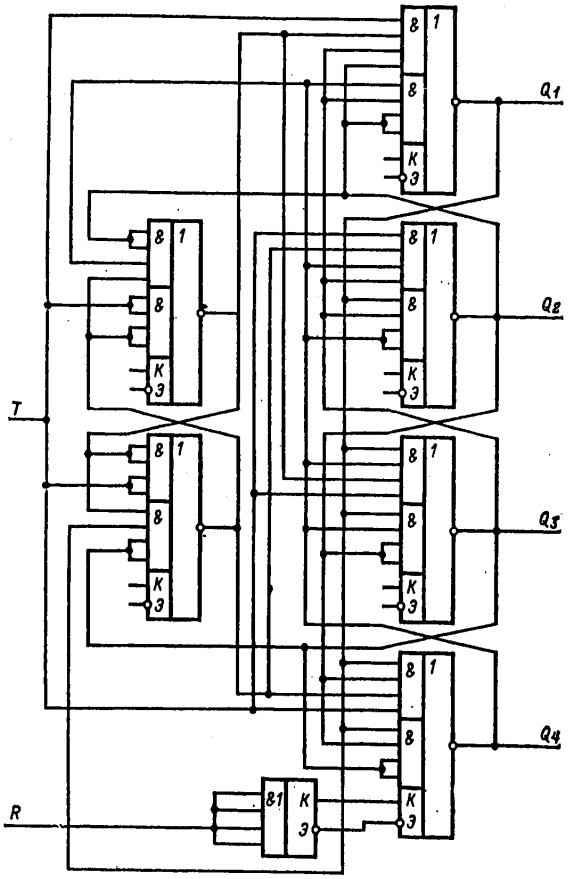


Figure 5-166. Four-bit counter with unitary coding

(1) Номер состояния счетчика	(2) Состояние выходов разрядов				(1) Номер состояния счетчика	(2) Состояние выходов разрядов			
	Q_1	Q_2	Q_3	Q_4		Q_1	Q_2	Q_3	Q_4
0	1	1	1	0	2	1	0	1	1
1	0	1	1	1	3	1	1	0	1

Key:
1. Counter state number
2. Bit output state

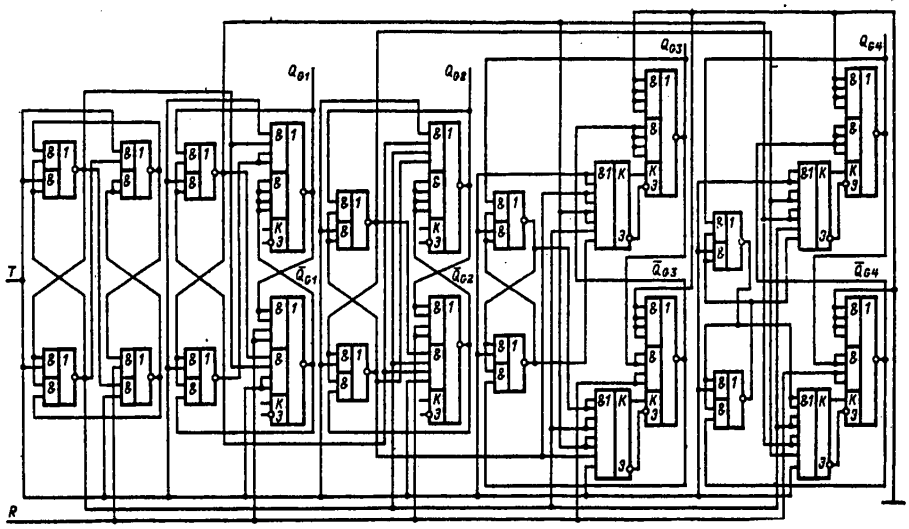


Figure 5-167. Four-bit counter with Grey code

(1) Номер состояния счетчика	(2) Состояние выходов разрядов			
	Q_{G1}	Q_{G2}	Q_{G3}	Q_{G4}
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	0	1	0	0
4	0	1	1	0
5	1	1	1	0
6	1	0	1	0
7	0	0	1	0
8	0	0	1	1
9	1	0	1	1
10	1	1	1	1
11	0	1	1	1
12	0	1	0	1
13	1	1	0	1
14	1	0	0	1
15	0	0	0	1

Key:
1. Counter state number
2. Bit output state

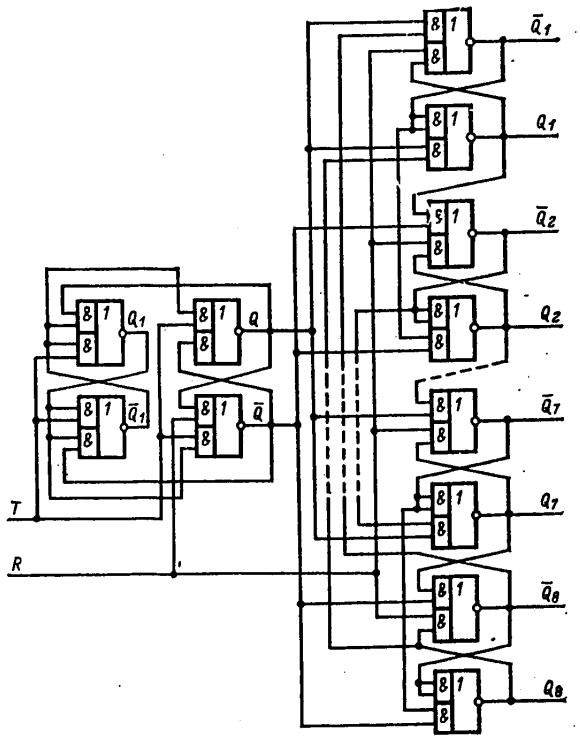


Figure 5-168. Eight-bit counter with Johnson code

(1)

Номер состояния счетчика	(2) Состояния выходов разрядов								Номер состояния счетчика	(2) Состояния выходов разрядов							
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8		Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
0	0	0	0	0	0	0	0	0	9	0	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	10	0	0	1	1	1	1	1	1
2	1	1	0	0	0	0	0	0	11	0	0	0	1	1	1	1	1
3	1	1	1	0	0	0	0	0	12	0	0	0	0	1	1	1	1
4	1	1	1	1	0	0	0	0	13	0	0	0	0	0	1	1	1
5	1	1	1	1	1	0	0	0	14	0	0	0	0	0	0	1	1
6	1	1	1	1	1	1	0	0	15	0	0	0	0	0	0	0	1
7	1	1	1	1	1	1	1	0	16	0	0	0	0	0	0	0	0
8	1	1	1	1	1	1	1	1									

Key:
1. Counter state number
2. Bit output state

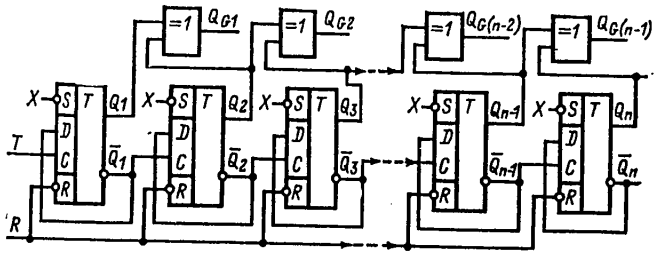


Figure 5-169. n-bit counter with Grey code converter based on halfadders

(1)

Номер состояния счетчика	(2) Состояния выходов разрядов							
	Q_{G1}	Q_{G2}	...	Q_{Gk}	Q_{Gk+1}	...	$Q_{G(n-1)}$	Q_{Gn}
0	0	0	...	0	0	...	0	0
1	1	0	...	0	0	...	0	0
2	1	1	...	0	0	...	0	0
3	0	1	...	0	0	...	0	0
...	...	...	...	...	...	...	...	...
2^k-2	1	0	...	1	0	...	0	0
2^k-1	0	0	...	1	1	...	0	0
2^k	0	0	...	1	1	...	0	0
...	...	...	...	...	...	...	...	...
$2^{n-1}-2$	1	0	...	0	0	...	1	0
$2^{n-1}-1$	0	0	...	0	0	...	1	0
2^{n-1}	0	0	...	0	0	...	1	1
...	...	...	...	...	...	...	...	...
2^n-2	1	0	...	0	0	...	0	1
2^n-1	0	0	...	0	0	...	0	1

Key:
1. Counter state number
2. Bit output states

The inputs X are connected to a 2.4-4.5 volt dc power supply.

$$\begin{cases} Q_{Gk} = Q_k + Q_{k+1}; \\ Q_{Gn} = Q_n; \end{cases}$$
$$k = 1, 2, \ldots, n-1.$$

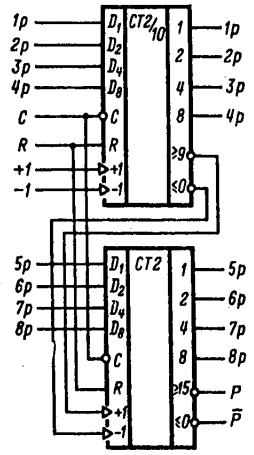


Figure 5-170. Connection of counters with an increase in word length

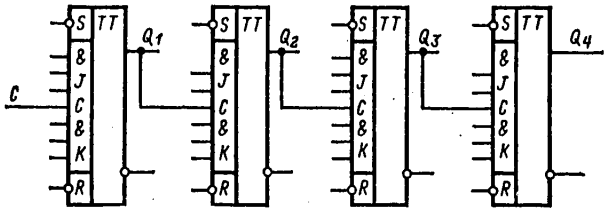


Figure 5-171. Functional diagram of an asynchronous binary counter

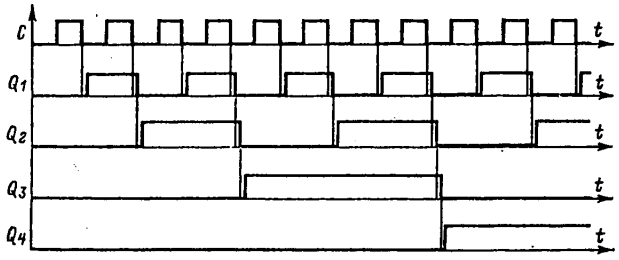


Figure 5-172. Operating time diagram of anasynchronous binary counter

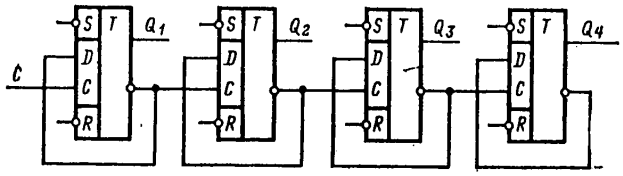


Figure 5-173. Functional diagram of an asynchronous binary counter

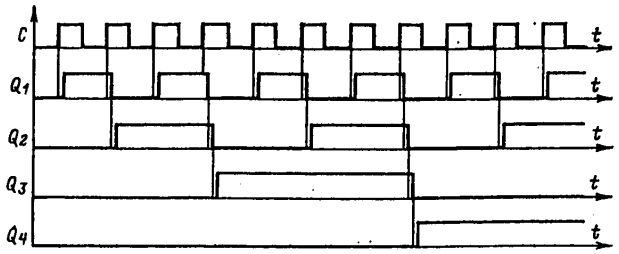


Figure 5-174. Operating time diagram of an asynchronous binary counter

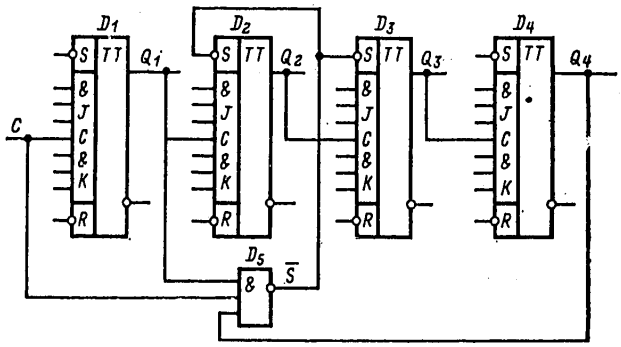


Figure 5-175. Functional diagram of an asynchronous mod 10 counter

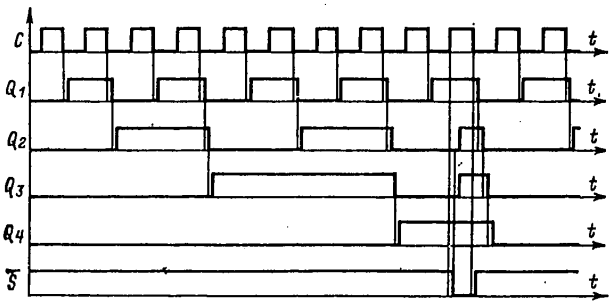


Figure 5-176. Operating time diagram of a mod 10 asynchronous counter

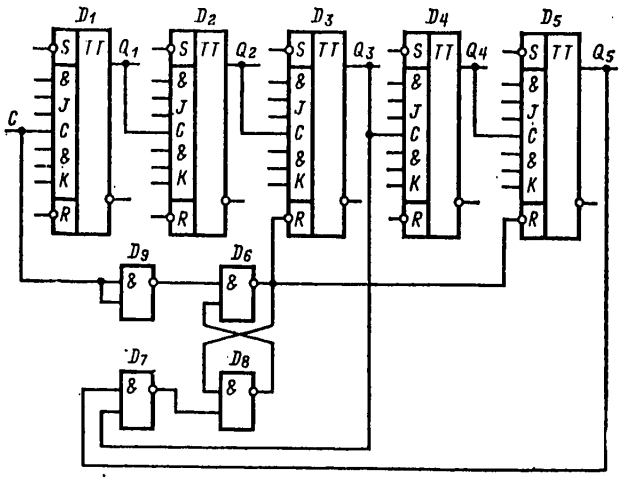


Figure 5-177. Functional diagram of a mod 20 asynchronous counter

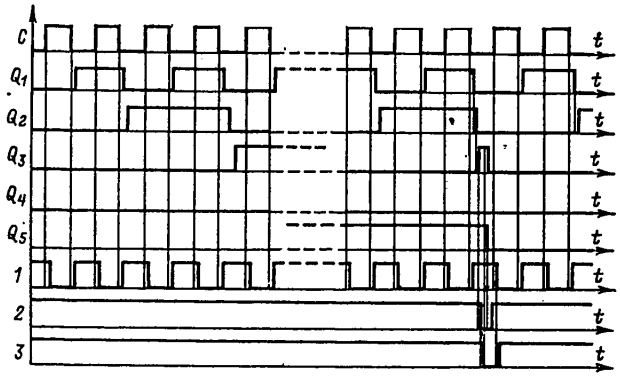


Figure 5-178. Operating time diagram of an asynchronous mod 20 counter

If the reversible control circuit is executed in the form of an RS-trigger, the functional possibilities of the reversible counter are expanded. In this case the circuit will have a number of advantages:

Switching from addition to subtraction and back can be accomplished by short pulses;

In addition to the addition and subtraction operations, it will be possible to perform the inversion operation on code entered in the counter, for which it is necessary to feed low levels to both inputs of the control RS-trigger, and then the synchronization pulse to the counting input of the counter. (In this case it is necessary to consider that the low levels can be fed to the input $\overline{R}$ and $\overline{S}$ of the RS-trigger also simultaneously, and picked up only alternately.)

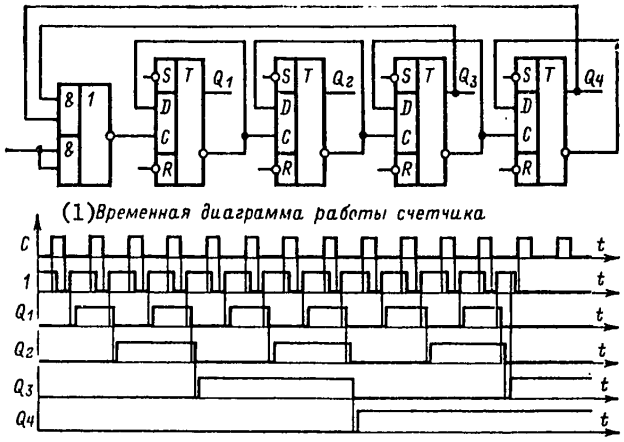


Figure 5-179. Asynchronous mod 12 counter with natural halt

Key:

1. Operating time diagram of the counter

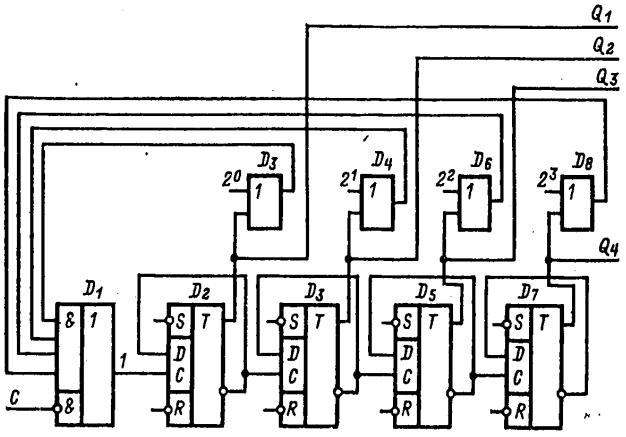


Figure 5-180. Functional diagram of an asynchronous binary counter with natural half on a selected number

The speed of multibit counters with parallel carry, including reversible counters, can be increased by introducing an additional carry trigger in the first group of bits as shown in Figure 5-193. Here the delay in the carry shaping circuit is excluded, for the carry trigger is switched synchronously with the triggers in the counter bits. The connection of the first group of bits to the subsequent ones is the same as in Figure 5-190.

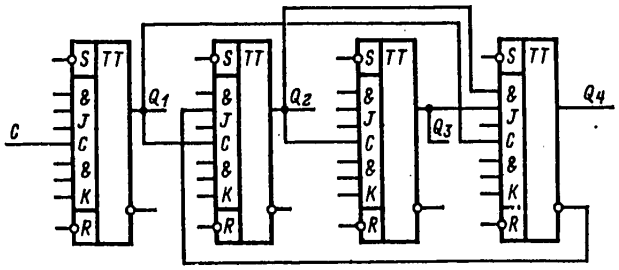


Figure 5-181. Functional diagram of an asynchronous summing scale-of-ten counter

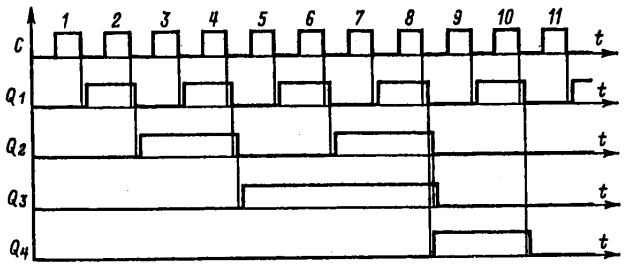


Figure 5-182. Operating time diagram of an asynchronous summing scale-of-ten counter

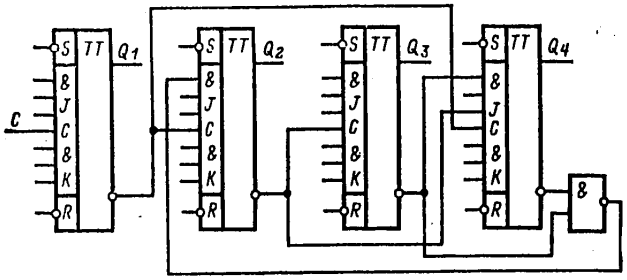


Figure 5-183. Functional diagram of an asynchronous subtracting scale-of-ten counter

The functional diagrams and operating time diagrams of synchronous counters for 3, 4, 5, 6, 7, 9, 10, 11, 12, 13 based on the JK and D-triggers of the K131, K155, K158 series microcircuits are presented in Figures 5-194 to 5-207.

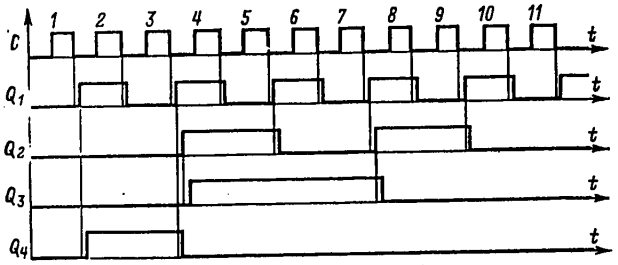


Figure 5-184. Operating time diagram of an asynchronous subracting scale-of-ten counter

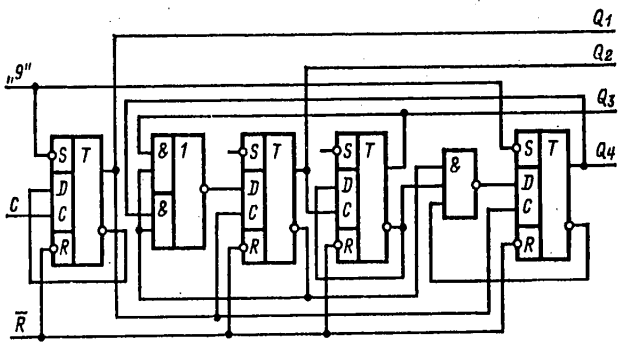


Figure 5-185. Functional diagram of an asynchronous subtracting scale-of-ten counter

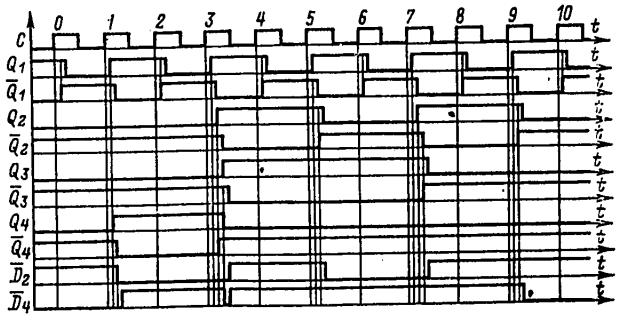


Figure 5-186. Operating time diagram of an asynchronous subtracting scale-of-ten counter

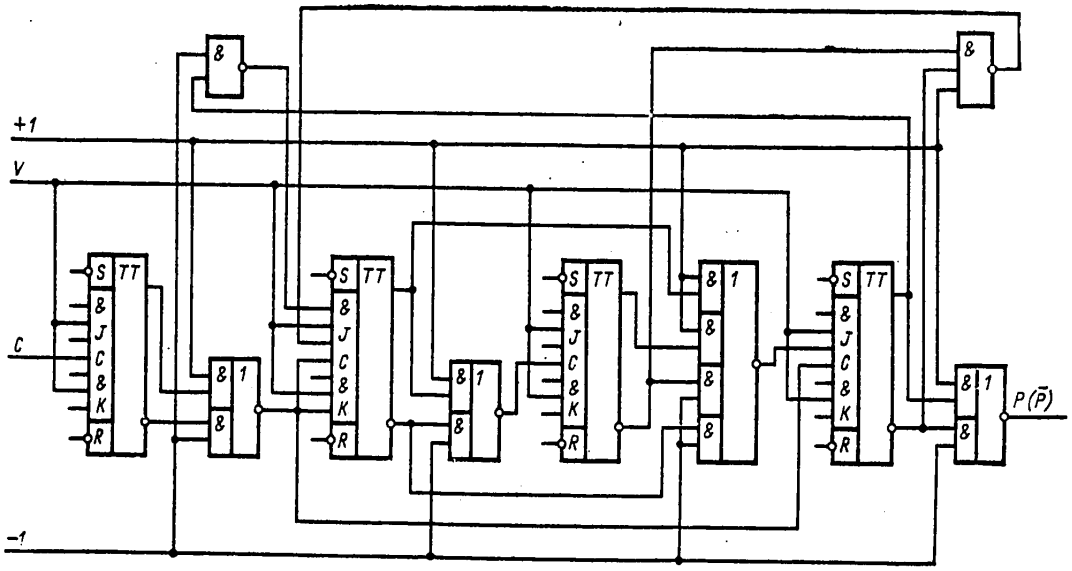


Figure 5-187. Functional diagram of an asynchronous reversible scale-of-ten counter

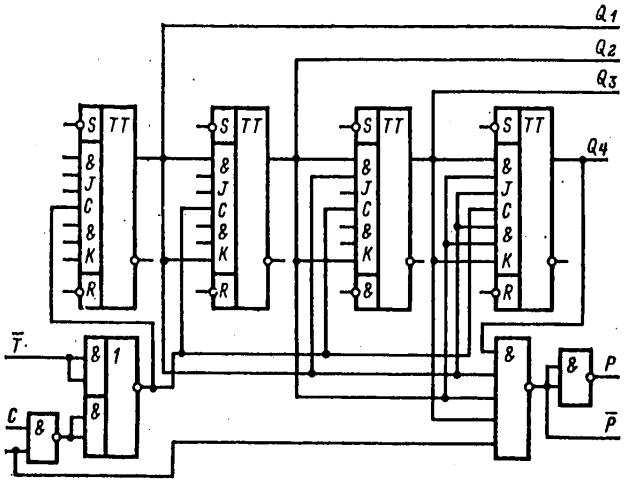


Figure 5-188. Functional diagram of synchronous binary countery with parallel carry

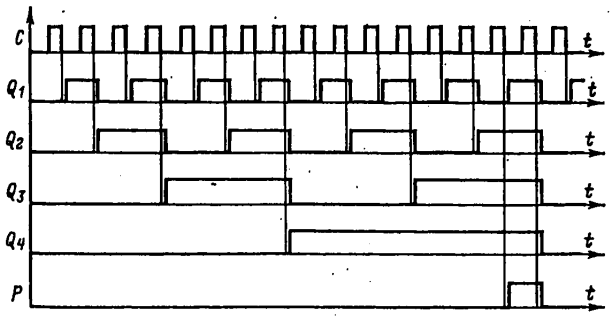


Figure 5-189. Operating time diagram of synchronous binary counter with parallel carry

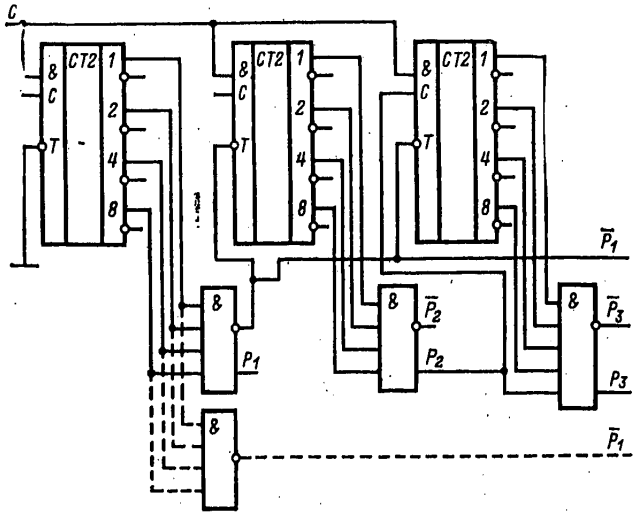


Figure 5-190. Functional diagram of a summing group counter

A distinguishing feature of synchronous counters with parallel carry is reduction of the load capacity of the trigger output as a result of their use for the organization of parallel carry.

The functional diagram and operating time diagram of a counter with parallel-series carry are presented in Figures 5-208, 5-209.

The given counter occupies an intermediate position between the counters with series and parallel carry, retaining the high load capacity of the outputs and simplicity of layout of the circuit characteristic of a counter with series carry.

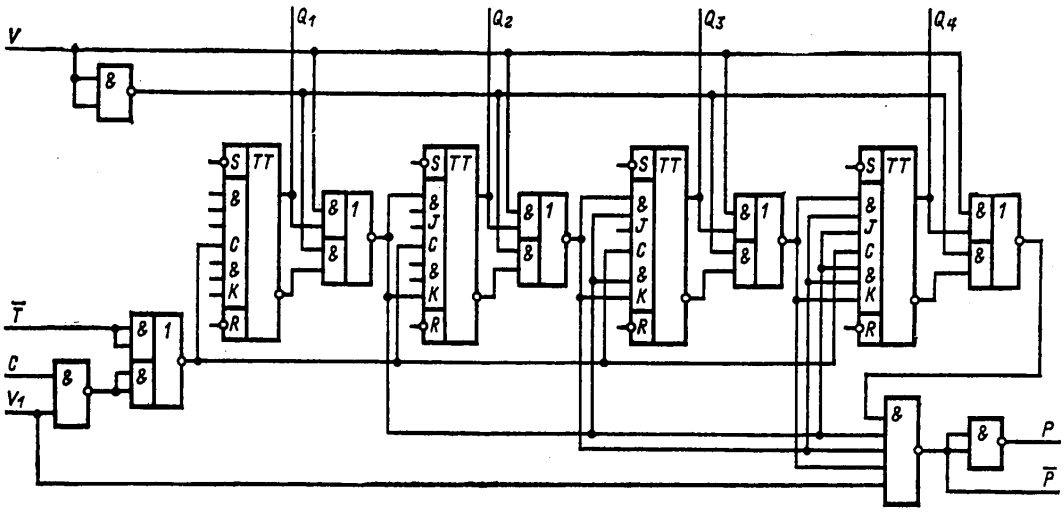


Figure 5-191. Functional diagram of a synchronous binary reversible counter with parallel carry

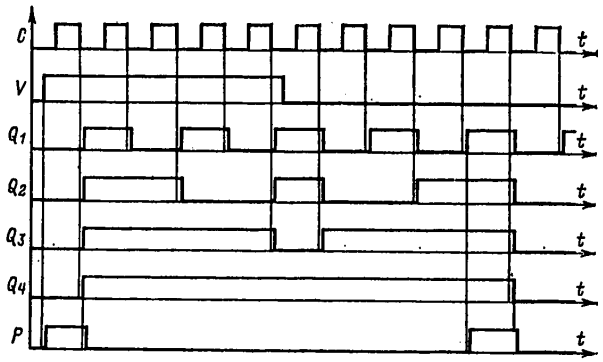


Figure 5-192. Operating time diagram of a synchronous binary reversible counter with parallel carry

The maximum counting frequency of such counters is determined by the formula $f_{count,\ max}$ presented on p 156; in the given case n is the number of series-connected groups of bits of the counter.

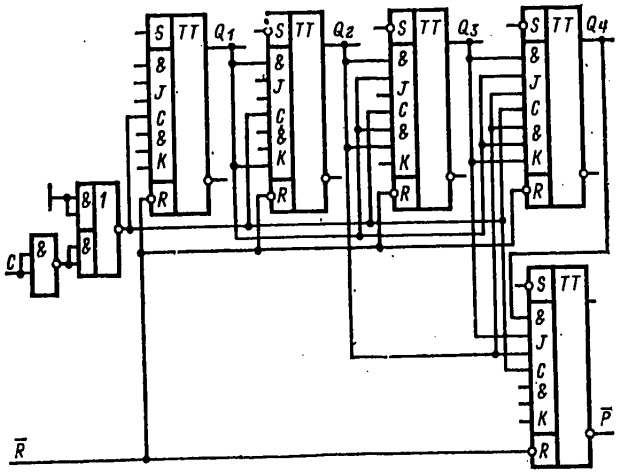


Figure 5-193. Counter with parallel carry and group parallel carry memory trigger. Electrical functional diagram.

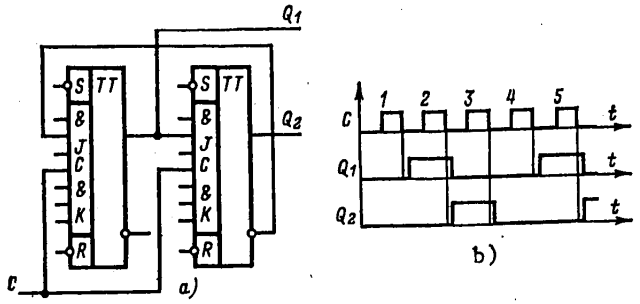


Figure 5-194. Functional diagram (a) and operating time diagram (b) of a mod 3 counter

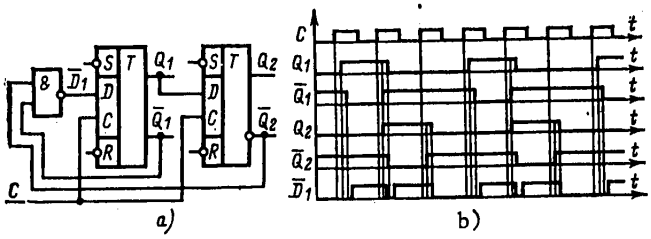


Figure 5-195. Functional diagram (a) and operating time diagram (b) of a mod 4 counter

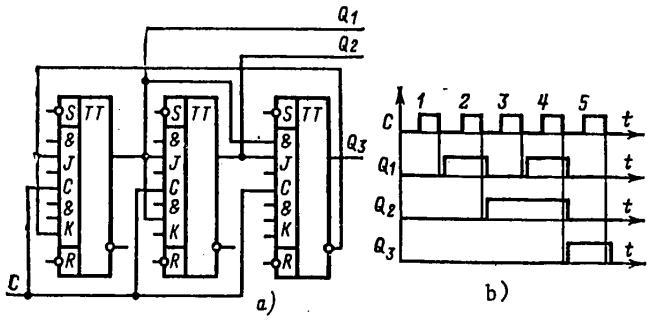


Figure 5-196. Functional diagram (a) and operating time diagram (b) of a mod 5 counter

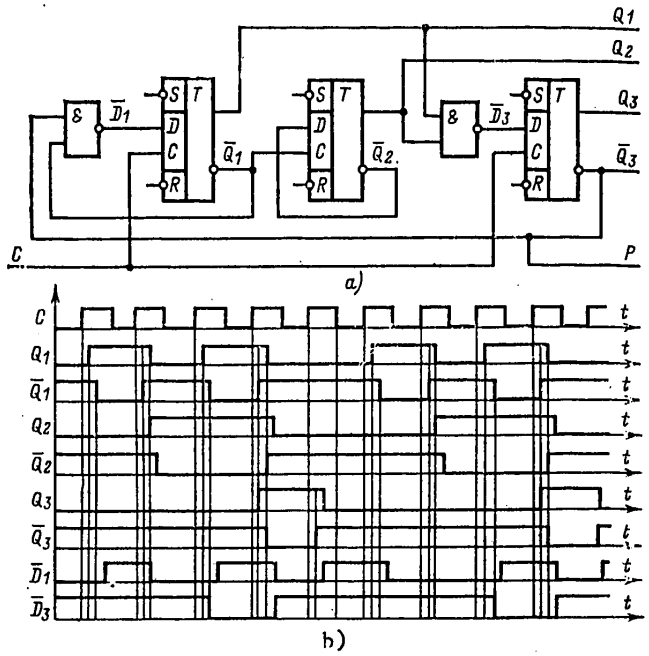


Figure 5-197. Functional diagram (a) and operating time diagram (b) of a mod 5 counter

The functional diagram of a synchronous scale-of-ten reversible counter operating in binary-decimal code with addition of the number 6 after the code 1001 is presented in Figure 5-210.

During direct counting after the 1001 code, by the next countable signal the first and fourth bits of the decade are switched to "0," and by the zero signal $\overline{P}_C$ the blocking of the second bit is realized. During reverse counting after the 0000 code by the next countable signal the first and fourth bits of the decade are switched to "1," and by the zero signal $\overline{P}_B$ the switching of the second and third bits is blocked.

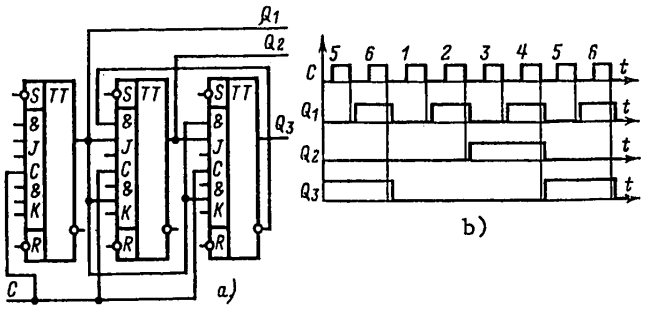


Figure 5-198. Functional diagram (a) and operating time diagram (b) of a mod 6 counter

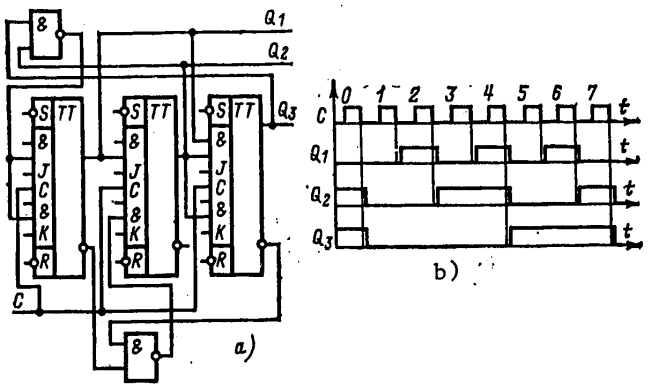


Figure 5-199. Functional diagram (a) and operating time diagram (b) of a mod 7 counter

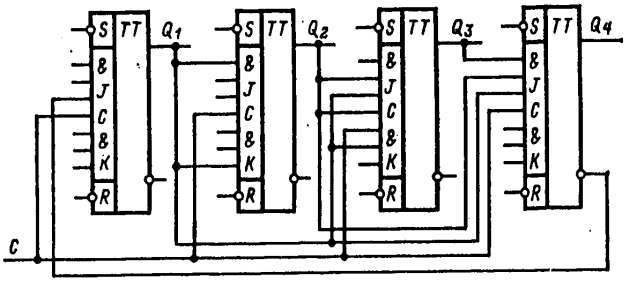


Figure 5-200. Functional diagram of a mod 9 counter

Reversing a counter constructed from JK-triggers of the K131 series is possible only at low level on the counting input.

The functional circuit diagram of four-bit groups is presented in Figure 5-211.

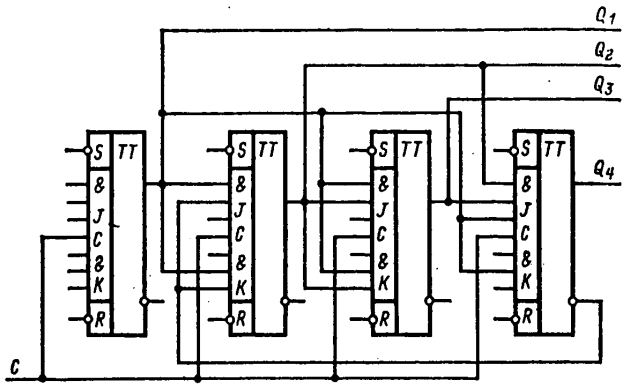


Figure 5-201. Functional diagram of a synchronous summing scale-of-ten counter

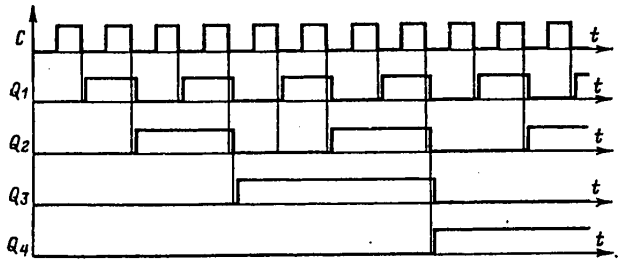


Figure 5-202. Operating time diagram of a synchronous summing scale-of-ten counter

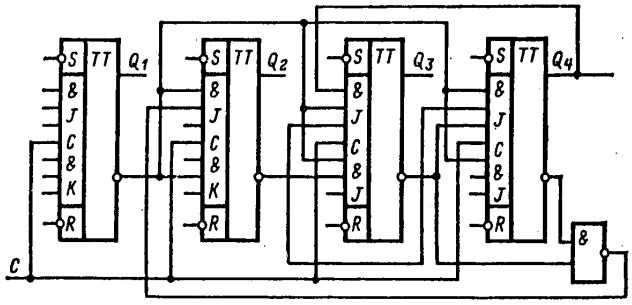


Figure 5-203. Functional diagram of a synchronous subtracting scale-of-ten counter

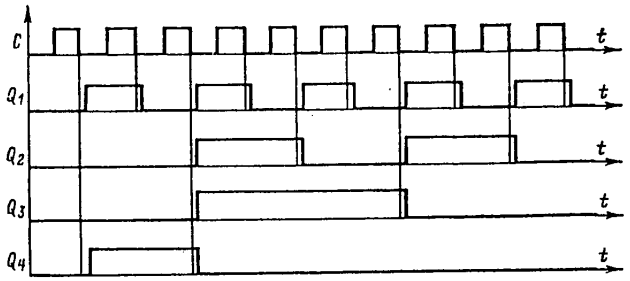


Figure 5-204. Operating time diagram of a synchronous subtracting scale-of-ten counter

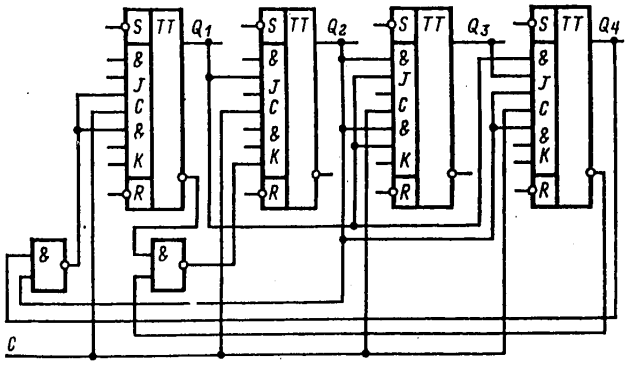


Figure 5-205. Functional diagram of a mod 11 counter

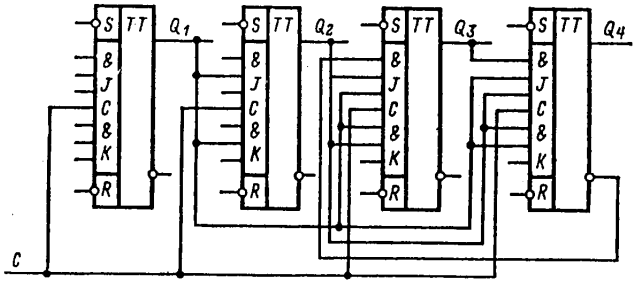


Figure 5-206. Functional diagram of a mod 12 counter

The functional diagram and operating time diagram of a synchronous scale-of-ten counter with parallel carry are presented in Figure 5-212.

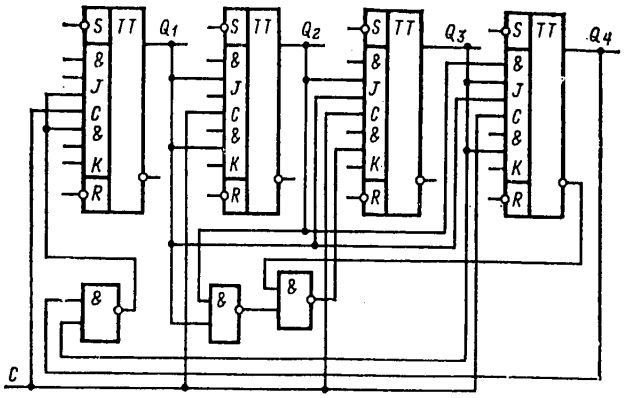


Figure 5-207. Functional diagram of a mod 13 counter

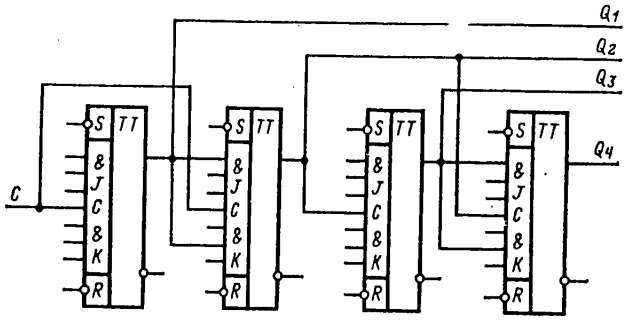


Figure 5-208. Functional diagram of a binary counter with parallel-series carry

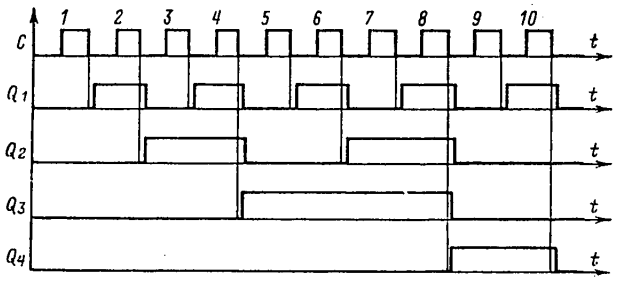


Figure 5-209. Operating time diagram of a binary counter with parallel-series carry

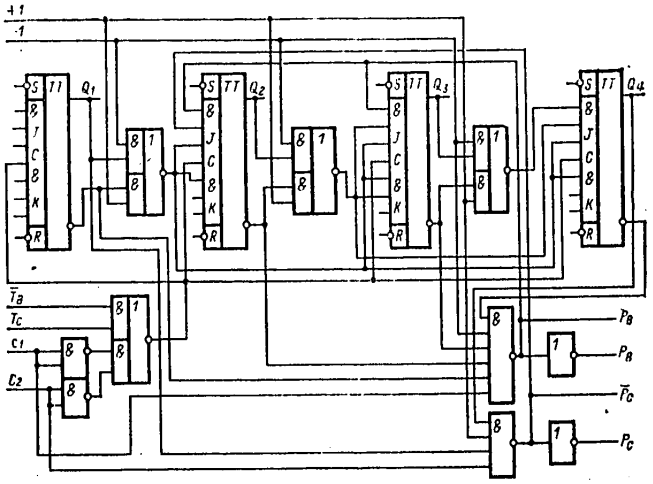


Figure 5-210. Functional diagram of a synchronous scale-of-ten reversible counter

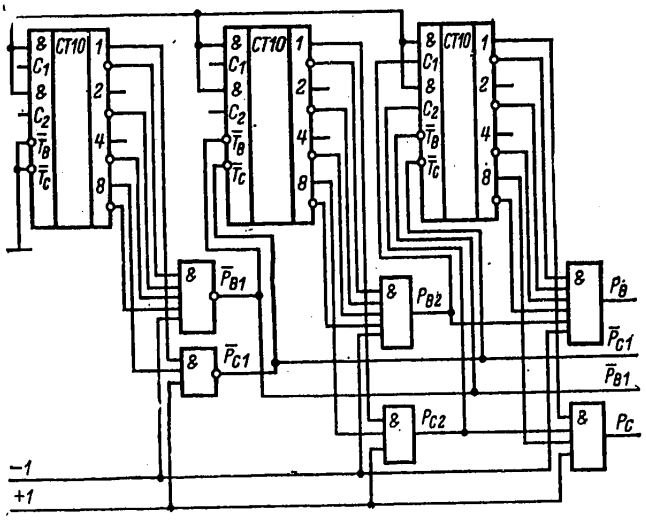


Figure 5-211. Functional diagram of a reversible group scale-of-ten counter

The functional diagram of a synchronous reversible counter with ripple-through carry is presented in Figure 5-213. On addition it is necessary to feed a logical one voltage to the "addition" input +1 and a logical zero voltage to the "subtraction" input -1. On subtraction the logical levels are switched to the opposite.

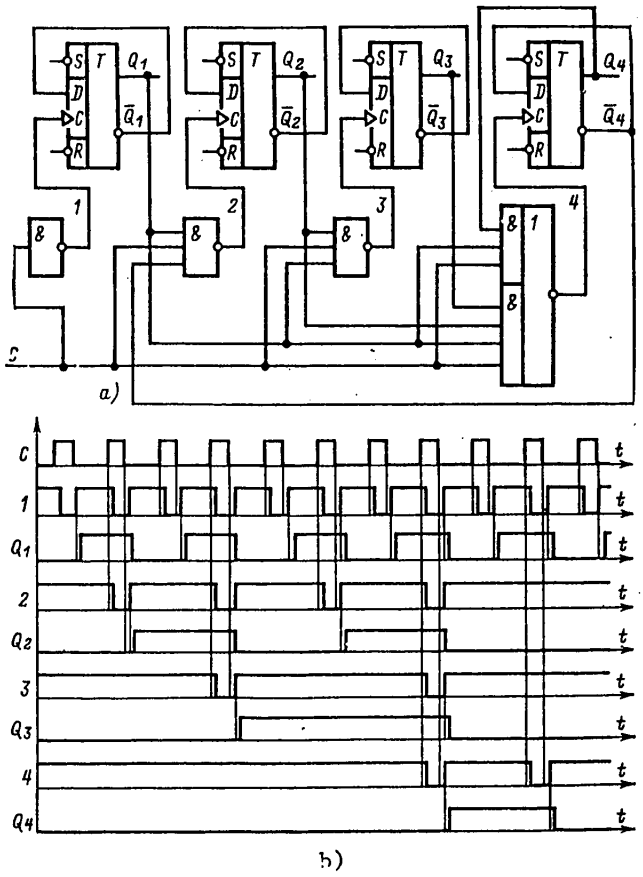


Figure 5-212. Functional diagram (a) and operating time diagram (b) of a synchronous scale-of-ten counter with parallel carry

The counter with variable counting factor performs the function of counting cycle pulses with given division factor K of the cycle pulse frequency. The functional diagram and operating time diagram of a counter with variable counting factor are presented in Figures 5-214, 5-215. For the 1111 code and high voltage level at the counting input C negative and positive output pulses are formed on the outputs Q_5 and Q_6. The positive output pulse interrogates the input elements AND-NOT, to which the control is fed in binary code. Here the signals confirming the setting to "1" reach the inputs S of the bits which have the "1" code in the controlling signal.

The counting factor is:

$$K = 16-N$$

where N is the decimal equivalent of the binary code reaching the AND-NOT input elements.

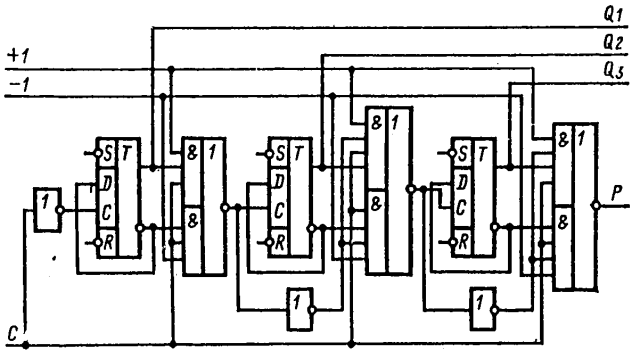


Figure 5-213. Functional diagram of a synchronous reversible counter with ripple-through carry

With an increase in the number of bits it is necessary to retain the parallel carry and increase the number of input elements AND-NOT on which the code 11...1 is assembled.

The basis for the shifting counter is a series register.

For construction of shifting counters it is recommended that registers based on D-triggers be used as the most economical.

The common characteristic of the circuits of this class is the presence of feedback from the outputs of the shift register to its series input.

The simplest shift counter is presented in Figure 5-216.

Feedback is introduced from the output Q_n of the last bit. The counter has n states, where n is the number of bits.

The operation of the counter is based on series copying of the "1" or "0" code from the low-order bit to the high-order bit, that is, the counter state is determined by the location of the "1" or "0" code.

Counters with a number of states K=n have 2^n-n unused states. Such counters require preliminary setting and periodic removal of the unused states.

The functional diagram of a counter with more complex feedback which provides for transition to the state with one one in the bits after a maximum of four input pulses is presented in Figure 5-217.

If the feedback in the shift counter is introduced from the output $\overline{Q}$ of the last bit, the number of states of the counter increases to 2n. The functional diagram of this counter is presented in Figure 5-218. For decoding the counter state it is necessary to have 2n two-input AND elements, the inputs of which are connected

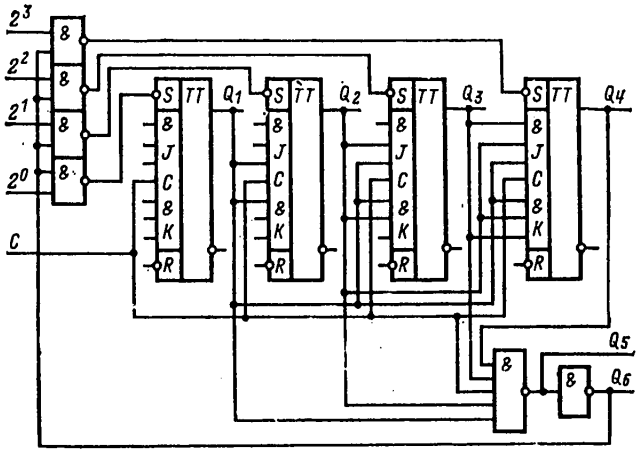


Figure 5-214. Functional diagram of the counter with variable counting factor

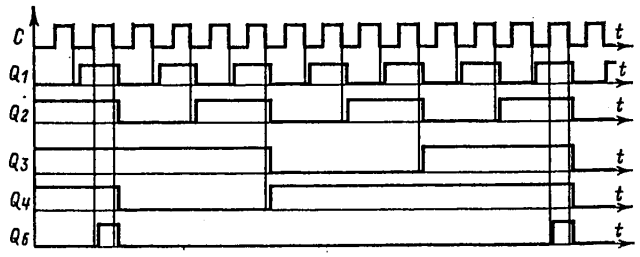


Figure 5-215. Operating time diagram of a counter with variable counting factor (K=12).

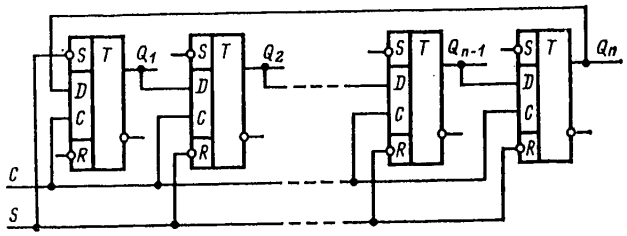


Figure 5-216. Functional diagram of a shift counter with K=n.

to the outputs Q and $\overline{Q}$ of the adjacent bits. The states of the shift counter with 2n states are presented in the table to Figure 5-220, and it is indicated which pairs of outputs must be fed to the input of the AND element. Figure 5-218 demonstrates how it is possible to realize decoding of n states of the counter, using the OR-NOT elements. The decoding of the remaining states is carried out analogously.

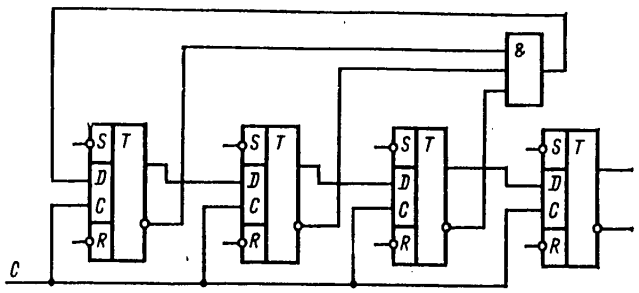


Figure 5-217. Functional diagram of a self-restoring shift counter

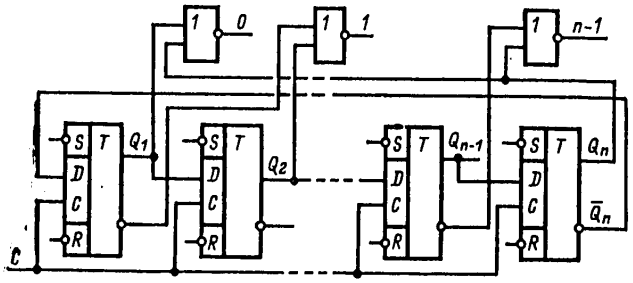


Figure 5-218. Functional diagram of a shift counter with K=2n.

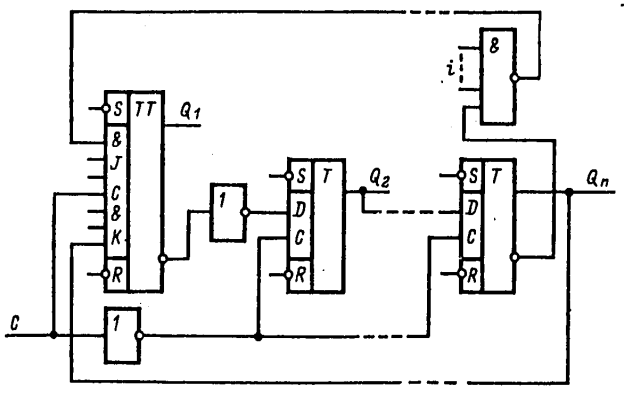


Figure 5-219. Functional diagram of a self-restoring shift counter with K=2n.

Since the shift counter with K=2n uses not all possible 2^n states, initial initialization of the counter is required.

The functional diagram of a self-restoring four-bit shift counter, the first bit of which is executed from a JK-trigger, is presented in Figure 5-219.

In the general case for the n-bit counter, it is necessary to feed the inputs $\overline{Q}$ with i last bits to the input of the AND element, where $i \geq n/3$.

The counters with K=2n can be used in the role of pulse distributors performing the function of alternate output and negative or positive pulses over separate channels.

If the states of the counter with K=2n are decoded using the OR-NOT elements (Figure 5-218), then positive pulses will appear at the output of these elements with duration equal to the period of the cycle pulses and with a frequency 2n times less. The time diagram of the pulse distributor for n=4 is presented in Fig 5-220 (0, 1, 2, 3, 4, 5, 6, 7 are the outputs of the OR-NOT elements).

If the decoding of the counter states with K=2n is realized using the element AND-NOT (using the data of the table to Figure 5-220), the negative pulse distributor is obtained. The time diagram of the negative pulse distributor for n=4 is presented in Figure 5-221. A characteristic feature of the given pulse distributor is overlapping of the lower levels at the outputs of each adjacent channel, which is caused by overlapping of the high levels at the outputs of the D-trigger.

The functional diagram of the n-bit shift counter with K=2n-1 is presented in Figure 5-222. The counter with K=2n-1 differs from the counter with K=2n only by the fact that as a result of the presence of feedback through the AND element, the state $Q_1=Q_2 \ldots Q_{n-1}$ is forbidden in the counter. The speed of the counter with K=2n-1 is lower than for the shift register as a result of a delay of the AND element.

The number of states K of the shift counters can be increased to 2^{n-1} if we use the "exclusive OR" for feedback. Such counters are simpler to design than the ordinary synchronous counters, for with a large number of bits they are more economical.

The feedback equations for shift counters having up to 12 bits are presented in the table to Figure 5-222.

Inasmuch as the "exclusive OR" 0 function is equal to "0," the state of all "0's" is a stable state; therefore preliminary setting is required. In order that the counter independently leave the zero state, the feedback equation must be equal to the logical sum of the "exclusive OR" functions and $\overline{Q}_1$, Q_2, ..., $\overline{Q}_n$.

Complementing the feedback by elements permitting the required number of states to be skipped, it is possible to obtain a shift counter with $K<2^{n-1}$. In the table to Figure 5-222, the states of the counter K are illustrated, and the values of the feedback equations F for obtaining the number of states K from 4 to 62 corresponding to them are also shown.

If the value of the feedback equation F must be equal to logical "1" (logical "0"), the "exclusive OR" function is logically added (multiplied) with the logical product (inversion of the logical product) of the state of the counter bit corresponding to the given K. For the counter with K=12 the feedback equation is:

$$Q_3 \oplus Q_4 + Q_1 Q_2 \bar{Q}_3 \bar{Q}_4 = Q_3 \oplus Q_4 + Q_1 \bar{Q}_2 \bar{Q}_3.$$

For a self-restoring counter with K=8, the feedback equation is:

$$(Q_3 \oplus Q_4)\overline{(\bar{Q}_1 Q_2 Q_3 \bar{Q}_4)} + \bar{Q}_1 \bar{Q}_2 \bar{Q}_3 \bar{Q}_4 = \bar{Q}_3 Q_4 + Q_1 Q_3 \bar{Q}_4 + \bar{Q}_1 \bar{Q}_2 \bar{Q}_4.$$

The functional diagrams of the counters with K=12 and K=8 are presented in Figures 5-223, 5-224, respectively.

The functional diagrams of pulse shapers are presented in Figure 5-225. The pulse duration is regulated by the number of NOT elements. For an odd number of NOT elements, the diagram in Figure 5-225, a is used; for an even number, Figure 5-225, b. The circuits based on JK-triggers shape the pulses by the pulse decay, the circuits based on the D-triggers, by the pulse front.

Diagrams permitting coordination of asynchronous information with the cycle pulse system are presented in Figures 5-226, 5-227.

In connection with the fact that the mutual arrangement of the signal fronts and decays reaching the inputs C and the information input can be arbitrary, the given diagrams can be executed only from K155TV1, K158TV1 microcircuits.

The diagram presented in Figure 5-227 permits a series of positive pulses to be obtained during the time that the logical one voltage is fed to the asynchronous input. The duration of the positive pulses is equal to the time interval during which a logical zero voltage is present at the input C. This circuit can be used as a "1" detector. The time diagram for this case is presented in Figure 5-227, b.

Registers. It is recommended that D-triggers be used to construct parallel type storage registers.

The functional diagram of a parallel register and the operating time diagram of the first bit for alternate entering of "1" and "0" codes are presented in Figure 5-228.

The parallel code is fed to the inputs D_1-D_n. The recording is made by positive pulse fed to the input C of the triggers. The code is picked up from the outputs Q_1-Q_n.

The shift registers perform the function of conversion of the parallel code to series code and vice versa.

From the point of view of decreasing the number of couplings and the equipment, it is more convenient to construct shift registers from D-triggers.

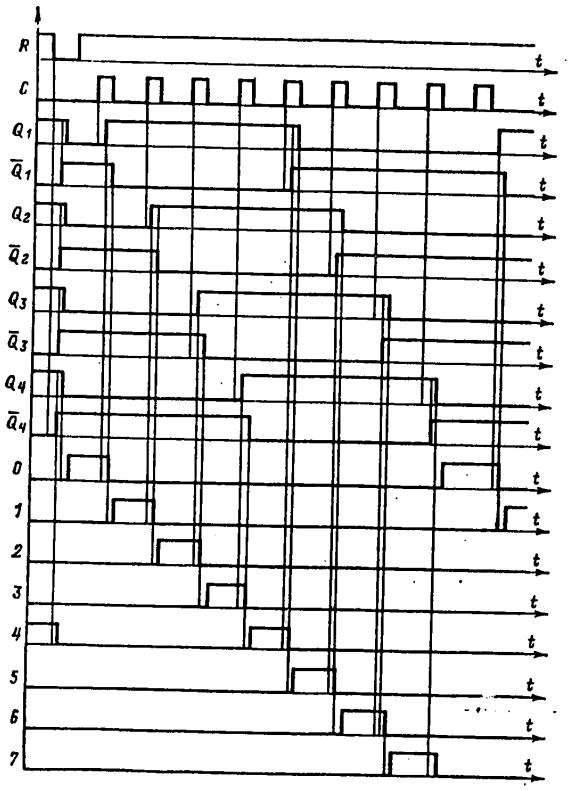


Figure 5-220. Time diagram of a positive pulse distributor

(1) Номер состояния	(2) Состояние счетчика 1	2	3	....	n−1	n	(3) Дешифратор логики (элемент И)
0	0	0	0	....	0	0	$\bar{Q}_1$ $\bar{Q}_n$
1	1	0	0	....	0	0	Q_1 $\bar{Q}_2$
2	1	1	0	....	0	0	Q_2 $\bar{Q}_3$
3	1	1	1	....	0	0	Q_3 $\bar{Q}_4$
.	.	.	.	....	.	.	. .
.	.	.	.	....	.	.	. .
.	.	.	.	....	.	.	. .
n−1	1	1	1	....	1	0	(Q_{n-1}) $\bar{Q}_n$
n	1	1	1	....	1	1	Q_1 Q_n

n

(1) Номер состояния	(2) Состояние счетчика 1	2	3	...	n−1	n	(3) Дешифратор логики (элемент И)
n+1	0	1	1	....	1	1	$\bar{Q}_1$ Q_2
n+2	0	0	1	....	1	1	Q_2 Q_3
n+3	0	0	0	....	1	1	Q_3 Q_4
.	.	.	.	....	.	.	. .
.	.	.	.	....	.	.	. .
.	.	.	.	....	.	.	. .
2n−1	0	0	0	....	0	1	$(\bar{Q}_{n-1})$ Q_n
2n	0	0	0	....	0	0	$\bar{Q}_1$ $\bar{Q}_n$

n

Key:
1. State No
2. Counter state
3. Logic decoder (AND element)

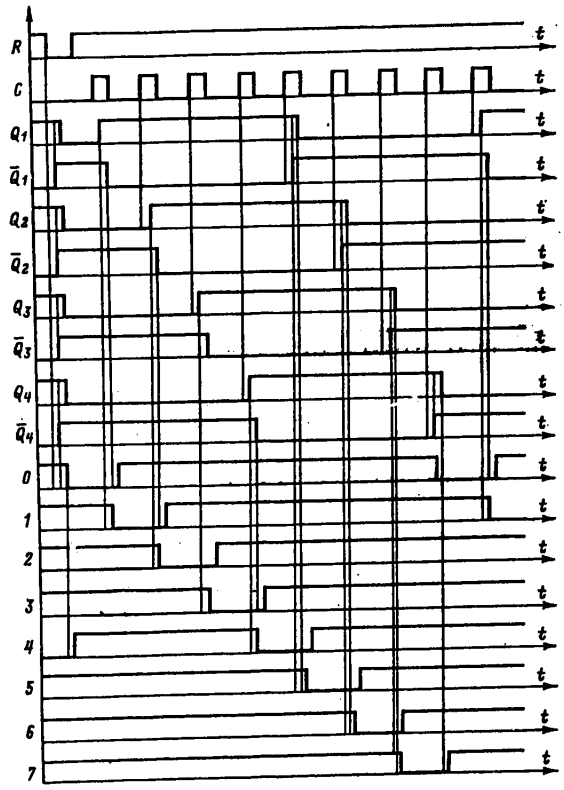


Figure 5-221. Time diagram of a negative pulse distributor

The functional diagrams of shift registers constructed from JK and D-triggers are presented in Figure 5-229, a, b. The registers are set to "0" by a negative pulse fed to the input R. The parallel code goes to the inputs S_1-S_n. The ones of the parallel code are entered by positive pulses fed to the input C_2.

The series code goes to the input D_1 of the circuit presented in Figure 5-229, a, and paraphasally to the inputs J_1 and K_1 of the circuits presented in Fig 5-229, b.

For determination of the necessary requirements on the mutual arrangement of the gradients at the inputs D_1 and C_1 (Figure 5-229, a) and J_1, K_1 and C_1 (Fig 5-229,b) it is necessary to consider the following.

The series K131, K155, K158 JK-triggers are universal triggers with paraphase information reception and with independent setting to the "0" and "1" states.

The series K131, K155, K158 JK-triggers are two-step, the information storage in which takes place using an auxiliary trigger.

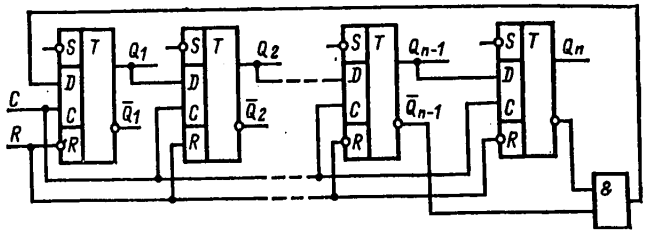


Figure 5-222. Electrical functional diagram of an n-bit shift counter

Table of feedback equations for K=2n-1

(1) Количество разряда счетчика	(2) Уравнение обратной связи	(1) Количество разряда счетчика	(2) Уравнение обратной связи
3	$Q_2 \oplus Q_3$	8	$Q_4 \oplus Q_5 \oplus Q_6 \oplus Q_8$
4	$Q_3 \oplus Q_4$	9	$Q_5 \oplus Q_9$
5	$Q_3 \oplus Q_5$	10	$Q_7 \oplus Q_{10}$
6	$Q_5 \oplus Q_6$	11	$Q_9 \oplus Q_{11}$
7	$Q_6 \oplus Q_7$	12	$Q_6 \oplus Q_8 \oplus Q_{11} \oplus Q_{12}$

Key:
1. Counter bit number
2. Feedback equation

Table of feedback equations for $K=2^{n-1}$

K	(1) Состояние счетчика		K	(1) Состояние счетчика		K	(1) Состояние счетчика	
4	110	1	25	01001	1	45	001011	1
5	001	1	26	10100	1	46	101001	0
6	011	0	27	01101	0	47	111001	1
8	0110	0	28	000010	1	48	110111	1
9	0010	1	29	11010	0	49	110001	1
10	0011	1	30	01111	0	50	001110	1
11	1100	1	32	011100	0	51	111000	1
12	0001	1	33	010011	0	52	101101	0
13	1101	1	34	000100	1	53	000010	1
14	0111	0	35	111010	1	54	100111	0
16	01011	1	36	101100	0	55	010100	0
17	10001	0	37	101111	0	56	010110	0
18	11000	0	38	101010	0	57	110000	1
19	10110	1	39	111110	1	58	000001	1
20	00111	0	40	100110	0	59	011011	0
21	10101	1	41	000101	1	60	110010	1
22	11110	1	42	111101	1	61	110101	1
23	10010	0	43	001000	1	62	011111	0
24	01100	0	44	000011	1			

Key:
1. Counter state

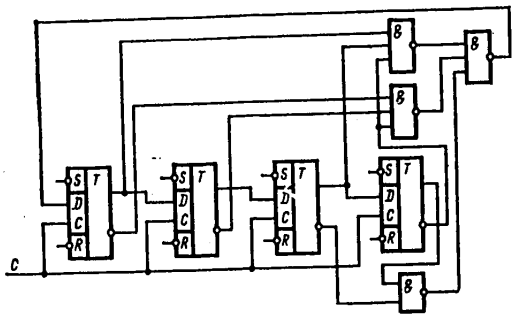


Figure 5-223. Functional diagram of a shift counter with K=12

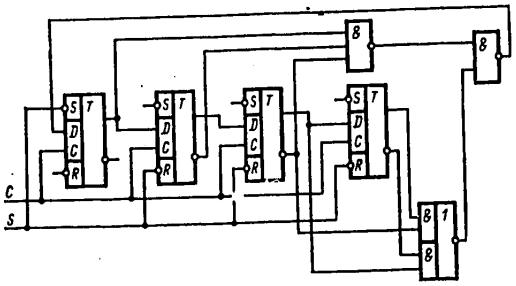


Figure 5-224. Functional diagram of a shift counter with K=8

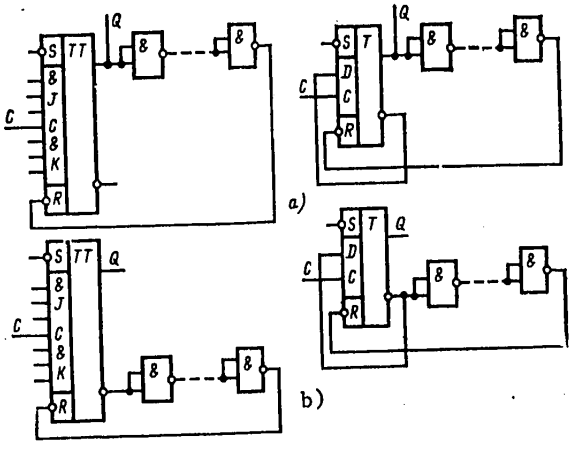


Figure 5-225. Functional diagrams of pulse shapers

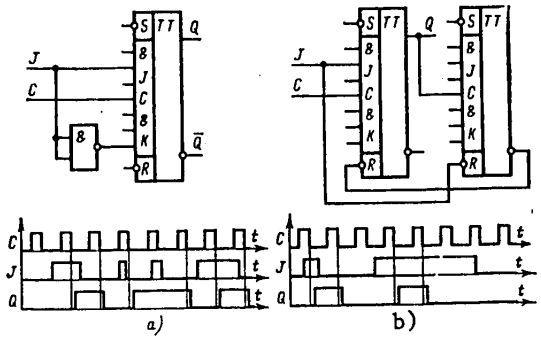


Figure 5-226. Functional diagrams (a) and operating time diagrams (b) of the asynchronous information coordination circuits

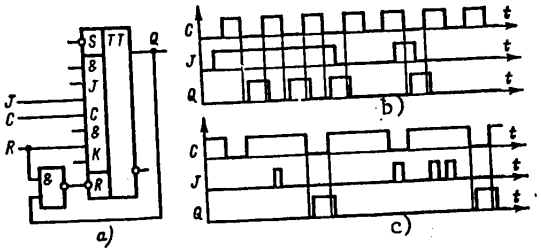


Figure 5-227. Functional diagram (a) and operating time diagrams (b, c) of a one detector

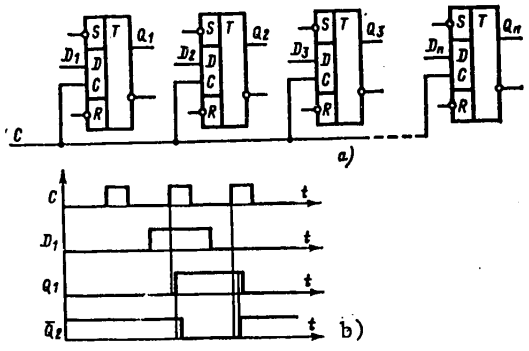


Figure 5-228. Functional diagram (a) and operating time diagrams of a parallel register (b)

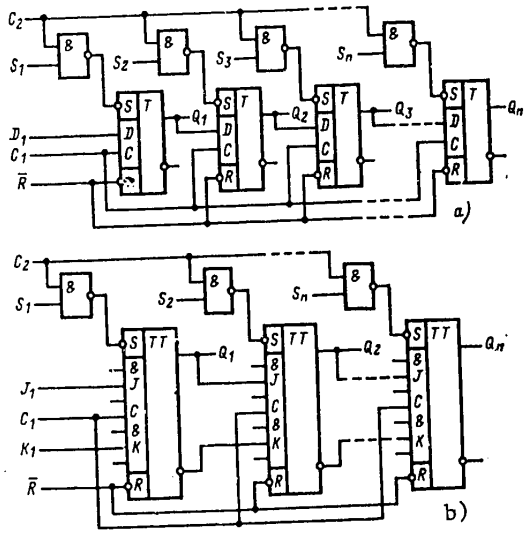


Figure 5-229. Functional diagrams of a shift register

The logical structures and operating time diagrams of the series K131, K155, and K158 JK-triggers are presented in Figures 5-230 to 5-235.

The series K131, K155, K158 JK-triggers (Figures 5-230, 5-233, 5-234) consist of two triggers: basic (the elements D_7, D_8 in Figure 5-230, 5-233 and the elements D_3, D_4 in Figure 5-234) and auxiliary (the elements D_3, D_4 in Figure 5-230, the elements D_3, D_4, D_5, D_6 in Figure 5-233, and the elements D_1, D_2 in Figure 5-234).

With the arrival of the synchronization pulse front at the input C, the information is recorded in the auxiliary trigger in accordance with the value of the signals at the inputs J and K.

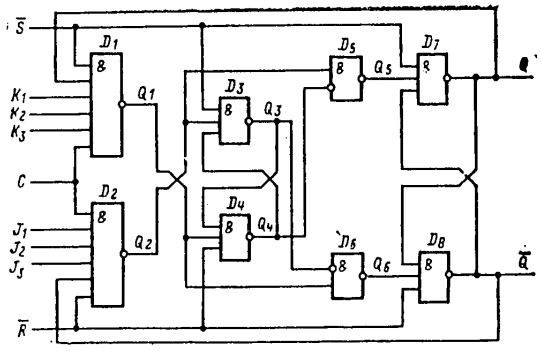


Figure 5-230. Logical structure of the K131TV1 microcircuit

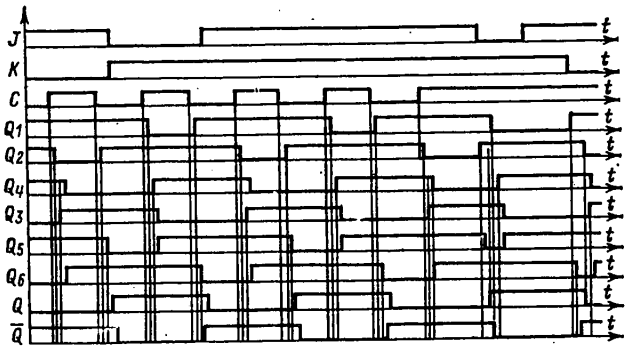


Figure 5-231. Operating time diagram of the K131TV1 microcircuit

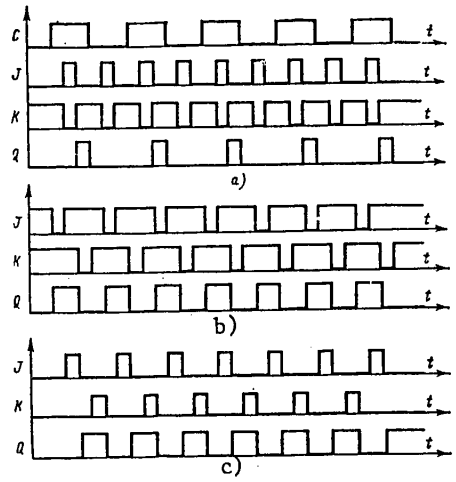


Figure 5-232. Operating time diagram of the K131TV1 microcircuit

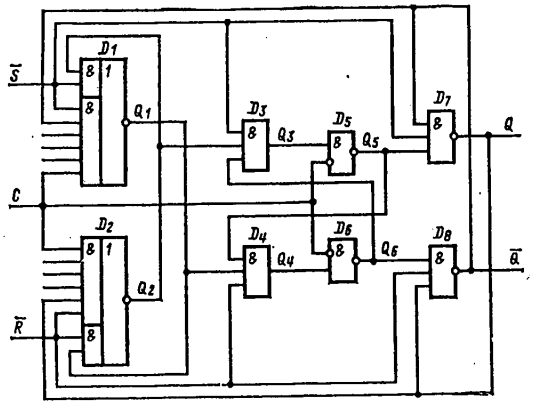


Figure 5-233. Logical structure of the K155TV1 microcircuit

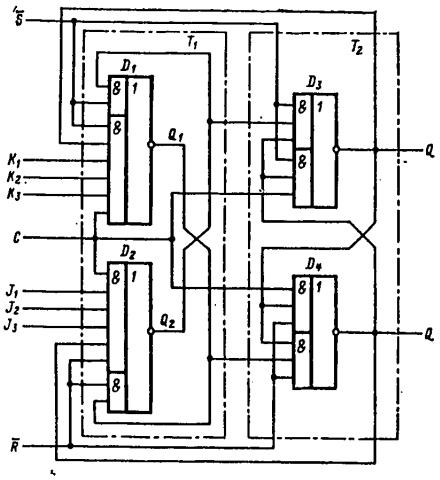


Figure 5-234. Logical structure of the K158TV1 microcircuit

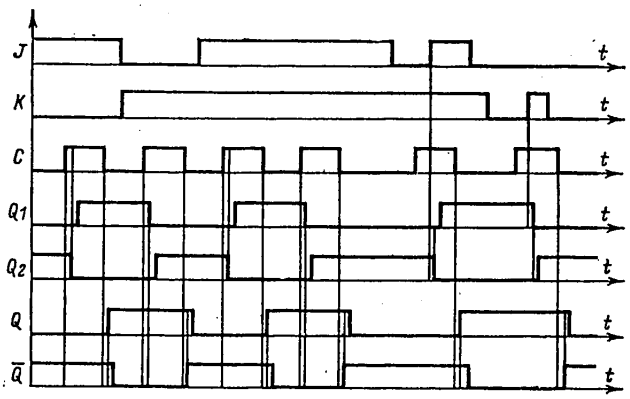


Figure 5-235. Operating time diagram of the K155TV1, K158TV1 microcircuits

Simultaneously, synchronization pulse blocks the copy circuits for copying information from the auxiliary trigger to the basic trigger (in the JK-trigger of K131TV1 total blocking does not occur). At the time of effect of the synchronization pulse the information entered in the preceding cycle is retained in the basic trigger.

With the arrival of a synchronization pulse decay, the blocking is removed, and the state is copied from the auxiliary trigger to the basic trigger.

Thus, the information is entered in the JK-trigger by the front, and the change in state at the output, by the decay of the synchronization pulse.

In the asynchronous mode the series K131, K155 and K158 JK-triggers operate with respect to the R and S inputs analogously to the ordinary RS-trigger (the states of the inputs J, K, and C are arbitrary).

In connection with the fact that the logical structure of the K131TV1 PC differs from the logical structure of the microcircuits K155TV1, K158TV1, there are significant differences in their operating logic.

The series K131 triggers (Figure 5-230) are constructed from AND-NOT elements, and they have transistorized coupling (D_5, D_6 elements) between the basic and the auxiliary triggers.

The logical structure of the K131TV1 JK-triggers also includes an element for entering a logical one in the basic trigger (the D_1 element), the element for entering the logical zero in the basic trigger (D_2 element).

The synchronization input C of the K131TV1 JK-trigger is logically equivalent to any pair of JK-inputs; therefore with the arrival of the synchronization pulse front complete blocking of the copy circuit from the auxiliary trigger to the basic trigger does not take place, and under defined conditions ($CJ_1J_2J_3Q=1$ or $CK_1K_2K_3Q=1$) a change in the output information of the trigger takes place by the decay at one of the inputs (J or K). The operating time diagrams of the JK-trigger are presented in Figure 5-232, a-c (for C=1).

This operating characteristic of the JK-triggers of the K131 series must be considered when constructing the functional units based on them. The K155 series JK-triggers (Figure 5-233) are constructed from AND-OR-NOT elements (auxiliary trigger), communication transistors D_5, D_6 and the AND-NOT elements (basic trigger). The JK-triggers of the K158 series are constructed from the AND-OR-NOT elements (Figure 5-234).

Each arm of the basic and auxiliary trigger includes the synchronization signal control element so that for all four elements permission or forbidding the introduction of synchronization is fed simultaneously, and complete blocking of the copying of the information from the auxiliary trigger to the basic one takes place.

In the presence at the synchronization input of the logical 1 level the positive pulse at the input J (for $\bar{Q}=1$) or at the input K (for Q=1) causes switching of the auxiliary trigger. In contrast to the JK-trigger of the K131 series the variation in state at the output does not take place in the given case although the auxiliary trigger "stores" this variation at the J or K input. Therefore it is not necessary to permit the appearance of false signals at the JK-inputs under the effect of the synchronization pulse.

The K131, K155 and K158 series D-triggers are universal triggers with single-phase information reception and with independent setting to the "0" and "1" states. The D-triggers of the K131, K155 and K158 series have identical logical structure and operating principle, but they are distinguished by speed and intake power. The logical structure, the operating time diagram and the truth table of the D-trigger are presented in Figure 5-236, 5-237.

The logical structure of the D-trigger contains the following elements:

The basic asynchronous RS-trigger T_3;

The auxiliary synchronous RS-trigger for entering the logical "1" in the basic trigger T_1;

The auxiliary synchronous R S-trigger for entering the logical "0" in the basic trigger T_2.

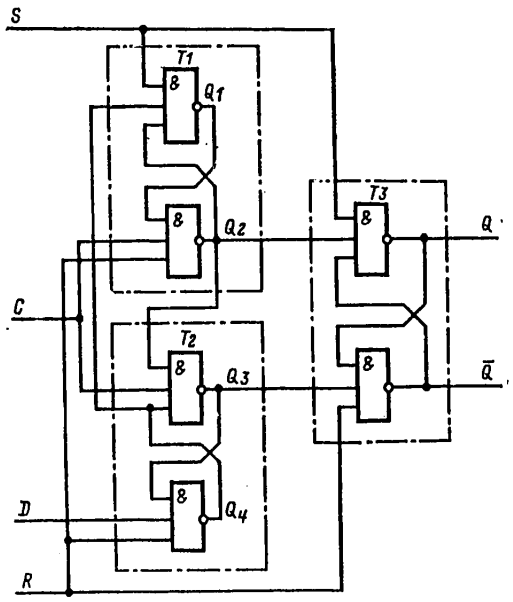


Figure 5-236. Logical structure of the K131TM2, K155TM2 and K158TM2 microcircuits

The series K131, K155, K158 D-triggers are dynamic triggers, in which the information is entered by the synchronization pulse front.

With the arrival of the synchronization pulse front at the time t the information goes to the input D, it is received in the auxiliary triggers T_1, T_2, but it appears at the output with a delay for the time t+1:Q(t+1)=D(t).

Thus, the D-trigger follows the variation of the input information at the time of arrival of the synchronization pulse front.

From the dynamic principle of operation of the D-trigger it follows that on the basis of inertia of the logical elements from which the triggers T_1-T_3 are constructed, to the right and left of the synchronization pulse front time intervals exist at the input C, during which the information at the input D must not change; otherwise "overruns" will occur in the D-trigger and ambiguous entry of the information in the trigger will occur.

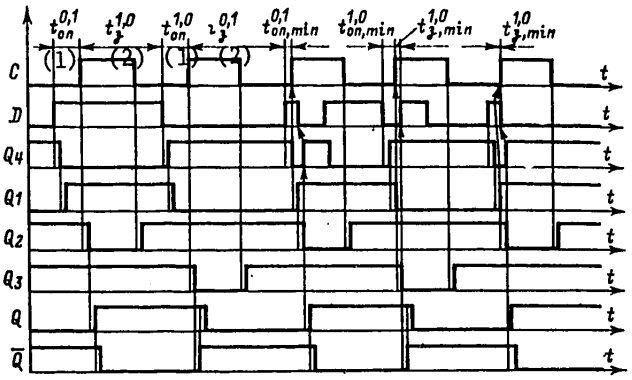


Figure 5-237. Operating time diagram of the K131TM2, K155TM2, and K158TM2 microcircuits

Key:
1. lead
2. delay

For stable operation of the D-trigger the following relations must be observed (Figure 5-237):

$$t^{0,1}_{\underset{(1)}{on},\,min} \leqslant t^{0,1}_{on} \leqslant T - t^{0,1}_{\underset{(2)}{3},\,min};$$
$$t^{1,0}_{on,\,min} \leqslant t^{1,0}_{on} \leqslant T - t^{1,0}_{3,\,min};$$
$$t^{0,1}_{3,\,min} \leqslant t^{0,1}_{3} \leqslant T - t^{0,1}_{on,\,min};$$
$$t^{1,0}_{\underset{(2)}{3},\,min} \leqslant t^{1,0}_{3} \leqslant T - t^{1,0}_{\underset{(1)}{on},\,min},$$

Key: 1. lead; 2. delay

where T is the synchronization pulse repetition period; $t^{0,1}_{lead}$, $t^{1,0}_{lead}$ is the lead time of the front and the information decay at the input D from the synchronization pulse front at the input C; $t^{0,1}_{delay}$, $t^{1,0}_{delay}$ is the delay time of the front and information decay at the input D from the synchronization pulse front at the input C; $t^{0,1}_{lead,\,min}$; $t^{1,0}_{lead,\,min}$; $t^{0,1}_{delay,\,min}$; $t^{1,0}_{delay,\,min}$ are the limiting minimum values of the time; $t^{0,1}_{lead}$; $t^{1,0}_{lead}$; $t^{0,1}_{delay}$; $t^{1,0}_{delay}$ are the same, respectively, for which fitness of the D-trigger is maintained.

The arrows in Figure 5-237 are pointed at the time on the variable t access, beginning with which the variation of this variable to the opposite is not felt in the processes in the D-trigger, for it is "blocked" by variation of another variable to which the tail end of the arrow is pointed.

The values of $t^{1,0}_{lead,\,min}$; $t^{0,1}_{lead,\,min}$; $t^{1,0}_{delay,\,min}$; $t^{0,1}_{delay,\,min}$ are the dynamic parameters of the D-trigger and along with the other parameters determine the possibility of the construction and use of the functional units (for example, shift registers) based on D-triggers. However, not all of the parameters

$t^{1,0}_{lead,\ min}$; $t^{0,1}_{lead,\ min}$; $t^{0,1}_{delay,\ min}$; $t^{1,0}_{delay,\ min}$ are necessary. From analysis of Figure 5-237 we have the qualitative relations:

$$t^{1,0}_{lead,\ min} > t^{0,1}_{lead,\ min}; t^{0,1}_{delay,\ min} > t_{delay,\ min},$$

and from Figure 5-237 it is obvious that on variation of the state of the outputs Q and $\overline{Q}$ of the D-trigger overlapping of the high levels takes place, that is, first comes the front on one of these inputs, and then the drop on the others; therefore for analysis of the fitness of the D-trigger circuit it is sufficient to consider the parameters $t^{1,0}_{lead,\ min}$ and $t^{1,0}_{delay,\ min}$.

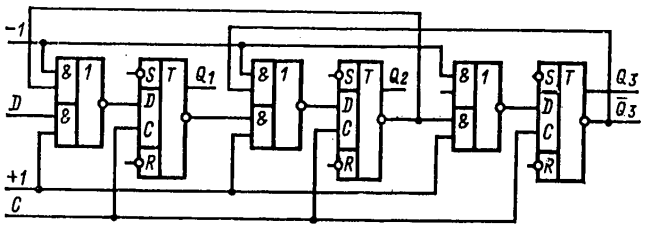


Figure 5-238. Functional diagram of a reversible shift register

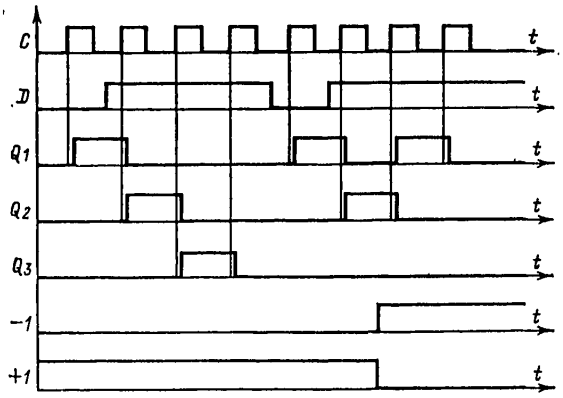


Figure 5-239. Operating time diagram of a reversible shift register

In the asynchronous mode the series K131, K155 and K158 D-triggers operate analogously to the RS-trigger (the states of the inputs D, C are arbitrary).

The functional diagrams of the reversible shift triggers and their operating time diagrams are presented in Figures 5-238 to 5-242.

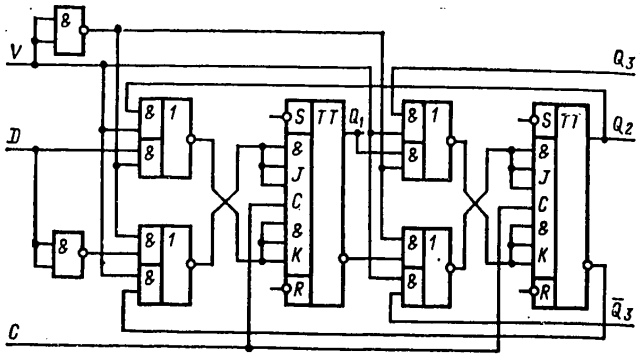


Figure 5-240. Functional diagram of a reversible shift register

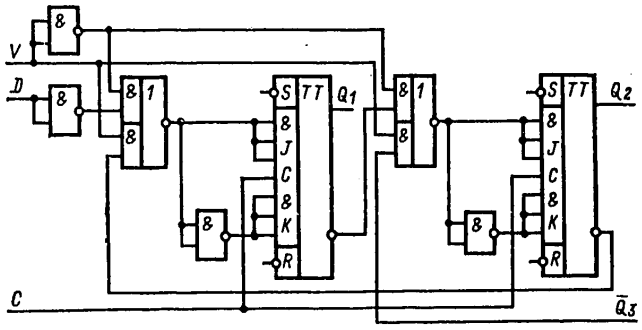


Figure 5-241. Functional diagram of a reversible shift register

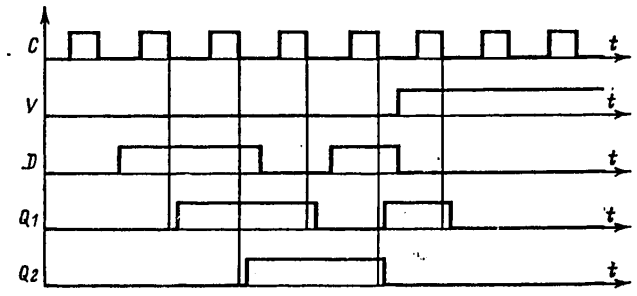


Figure 5-242. Operating time diagram of a reversible shift register

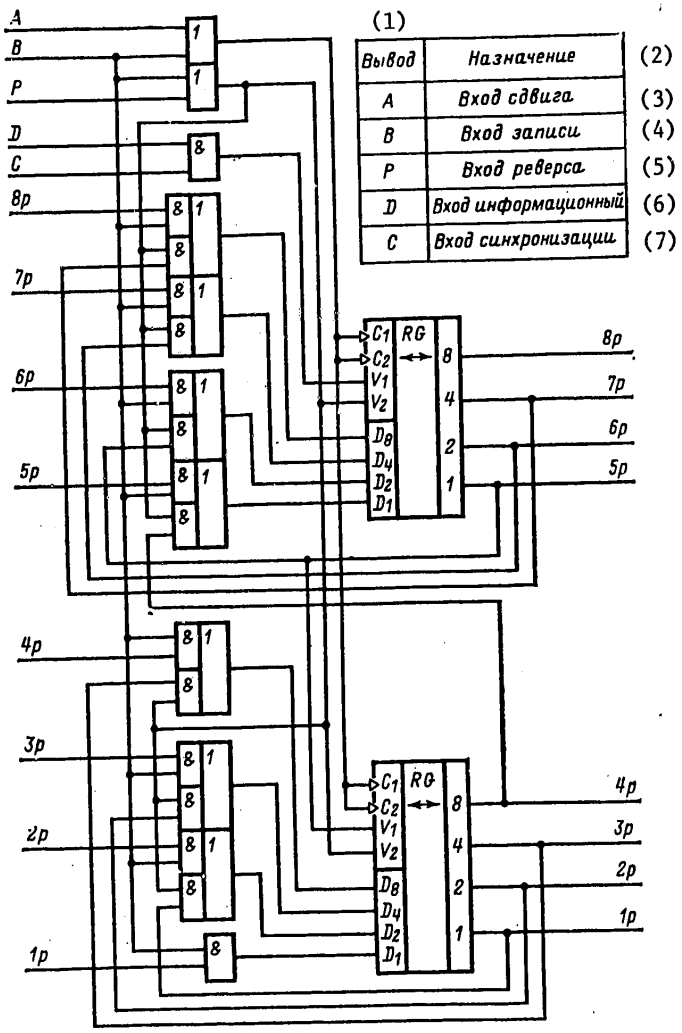


Figure 5-243. Functional diagram of an eight-bit reversible shift register

Key:

1. Lead
2. Purpose
3. Shift input
4. Entering input
5. Reversing input
6. Information input
7. Synchronization input

The diagram presented in Figure 5-240 has higher speed, but it requires a larger number of logical elements than the diagram presented in Figure 5-241. The operating time diagram of the circuit is presented in Figure 5-242. If the last two circuits are executed from JK-triggers of the K131 series, then the reverse V and variation of information at the information input D must be realized in the absence of a synchronization pulse at the "shift" C input.

The diagram of a reversible shift counter based on the K155IR1 microcircuit and using elements with a low degree of integration is presented in Figure 5-243.

A 10-bit shift register is depicted in Figure 5-244. It is executed on the basis of four-bit universal shift registers of the K155IR1 series. For construction of the n-bit shift register it is necessary to connect the output of the last bit of the universal register to the series input V of the next register. In this case the time required for the code shift by n bits is:

$$t_n = nt_{shift},$$

where t_{shift} is the time required to shift the code by 1 bit.

Two modes are possible in the operation of the shift register -- "enter" and "shift." The mode control is realized by the "mode" signal coming to the input V_2.

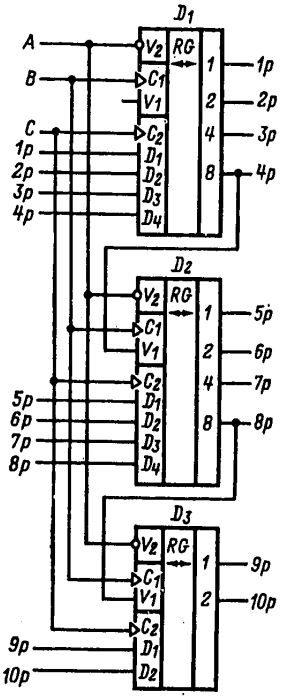


Figure 5-244. Functional diagram of a shift register.
A -- mode input; B -- shift input; C -- enter input

If the "mode" signal is equal to "1," the register operates in the "enter" mode. In this case the informatin reaching the inputs D_1-D_4 is entered in the register by the synchronization signal drop C_2. If the "mode" signal is equal to "0," the information shift takes place by the drop of the synchronization signal reaching the input C_1.

The time diagrams explaining the operation of the shift register are presented in Figure 5-245.

Adders. The functional diagram of the single-bit adder (Figure 5-246) with direct and inverse addent codes is constructed from AND-NOT logical elements.

The functional diagram of a single-bit adder (Figure 5-247) is constructed from AND-OR-NOT logical elements.

The functional diagram of a single-bit adder using only direct addend codes (Figure 5-248) is constructed from the AND-NOT logical elements.

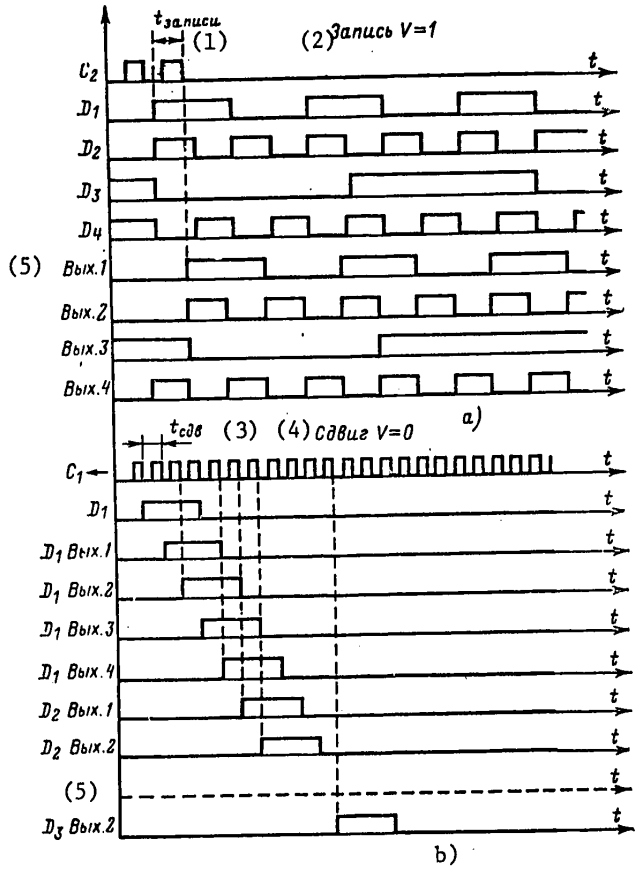


Figure 5-245. Operating time diagram of the shift register

Key: 1. enter; 2. enter V=1; 3. t_{shift}; 4. shift V=0; 5. output ...

The functional diagram of a four-bit adder with parallel carry constructed according to the system of structural logical equations is presented in Figure 5-249.

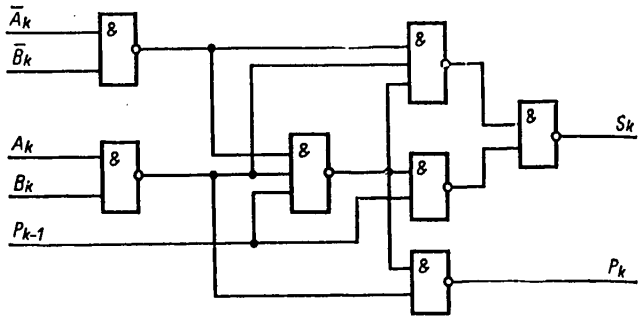


Figure 5-246. Functional diagram of a single-bit adder with direct and inverse addend codes

A_k	B_k	P_{k-1}	S_k	P_k	A_k	B_k	P_{k-1}	S_k	P_k
0	0	0	0	0	0	1	1	0	1
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
1	0	0	1	0	1	1	1	1	1

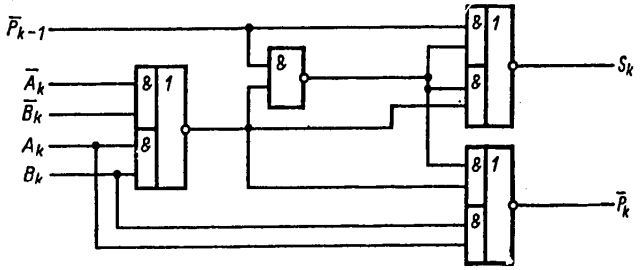


Figure 5-247. Functional diagram of a single-bit adder based on AND-OR-NOT logical elements

A_k	B_k	P_{k-1}	S_k	P_k	A_k	B_k	P_{k-1}	S_k	P_k
0	0	0	0	0	0	1	1	0	1
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
1	0	0	1	0	1	1	1	1	1

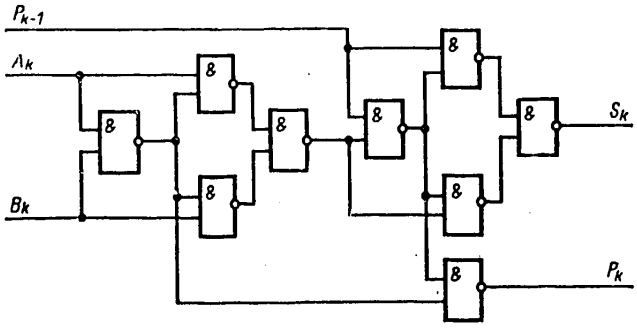


Figure 5-248. Functional diagram of a single-bit adder with direct addend codes

A_k	B_k	P_{k-1}	S_k	P_k	A_k	B_k	P_{k-1}	S_k	P_k
0	0	0	0	0	0	1	1	0	1
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
1	0	0	1	0	1	1	1	1	1

Figure 5-250 depicts an accumulating adder executed on the basis of full combination adders and memory register.

Before beginning summation, all the memory registers are zeroed. For this purpose the mode switching signal -- logical 0 -- is fed to the inputs V_2. Figure 5-251 explains the process of zeroing the memory register in the example of zeroing a universal register D_4. A zero signal is fed to the series input V_1. Then the signal is entered in series in all four bits of the register by shifting the input information in 4 cycles of the "zeroing" signal reaching the input C_1. As a result of the given operation the register is zeroed.

The number code which is added to the contents of the memory register reaches the input of the full combination adder. The obtained sum is entered in the memory register at the time the "enter" signal C_2 drops, for the mode switching signal equal to "1." Thus, the given sum will be the addend for the next added number. The addition time includes the response time of the adder and the time for entering the sum in the register:

$$t_\Sigma = nt_c + t_{вв}, \quad (1)$$

Key: 1. enter

where n is the number of full combination adders; t_c is the maximum summation time of the full combination adder; t_{enter} is the time for entering the sum in the memory register.

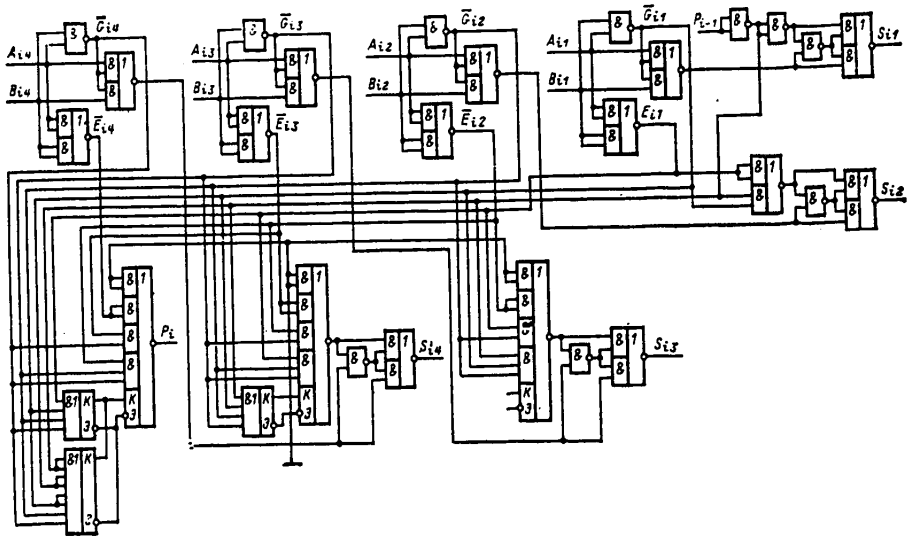


Figure 5-249. Functional diagram of a four-bit adder with parallel carry and direct addend codes.

$$S_{ik} = \overline{A_{ik}\bar{G}_{ik} + B_{ik}\bar{G}_{ik}}\,\overline{A_{ik}\bar{G}_{ik} + B_{ik}\bar{G}_{ik}}P_{i-1} + P_{i-1}\overline{A_{ik}\bar{G}_{ik} + B_{ik}\bar{G}_{ik}}P_{i-1};$$

$$P_i = \overline{\bar{E}_{i4} + \bar{G}_{i4}\bar{E}_{i3} + \bar{G}_{i4}\bar{G}_{i3}\bar{E}_{i2} + \bar{G}_{i4}\bar{G}_{i3}\bar{G}_{i2}\bar{E}_{i1} + \bar{G}_{i4}\bar{G}_{i3}\bar{G}_{i2}\bar{P}_{i-1}};$$

$$\bar{G}_{ik} = \overline{A_{ik}B_{ik}}; \qquad E_{ik} = \overline{A_{ik} + B_{ik}}.$$

A functional diagram of the addition of two four-bit positive numbers based on the K155IM2 and K155TM5 microcircuits is presented in Figure 5-252.

The functional diagram of a series adder based on the K155TV1 (D_1, D_2, D_4), K155IM1 (D_3) microcircuits and AND-NOT elements is presented in Figure 5-253. The triggers D_1 and D_2 are used to convert the direct code to complementary code, where the logical zero level at the "sign A" and "sign B" inputs corresponds to a positive sign of the number, and the logical one, a negative sign. The trigger D_4 is used to store the carry of the preceding bit.

Decoders. The functional diagram of a full three-bit decoder constructed from the AND-NOT and the AND-OR-NOT elements is presented in Figure 5-254.

Figure 5-255 shows the diagram of the "1 out of 32" decoder executed from the K155ID3 PC. The information in the form of a five-bit binary number is fed to the input of the decoder. Here four low-order bits of the number are fed directly to the corresponding information inputs A_0, A_1, A_2, A_3. The high-order bit of the number is fed directly to the gating input W_0 of the microcircuit D_2 and to the gating input $\overline{W}_0$ of the microcircuit D_3 through the inverter.

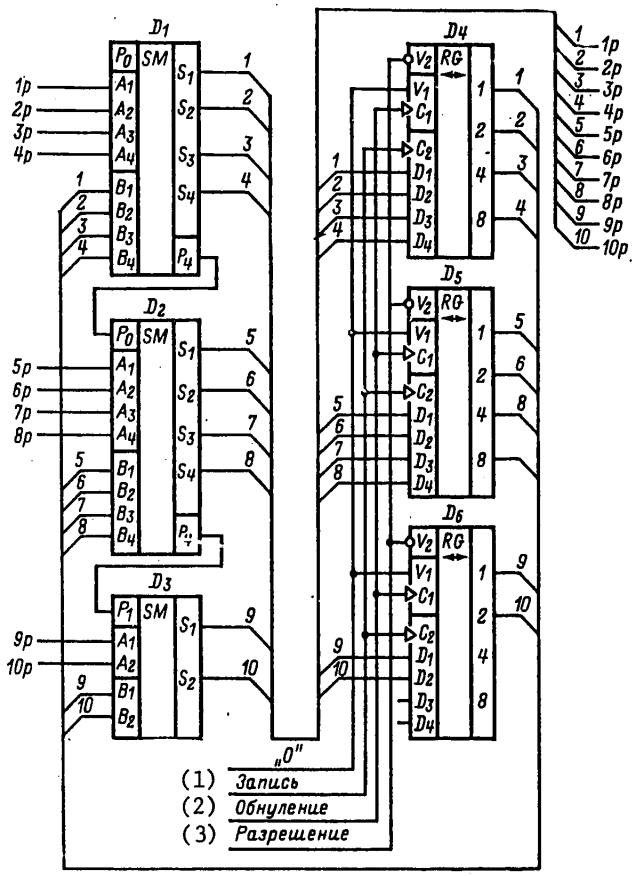


Figure 5-250. Functional diagram of an accumulating adder. D_1, D_2 -- K155IM3 microcircuit; D_3 -- K155IM2 microcircuit; D_4-D_6 -- K155IR1 microcircuit

Key:

1. Enter
2. Zeroing
3. Permission

For a decimal number light display the K155ID1 high-voltage decoder is used. The functional diagram for connecting the K155ID1 microcircuit to the IN-16 (IN-4, IN-12, IN-14) display tube is presented in Figure 5-256. Other tubes operating anode voltage of 170-200 volts can be used as the display; here it is necessary to consider that the working cathode current must not exceed 7 milliamps, and the leakage current on the cathode of a number that is not lit up must not exceed 250 microamps in the temperature range. The resistor R in the anode feed circuit is used to reduce the logical 1 voltage at the output of the decoder. Signals corresponding to the lit number in binary code are fed to the input X_1-X_4 to illuminate the numbers.

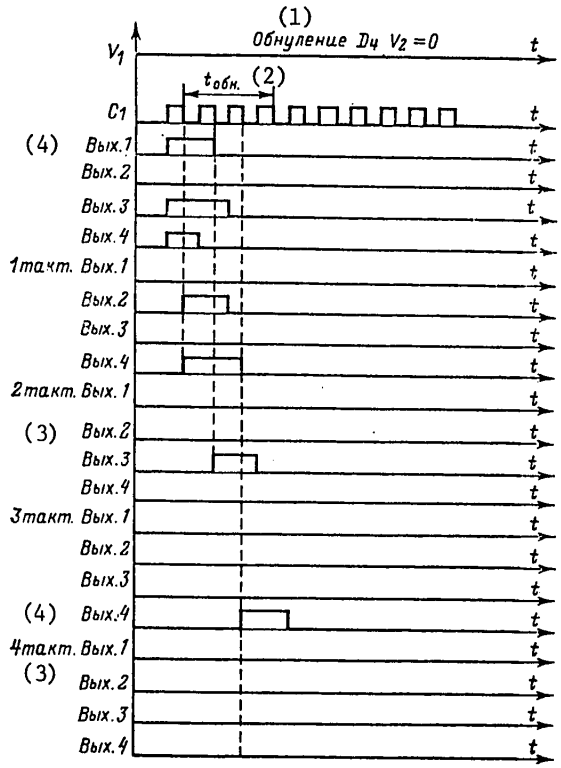


Figure 5-251. Time diagram of zeroing the memory register of an accumulating adder

Key:
1. Zeroing
2. $t_{zeroing}$
3. Cycles
4. Output ...

Comparison Circuits. The functional diagram and logical equation of a comparison circuit realizing the function of equivalence are presented in Figure 5-257.

The functional diagram and system of logical equations of a four-bit comparison circuit realizing the function of equality, strict and unstrict inequality are presented in Figure 5-258.

A comparison circuit of two four-bit numbers executed from the K155IM1 microcircuit and AND-NOT elements is presented in Figure 5-259.

An equality circuit of two four-bit numbers executed from K155ID3 and K155KP7 microcircuits and the AND-NOT elements is presented in Figure 5-260.

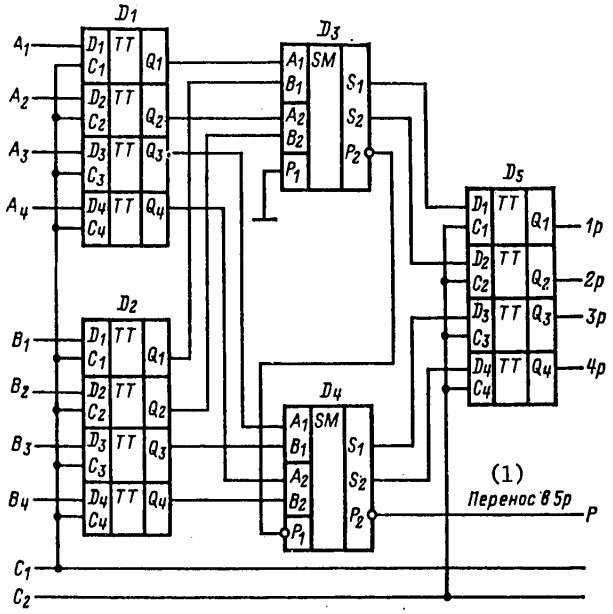


Figure 5-252. Functional diagram of the addition of two four-bit positive numb ers A and B.
D_1, D_2, D_5 -- K155TM5 microcircuits; D_3, D_4 -- K155IM2 microcircuit

Key:
1. carry to 5p

A diagram of a pulse filter executed from AND-NOT elements in the form of four RS-triggers (8 AND-NOT elements) connected through four inverters to the AND-NOT element providing for shaping of the output signal, is presented in Fig 5-261.

The operating principle is explained by the time diagrams presented in Fig 5-262. A signal of duration τ_1 subject to filtration and interference pulses of duration $\Delta\tau_1$ reach the input X of the filter which is in the form of parallel-connected inputs X of four RS-triggers. The complementary pulse signals A, B, $\overline{A}$, $\overline{B}$ come to the minority inputs of the filter which are in the form of "0" inputs of the RS-triggers.

The order of feeding the complementary pulse signals is presented in the diagram. The duration of the auxiliary signal pulse τ_2 is related to the duration of the interference pulse $\Delta\tau_1$ by the expression

$$\Delta\tau_1 \leqslant \tau_2.$$

Depending on the time position of the interference, it is suppressed in one of the four RS-triggers.

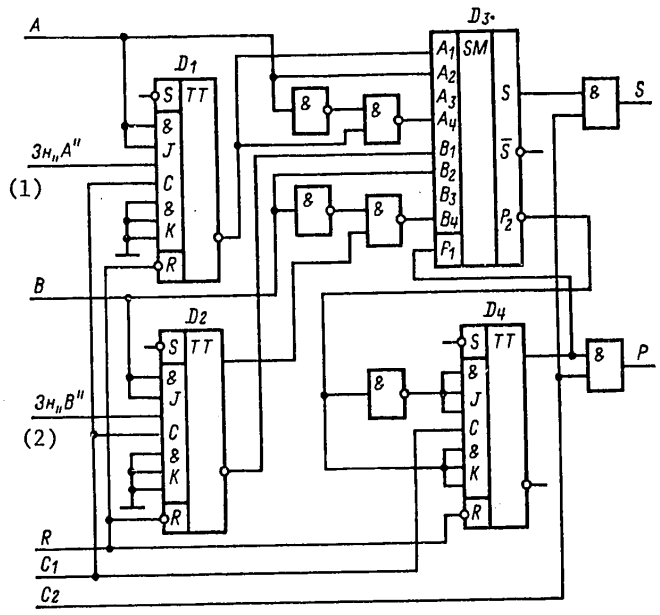


Figure 5-253. Functional diagram of a series adder

Key:
1. Sign "A"
2. Sign "B"

The use of four RS-triggers insures suppression of the interference arbitrarily arranged in time. On passage of the input pulse through the triggers its front is delayed in the case where the pulse front at the S-input coincides with a positive voltage of the pulse reaching the R-input.

As a result of the effect of the basic and the complementary pulse signals on the "0" or "1" inputs of the RS-triggers, pulses are shaped at the inputs X of the RS-triggers which go to the input of the element D_4. A negative pulse free of interference is shaped at the output Y.

The pulse delay circuit is presented in Figure 5-263. The circuit consists of four delay elements, each of which is 2 series-connected RS-triggers.

The operating principle of the circuit is explained by the time diagrams presented in Figure 5-264.

The circuit delays the pulse reaching the input X. At the output of the delay circuit (output Y) a pulse is formed which is delayed with respect to the input pulse by $t_{del}=\tau_2/2$.

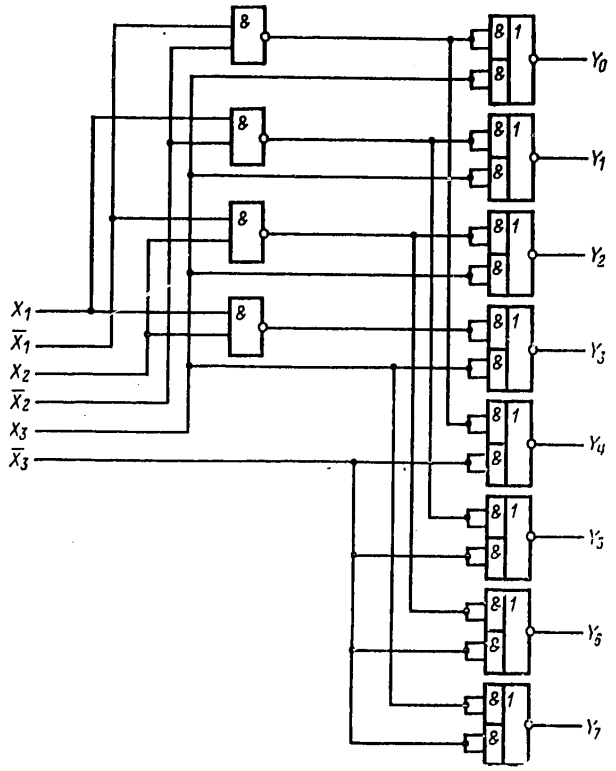


Figure 5-254. Functional diagram of a three-bit decoder

(1) Десятичная цифра	(2) Двоично-десятичный код			(3) Десятичный код							
	x_3	x_2	x_1	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
2	0	1	0	0	0	1	0	0	0	0	0
3	0	1	1	0	0	0	1	0	0	0	0
4	1	0	0	0	0	0	0	1	0	0	0
5	1	0	1	0	0	0	0	0	1	0	0
6	1	1	0	0	0	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	0	1

Key:
1. Decimal number
2. Binary-decimal code
3. Decimal code

In order to increase the delay by n times, it is necessary to connect n delay elements in series; then the total delay time will be defined as $t_{del}=n\tau_2/2$.

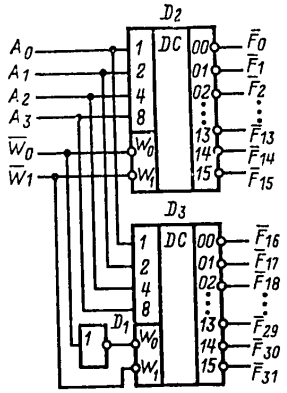


Figure 5-255. Functional diagram of a 1 out of 32 decoder

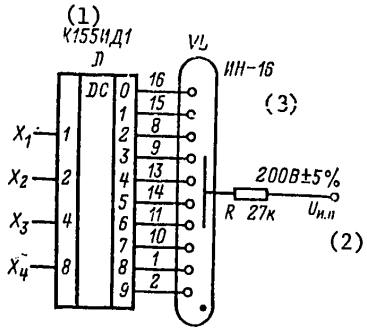


Figure 5-256. Functional diagram of the joint operation of a K155ID1 microcircuit with a gas discharge display

Key:
1. K155ID1
2. $U_{p.s}$
3. IN-16

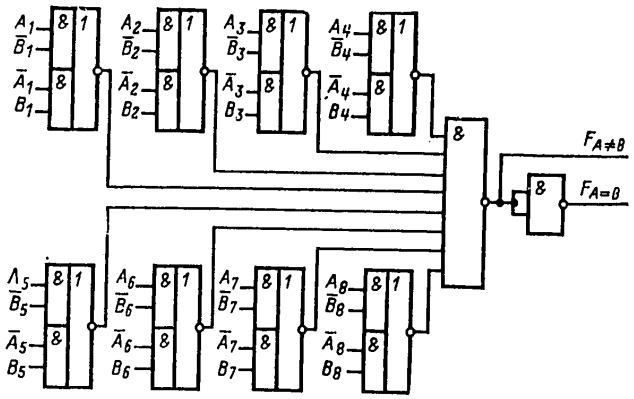


Figure 5-257. Functional diagram of a comparison circuit realizing the equivalence function

In the given example the case is considered where it is necessary to coordinate the input pulse front and decay with the front of the cycle pulse fed to the input A and the decay of the cycle pulse fed to the input B. In the given case a pulse (output Y) delayed with respect to the input pulse is also shaped.

The pulse shaper circuit and diagram explaining the operating principle of the circuit are presented in Figure 5-265.

The pulse shaper is in the form of two RS-triggers series connected through an inverter, each of which consists of two AND-NOT elements. The circuit expands the input pulse. A pulse of negative polarity with duration τ_1 reaches the basic input x, and cycle pulses shifted in time with a repetition period of $2t_2$ are fed to the auxiliary input x_2, x_3. For the case of $\tau_1 >> t_2$ an example of the operation of the circuit is presented in Figure 5-265, b. A pulse of positive polarity of duration $\tau_2=\tau_1+t_2/2$ is picked up from the output D_1.

From the output of the pulse shaper D_4 the expanded pulse of positive polarity with duration $\tau_3=\tau_1+t_2$ is picked up. For n RS-triggers series-connected through inverters, the shaper circuit permits expanded pulses of duration $\tau_3=\tau_1+nt_2$ to be obtained.

Figure 5-265, c illustrates the obtaining of an expanded pulse at the element output for the case $\tau_1 << t_2$.

In Figure 5-266 a diagram is presented for a multiplexer-selector from 16 channels to one with gating executed from a K155KP7 microcircuit and logical element.

Figure 5-267 gives an example of the application of the K155IP2 microcircuit as a nine-bit parity check circuit.

Figure 5-268 gives a diagram of a storage element with the application of K155TM5 or K155TM7 microcircuit jointly with the key switches. On pressing one of the 4 keys (S_1-S_4) a logical one voltage appears at the corresponding input D of the microcircuit K155TM5 (K155TM7). A logical one voltage is also fed through the inverter to the synchronization input. This causes the selected trigger to be set. Since a logical zero is fed to all other D-inputs, all the remaining memory cells are initialized. The vibration of the key contacts has no effect on the given system.

The functional diagram of a module of a ready-access memory with 64 single-bit words using the K155RU1 and K155ID1 microcircuits is presented in Figure 5-269.

The inputs W_0 and W_1 and the outputs F_1 of the microcircuit are combined respectively. In order to obtain 64 addresses the inputs X and the inputs Y are joined in pairs.

A diagram of a ready-access memory for 16 four-bit words executed from the K155RU1 microcircuit and logical elements is presented in Figure 5-270.

This circuit has 4 control inputs (A,B,C,D) permitting the required word to be accessed, the access permission input V, the information enter permission input V_1 and the information entry inputs 1p, 2p, 3p, 4p.

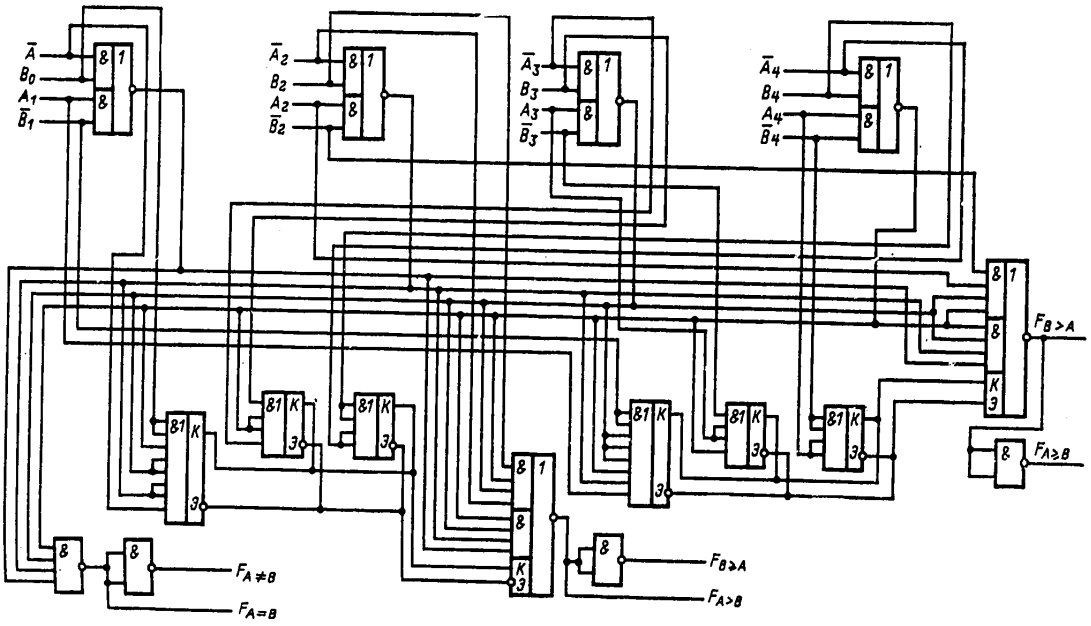


Figure 5-258. Functional diagram of a four-bit comparison circuit realizing the function of the quality, strict and nonstrict inequality

$$F_{B>A} = \overline{A_4\bar{B}_4 + A_3\bar{B}_3(\overline{\bar{A}_4B_4 + A_4\bar{B}_4}) + A_2\bar{B}_2(\overline{\bar{A}_3B_3 + A_3\bar{B}_3})(\overline{\bar{A}_4B_4 + A_4\bar{B}_4}) + A_1\bar{B}_1(\overline{\bar{A}_2B_2 + A_2\bar{B}_2})(\overline{\bar{A}_3B_3 + A_3\bar{B}_3})(\overline{\bar{A}_4B_4 + A_4\bar{B}_4}) + (\overline{\bar{A}_1B_1 + A_1\bar{B}_1})(\overline{\bar{A}_2B_2 + A_2\bar{B}_2})(\overline{\bar{A}_3B_3 + A_3\bar{B}_3})(\overline{\bar{A}_4B_4 + A_4\bar{B}_4})};$$

$$F_{A>B} = \overline{\bar{A}_4B_4 + \bar{A}_3B_3(\overline{\bar{A}_4B_4 + A_4\bar{B}_4}) + \bar{A}_2B_2(\overline{\bar{A}_3B_3 + A_3\bar{B}_3})(\overline{\bar{A}_4B_4 + A_4\bar{B}_4}) + A_1\bar{B}_1(\overline{\bar{A}_2B_2 + A_2\bar{B}_2})(\overline{\bar{A}_3B_3 + A_3\bar{B}_3})(\overline{\bar{A}_4B_4 + A_4\bar{B}_4}) + (\overline{\bar{A}_1B_1 + A_1\bar{B}_1})(\overline{\bar{A}_2B_2 + A_2\bar{B}_2})(\overline{\bar{A}_3B_3 + A_3\bar{B}_3})(\overline{\bar{A}_4B_4 + A_4\bar{B}_4})};$$

$$F_{A=B} = \overline{(\overline{\bar{A}_1B_1 + A_1\bar{B}_1})(\overline{\bar{A}_2B_2 + A_2\bar{B}_2})(\overline{\bar{A}_3B_3 + A_3\bar{B}_3})(\overline{\bar{A}_4B_4 + A_4\bar{B}_4})};$$

$$F_{A \neq B} = \overline{F_{A=B}}.$$

In complex logical systems multiphase cycle clocks are required to control the individual functions. Figure 5-271 shows a diagram of a multiphase cycle clock executed from the K155IR1, K155LI1, and K155LR4 microcircuits.

All of the register inputs are connected to each other through an OR-inverting cell, the output of which is connected to the series input of the register. Therefore the logical zero signals will be entered in the register while there is a logical one voltage at one of the outputs of the register. After four cycle pulses the microcircuit K155LI1 is switched, after which there will be a logical one voltage at the series input during the cycle period time.

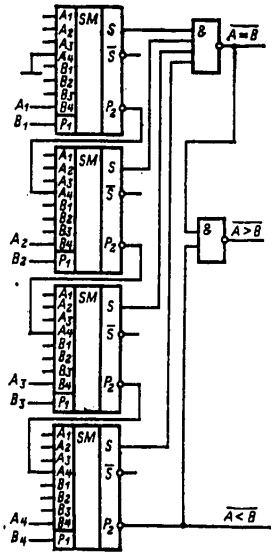


Figure 5-259. Functional diagram of a comparison circuit for two four-bit numbers

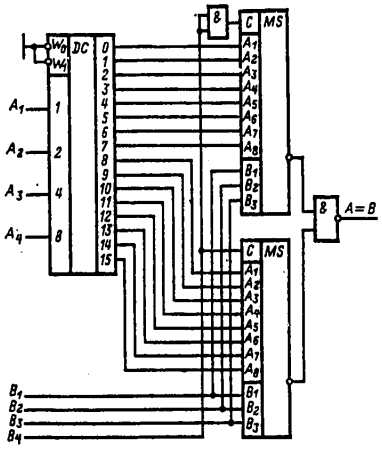


Figure 5-260. Functional diagram of the equality of two four-bit numbers

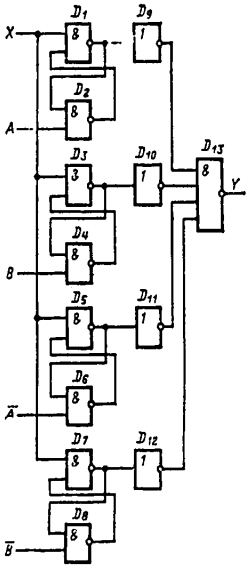


Figure 5-261. Functional diagram of a pulse filter

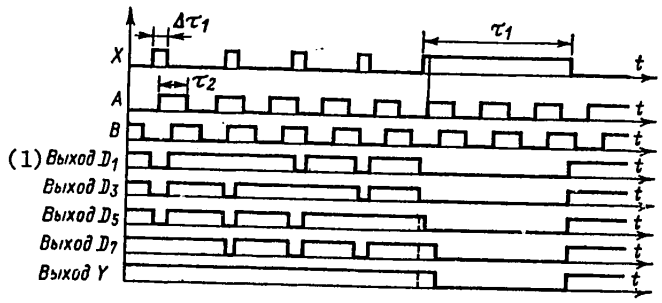


Figure 5-262. Time diagram of a pulse filter

Key:

1. Output ...

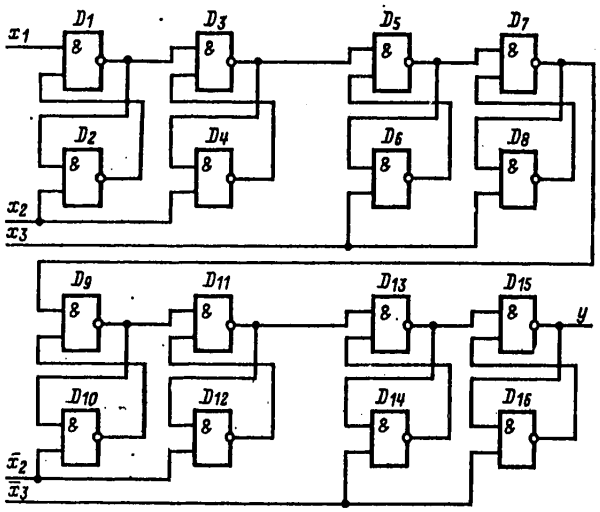


Figure 5-263. Functional diagram of a delay circuit

Accordingly, the logical one will occur only at one output of the register. In order to prevent superposition of cycle signals formed in this way on each other, all of the register outputs are connected to the K155LN1 microcircuit performing the AND function, the other inputs of which are fed the initial cycle signal.

A diagram of a fast parallel multiplier executed from four K155LI1 and three K155IM3 microcircuits is presented in Figure 5-272.

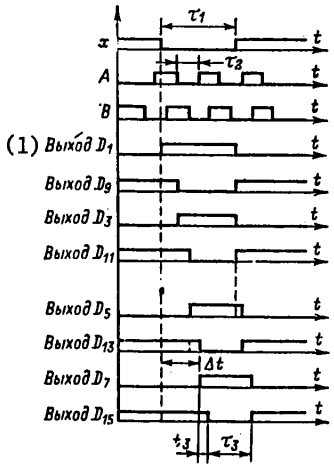


Figure 5-264. Time diagram of a delay circuit
Key:
1. Output

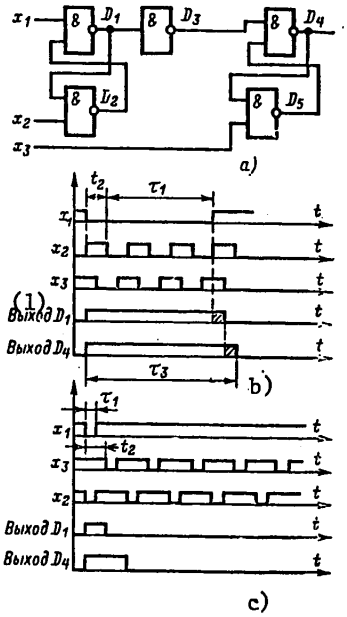


Figure 5-265. Functional diagram (a) and time diagrams (b, c) of a pulse shaper
Key:
1. Output

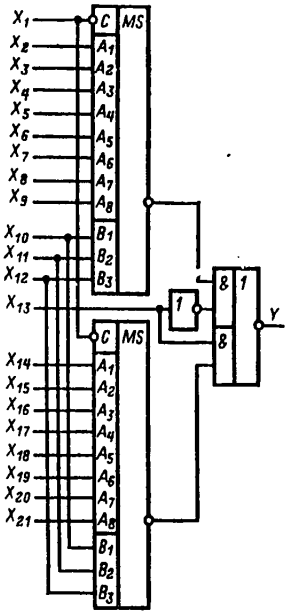


Figure 5-266. Functional diagram of a multiplexer-selector of 16 channels to 1

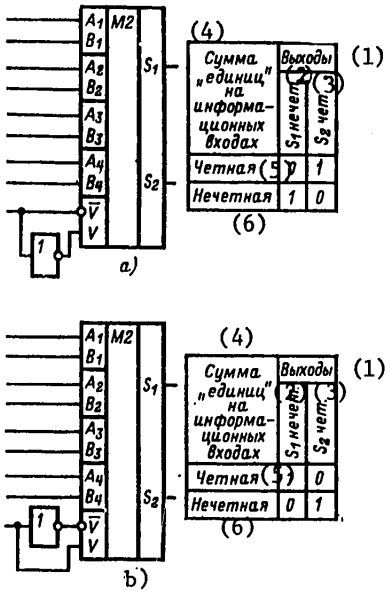


Figure 5-267. Functional diagram of a parity check circuit for nine bits

Key:
1. Outputs
2. S_1 odd
3. S_2 even
4. "ones" sum at the information inputs
5. even
6. odd

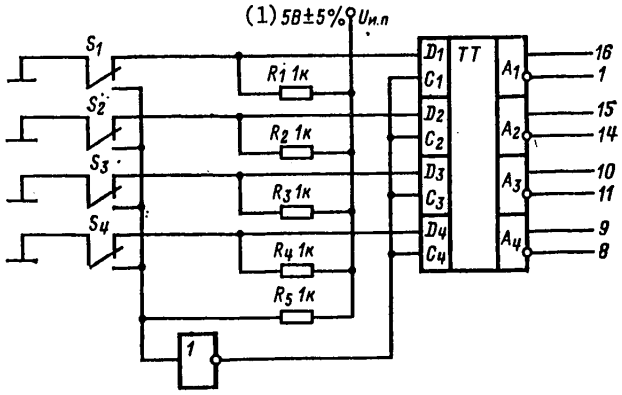


Figure 5-268. Functional diagram of a storage element

Key:
1. 5 volts±5% $U_{p.s}$

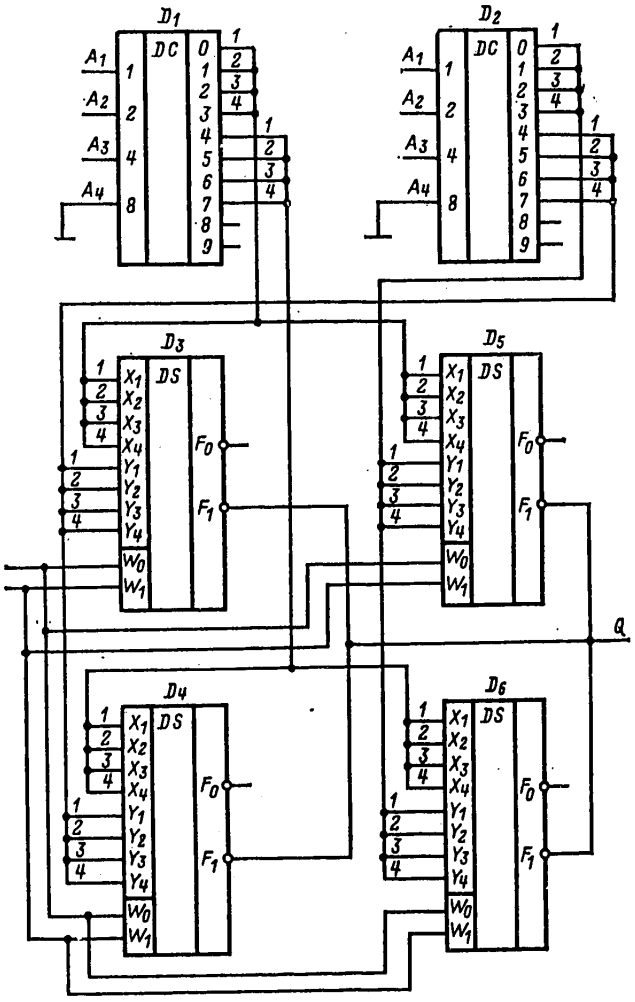


Figure 5-269. Functional diagram of a memory module

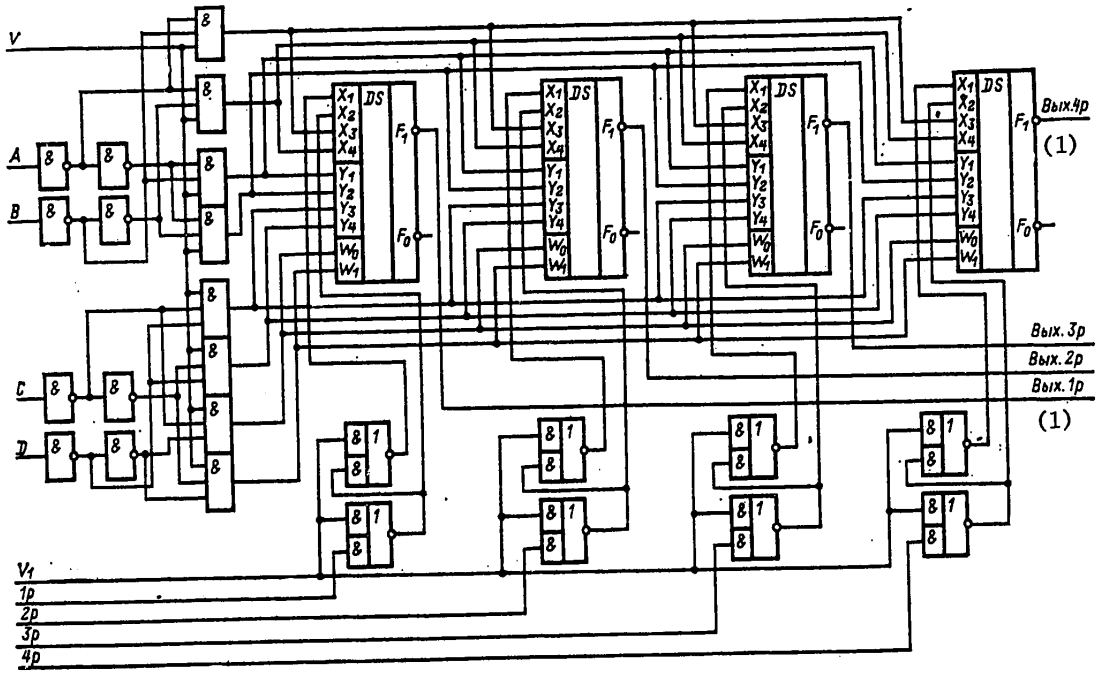


Figure 5-270. Functional diagram of a ready-access memory of 16 four-bit words

Key:

1. Output ...

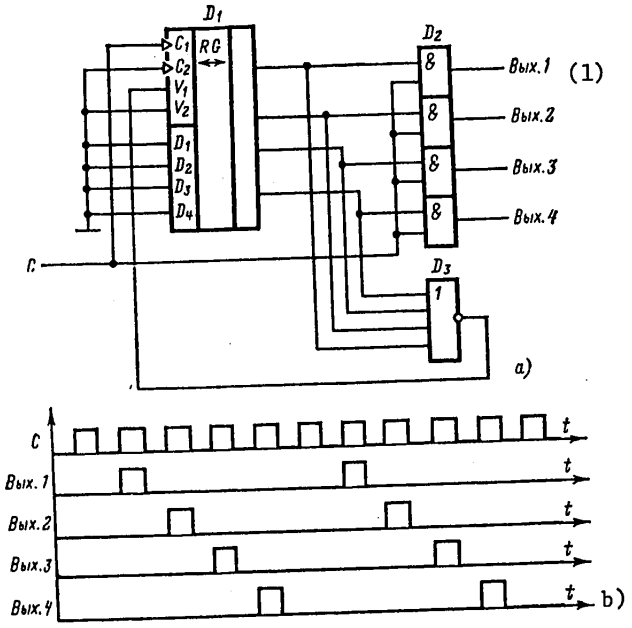


Figure 5-271. Functional diagram (a) and operating time diagram (b) of a multiphase cycle clock

Key:

1. Output ...

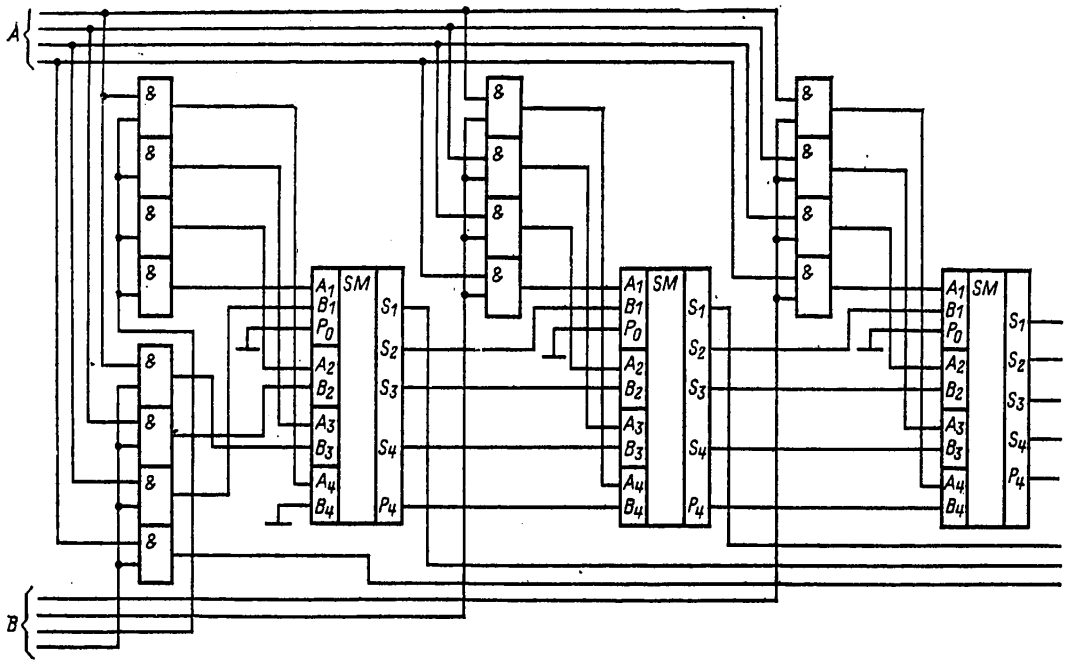


Figure 5-272. Functional diagram of a fast parallel multiplier

5-3. Examples of the Construction of the Functional Units of Electronic Equipment Based on Analog Microcircuits

In this section some examples are presented of the construction of the functional units of electronic equipment based on analog integrated microcircuits with approximate electrical parameters of these units at normal temperature.

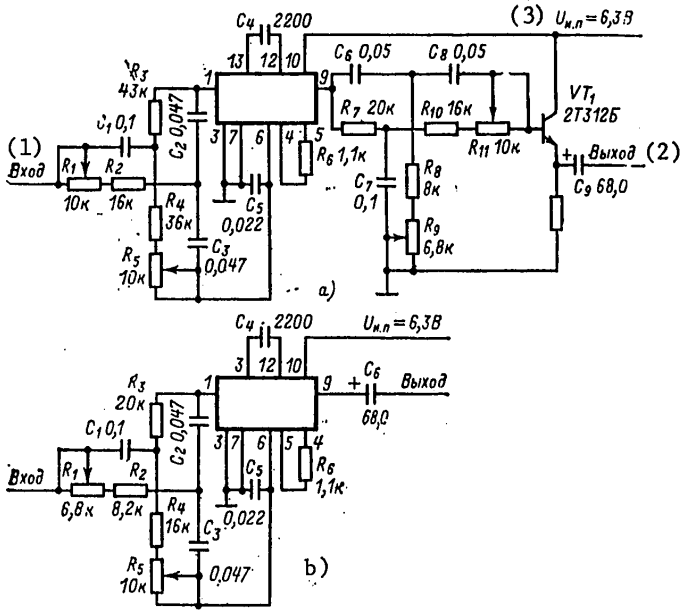


Figure 5-273. Diagrams of selective amplifiers based on the 123UN1A microcircuit
a -- for a frequency of 80 hertz; b -- for a frequency of 160 hertz

Key:
1. Input
2. Output
3. $U_{p.s}$=6.3 volts

Selective Amplifier Based on the 123UN1A Microcircuit	
Central pass band frequency	80 hertz
Pass band width at the 0.7 level	6 hertz
Input voltage	1.0 millivolts
Input impedance	20 kilohms
Output voltage no less than	2 volts

Selective Amplifier Based on the 123UN1A Microcircuit	
Central pass band frequency	160 hertz
Pass band width at the 0.7 level	10 hertz
Input voltage	3.0 millivolts
Output voltage no less than	1.5 volts

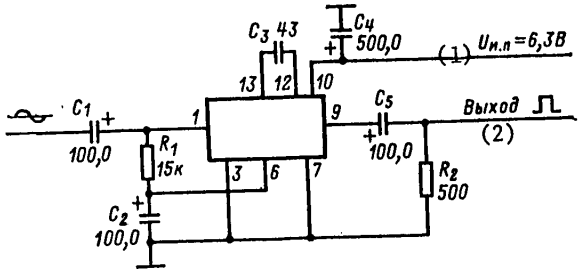


Figure 5-274. Diagram of an amplifier-limiter based on the 123UN1A microcircuit

Key:
1. $U_{p.s}$=6.3 volts
2. Output

Amplifier-Limiter Based on the 123UN1A Microcircuit

Input voltage no more than	0.4 volts
Upper limiting frequency no more than	100 kilohertz
Clipping voltage at the output	0.8-2.0 volts

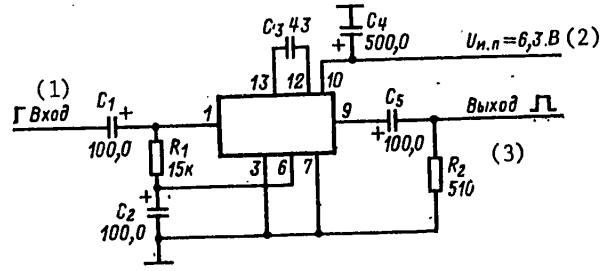


Figure 5-275. Diagram of a video amplifier based on the 123UN1A microcircuit

Key:
1. Input
2. $U_{p.s}$=6.3 volts
3. Output

Video Amplifier based on the 123UN1A Microcircuit

Input pulse amplitude no more than	0.4 volt
Input pulse polarity	Positive (negative)
Pulse duration no less than	10.0 microseconds
Repetition frequency no more than	50.0 kilohertz
Output pulse amplitude, no more than	2.2 volts
Output pulse polarity	Positive (negative)

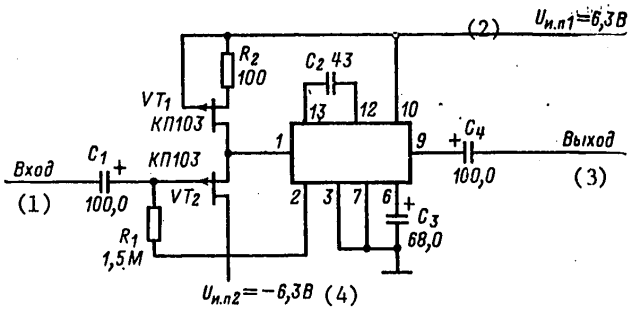


Figure 5-276. Diagram of a low-noise amplifier based on the 123UN1A microcircuit

Key:
1. Input
2. $U_{p.s1}$=6.3 volts
3. Output
4. $U_{p.s2}$=-6.3 volts

Low-Noise, Low-Frequency Amplifier Based on the 123UN1A Microcircuit

Input impedance no less than	1.5	megohms
Nonuniformity of the frequency-amplitude characteristic in the 20 hertz to 200 kilohertz range, no more than	1.5	decibels
Maximum output voltage, no less than	1.5	volts
Input capacitance, no more than	10.0	picofarads
Load resistance	500	ohms
Noise voltage in the frequency band 20 hertz to 200 kilohertz	3-30	microvolts

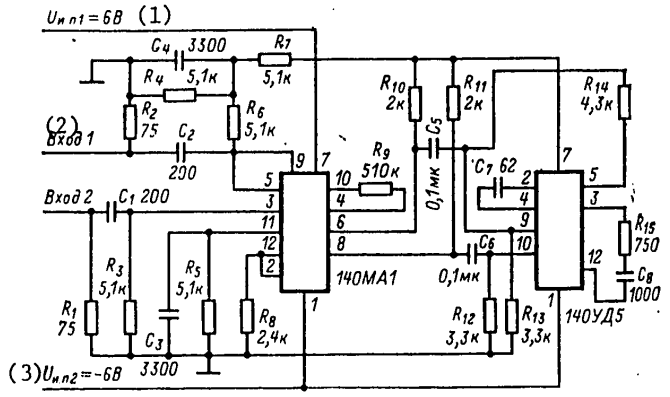


Figure 5-277. Diagram of a phase detector based on the 140MA1 and 140UD5 microcircuits

Key:
1. $U_{p.s1}$=6 volts
2. Input ...
3. $U_{p.s2}$=-6 volts

Phase Detector Based on 140MA1 and 140UD5 Microcircuits

Control signal voltage	150 millivolts
Reference signal voltage	50 millivolts
Input signal frequency (control and reference)	30 megahertz
Suppression coefficient of the input signal levels at the output, no less than	37 decibels
Steepness of the phase characteristic	100 millivolts/deg

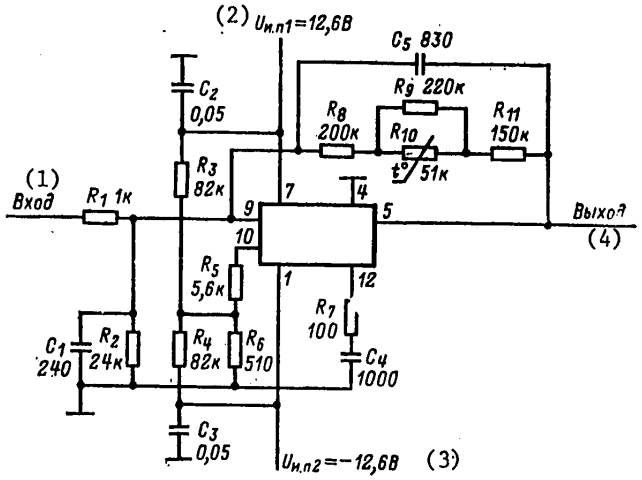


Figure 5-278. Diagram of a sawtooth voltage shaper based on the 140UD1B microcircuit

Key:
1. Input
2. $U_{p.s1}$=12.6 volts
3. $U_{p.s2}$=−12.6 volts
4. Output

Sawtooth Voltage Shaper Based on the 140UD1B Microcircuit

Working stroke duration	5-100 microseconds
Return stroke duration	2-10 microseconds
Harmonic coefficient no more than:	
for U_{out}=3.4 volts	1%
for U_{out}=6.0 volts	5%

Balance Modulator Based on 140MA1 Microcircuit

Maximum voltage at input 1	50 millivolts
Maximum voltage at input 2	200 millivolts
Control signal frequency	6 kilohertz
Reference signal frequency	60 kilohertz

Differentiating Amplifier Based on the 140UD1B Microcircuit

Input signal pulse duration	10 microseconds
Input pulse repetition frequency	10 kilohertz
Maximum output signal amplitude	+9.8 volts
	-7.2 volts

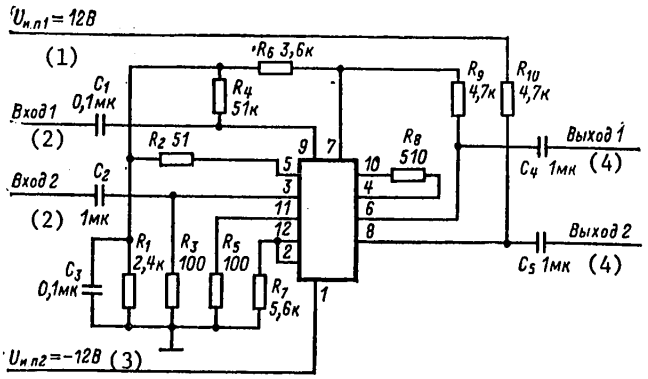


Figure 5-279. Diagram of a balance modulator based on the 140MA1 microcircuit

Key:
1. $U_{p.s1}$=12 volts
2. Input ...
3. $U_{p.s2}$=-12 volts
4. Output ...

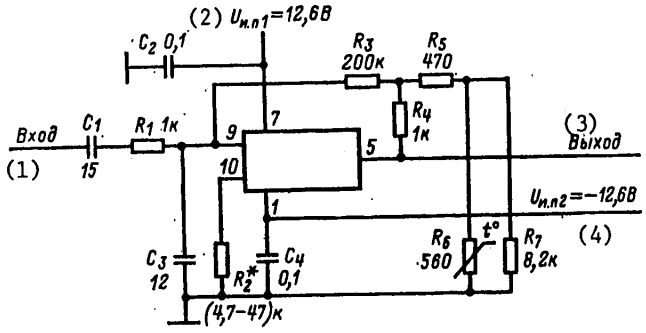


Figure 5-280. Diagram of a differentiating amplifier based on the 140UD1B Microcircuit.

Key:
1. Input
2. $U_{p.s1}$=12.6 volts
3. Output
4. $U_{p.s2}$=-12.6 volts

The resistor R_2 is selected for tuning the amplifier.

Output pulse duration (with respect to 0.5 level):	
positive	+0.55 microseconds
negative	-0.65 microseconds
Output pulse front duration:	
positive	0.13 microseconds
negative	0.3 microseconds
Output pulse decay time:	
positive	1.2 microseconds
negative	1.5 microseconds

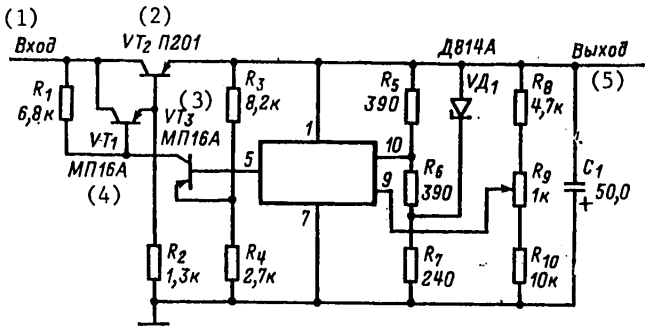


Figure 5-281. Voltage stabilizer circuit based on 140UD1B microcircuit

Key:
1. Input
2. VT_2P201
3. VT_3 MP16A
4. VT_1 MP16A
5. Output

Voltage Stabilizer Based on the 140UD1B Microcircuit

Input voltage U_{inp}	17-27 volts
Rated stabilized voltage U_{out}	12.6 volts
Range of regulation of stabilized voltage	11-14 volts
Stabilization accuracy	1%
Pulsation voltage for I_{out}=300 milliamps	5 millivolts

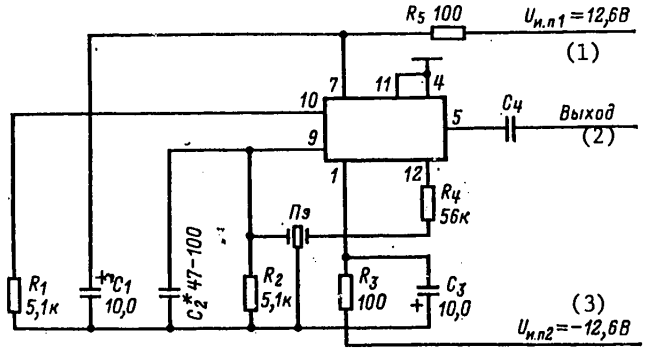


Figure 5-282. Diagram of a low-frequency oscillator based on the 140UD1B microcircuit

Key:
1. $U_{p.s1}$=12.6 volts
2. Output
3. $U_{p.s2}$=-12.6 volts

Low-Frequency Oscillator Based on the 140UD1B Microcircuit

Output voltage	7.0-9.0 volts
Output signal frequency	450 hertz
Instability of the input signal frequency	±10%
Output pulse duty factor	2±0.1

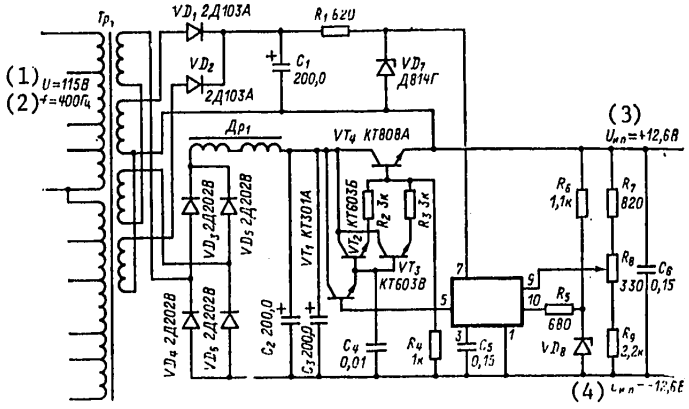


Figure 5-283. Diagram of a rectifier with voltage stabilizer based on 140UD1B microcircuit

Key:
1. U=115 volts
2. f=400 hertz
3. $U_{p.s}$=+12.6 volts
4. $U_{p.s}$=-12.6 volts

Rectifier with voltage stabilizer based on the 140UD1B Microcircuit

Stabilized output voltage	12.6 volts
Stabilization accuracy	1.0%
Pulsation voltage no more than	2.0 millivolts
Maximum load current	0.8 amps

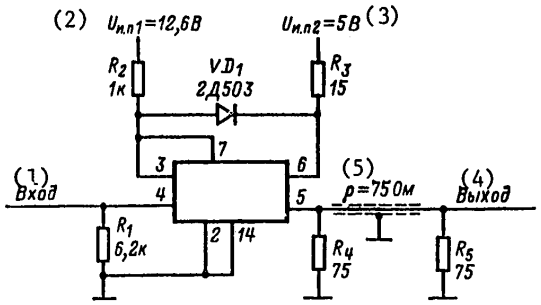


Figure 5-284. Diagram of an amplifier based on the 149KT1B microcircuit

Key:

1. Input
2. $U_{p.s1}$=12.6 volts
3. $U_{p.s2}$=5 volts
4. Output
5. ρ=75 ohms

Cable-Operating Amplifier Based on the 149KT1B Microcircuit

Input signal amplitude	3.0 volts
Input signal pulse duration	10.0 microseconds
Repetition frequency	10 kilohertz
Output pulse fall time no more than	1.0 microseconds
Output pulse front duration, no more than	0.5 microseconds
Output signal amplitude	2-4 volts

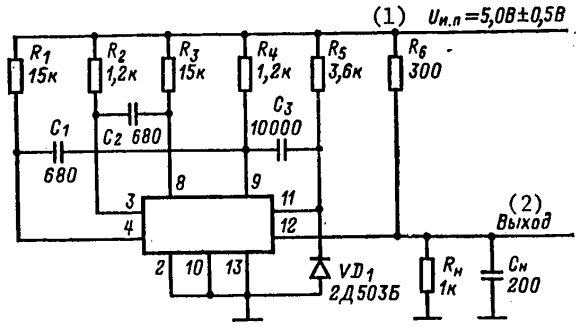


Figure 5-285. Diagram of a square pulse generator based on the 149KT1B microcircuit

Key:

1. $U_{p.s}$=5.0volts±0.5 volt; 2. Output

Square Pulse Generator Based on the 149KT1B Microcircuit

Output pulse amplitude	4.0 volts
Output pulse duration	2.5 microseconds
Output pulse front duration	0.3 microseconds
Output pulse decay time	0.2 microseconds
Pulse repetition frequency	130 kilohertz
Duty factor	3.0

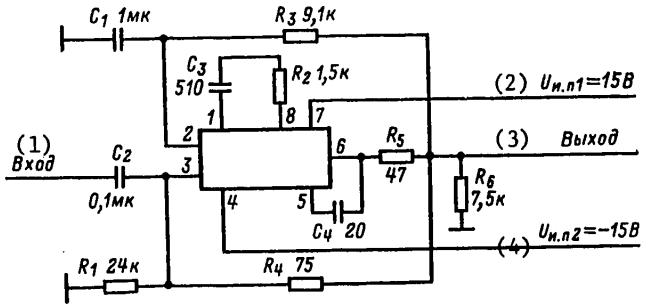


Figure 5-286. Diagram of a unistable multivibrator based on the M153UD1 microcircuit

Key:
1. Input
2. $U_{p.s1}$=15 volts
3. Output
4. $U_{p.s2}$=-15 volts

Diagram of a Unistable Multivibrator Based on the 153UD1 Microcircuit

It is possible to synchronize the operation of the circuit by feeding pulses to the input of the circuit through the capacitor C_2.

Output voltage scale, no less than	±10 volts
Output pulse repetition period	10,000 microseconds

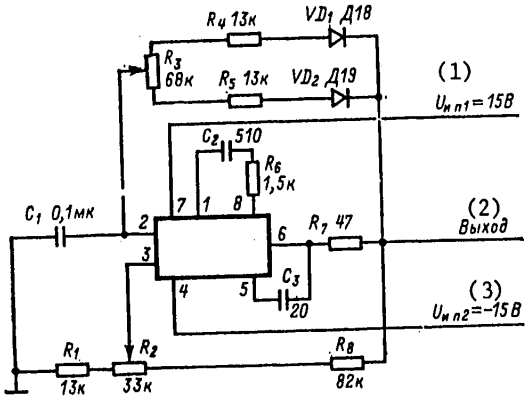


Figure 5-287. Diagram of a square pulse generator with regulated pulse duration based on the 153UD1 microcircuit

Key: 1. $U_{p.s1}$=15 volts; 2. Output; 3. $U_{p.s2}$=-15 volts

Diagram of a Square Pulse Generator with Regulatable Pulse Duration Based on the 153UD1 Microcircuit

The duration of the output pulses is regulated by using the resistor R_3. The output pulse repetition period is regulated by using the resistor R_2.

Scale of output voltage, no less than	±10 volts
Output pulse duration	250-1600 microseconds
Output pulse repetition period	1750-8000 microseconds

Video Signal Commutator Circuit Based on the 168KT2A Microcircuit

Video signals of positive polarity go to the inputs 3 and 5 of the 168KT2A microcircuit. The commutation of the switches is realized by feeding control voltages to the inputs 2, 6 and 9 of the microcircuits.

Input pulse amplitude	0.05-4.5 volts
Input pulse duration	0.1-250 microseconds
Control signal amplitude	±10 volts

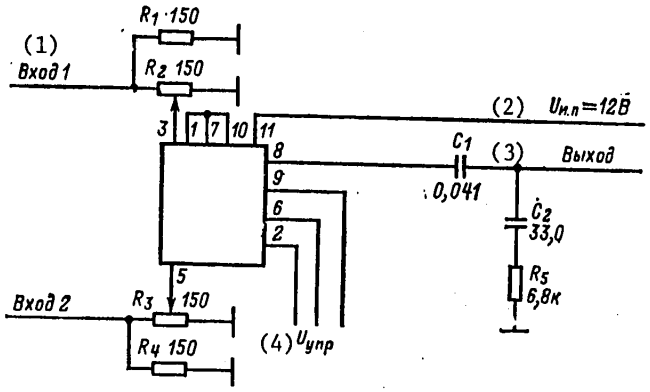


Figure 5-288. Diagram of a video signal commutator based on the 168KT2A microcircuit

Key:
1. Input ...
2. $U_{p.s}$=12 volts
3. Output
4. $U_{control}$

Gain	0.7-0.8
Pass band	10.0 millihertz
Dynamic range	30 decibels

Cable Amplifier Based on K170AA3 Microcircuit

This circuit operates on a coaxial cable with wave impedance of 75 to 100 ohms and cable length to 70 meters.

The admissible load distributed along the communication line or lumped at the end of the communication line is no more than 15 inputs of the TTL-circuits of the 133LA1 type with insurance of a pulse amplitude on the matching resistance of 2.4 volts; here the current load is approximately 8 milliamps.

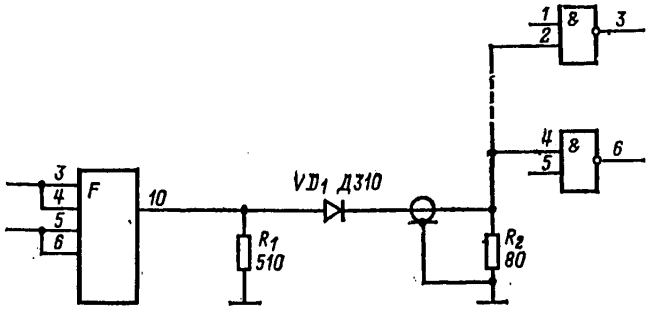


Figure 5-289. Diagram of a cable amplifier based on the K170AA3 microcircuit

The magnitude of the matching resistance R_3 when operating on the RK15, RK100 cable and a load of 15 inputs of TTL-circuits will be 80-120 ohms.

Display Circuit Based on the K170AA1 Microcircuit

The input control is realized from the series K133 (K155) TTL-circuits.

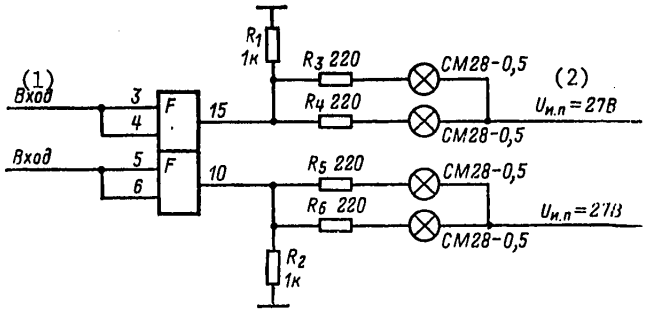


Figure 5-290. Display circuit based on the K170AA1 microcircuit

Key:
1. Input
2. $U_{p.s}$=27 volts

In the operating state a current on the order of 80 milliamps flows through the open output transistor of the shaper.

Logarithmic Intermediate Frequency Amplifier Stage Based on the 228UV2 Microcircuit

In this circuit diagram the microcircuit performs the functions of an amplifier-limiter and detector.

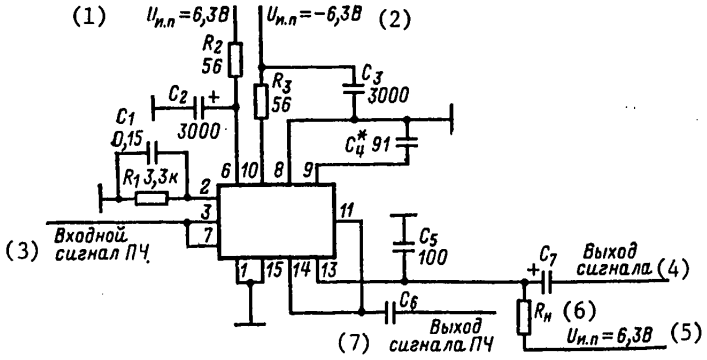


Figure 5-291. Diagram of an intermediate frequency amplifier stage with logarithmic transient characteristic based on the 228UV2 microcircuit

Key:
1. $U_{p.s}$=6.3 volts
2. $U_{p.s}$=-6.3 volts
3. Intermediate frequency input signal
4. Signal output
5. $U_{p.s}$=6.3 volts
6. R_{load}
7. Intermediate frequency signal output

Amplification coefficient no less than	5
Upper limiting frequency at the 0.7 level no less than	80 megahertz
Central frequency	30-80 megahertz*
Video signal polarity	Negative

*The capacitance C_4 corresponds to frequency of 60 megahertz.

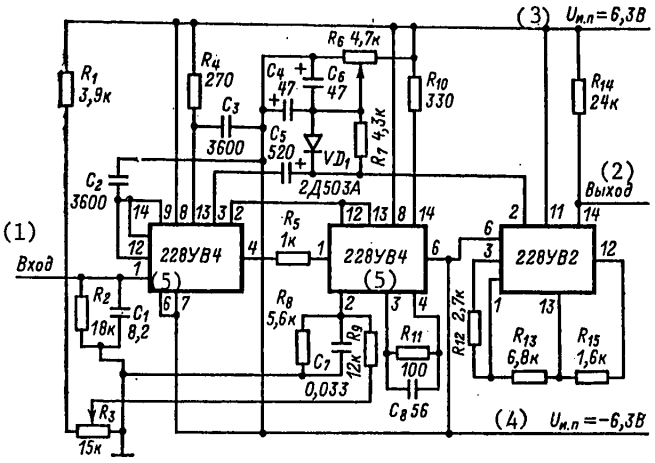


Figure 5-292. Diagram of a pulse shaper based on the 228UV4 and 228UV2 microcircuits

Key:

1. Input
2. Output
3. $U_{p.s}$=6.3 volts
4. $U_{p.s}$=-6.3 volts
5. 228UV4

Pulse Shaper Based on 228UV2 and 228UV4 Microcircuits

Parameters of input pulses of positive polarity:	
Amplitude	0.5-2 volts
Duration	0.1 microsecond to 1 millisecond
Repetition frequency	10 hertz to 100 kilohertz
Amplitude of output pulses of positive polarity, no less than	3.0 volts

Emitter Repeater Based on 228UV4 Microcircuit

Lower limiting frequency f_{low}	3 megahertz
Upper limiting frequency f_{upper}	30 megahertz
Gain	0.92 to 1.0
Input impedance, no more than	120 ohms

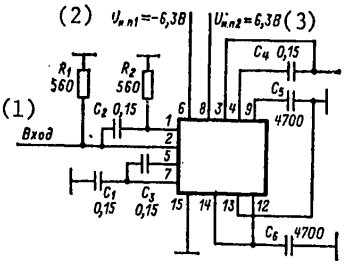


Figure 5-293. Diagram of an emitter repeater based on the 228UV4 microcircuit

Key:

1. Input
2. $U_{p.s1}$=-6.3 volts
3. $U_{p.s2}$=6.3 volts

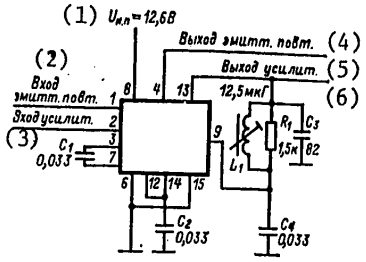


Figure 5-294. Diagram of an emitter repeater and amplifier based on the 228UV4 microcircuit

Key:

1. $U_{p.s}$=12.6 volts
2. Emitter repeater input
3. Amplifier input
4. Emitter repeater output
5. Amplifier output
6. 12.5 microhertz

Emitter Repeater and Amplifier Based on the 228UV4 Microcircuit

Input signal amplitude of emitter repeater	150-200 millivolts
Input signal frequency of emitter repeater	5.0 megahertz
Input signal amplitude of amplifier, no less than	20 millivolts
Input signal frequency of amplifier	5.0 megahertz

APPENDIX

Table P1-1. Graphical Symbols for Logical Elements

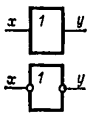
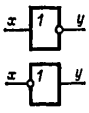
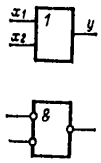
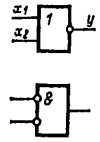
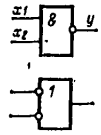
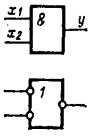
Name	Truth table	Symbols
Repeater Logically equivalent form	x y 0 0 1 1	
NOT (inverter) Logically equivalent form	x y 0 1 1 0	
OR (disjunctor)[1] Logically equivalent form	x_1 x_2 y 0 0 0 0 1 1 1 0 1 1 1 1	
OR-NOT (Pierce element)[1] Logically equivalent form	x_1 x_2 y 0 0 1 0 1 0 1 0 0 1 1 0	
AND (conjunctor)[1] Logically equivalent form	x_1 x_2 y 0 0 0 0 1 0 1 0 0 1 1 1	
AND-NOT (Scheffer element)[1] Logically equivalent form	x_1 x_2 y 0 0 1 0 1 1 1 0 1 1 1 0	

Table P1-1 (continued)

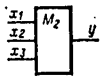
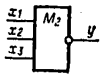
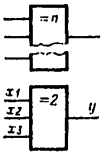
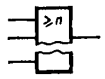
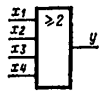
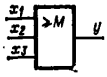
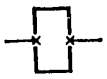
Name	Truth table	Symbols
Mod 2 addition (oddness)[1]	x_1 x_2 x_3 y 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1 1	
Mod 2 addition with negation (evenness)[1]	x_1 x_2 x_3 y 0 0 0 1 0 0 1 0 0 1 0 0 0 1 1 1 1 0 0 0 1 0 1 1 1 1 0 1 1 1 1 0	
Equivalence[1]	x_1 x_2 x_3 y 0 0 0 1 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1	
Exclusive OR ("1 and only 1")	x_1 x_2 x_3 y 0 0 0 0 0 0 1 1 0 1 0 1 0 1 1 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1 0	
"n" and only "n"[2]. General designation	x_1 x_2 x_3 y 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 1 1 0 0 0 1 0 1 1 1 1 0 1 1 1 1 0	

Table P1-1 (continued)

Name	Truth table	Symbols
Logical threshold[3], General designation	x_1 x_2 x_3 x_4 y 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 1 1 0 1 0 0 0 0 1 0 1 1 0 1 1 0 1 0 1 1 1 1 1 0 0 0 0 1 0 0 1 1 1 0 1 0 1 1 0 1 1 1 1 1 0 0 1 1 1 0 1 1 1 1 1 0 1 1 1 1 1 1	 
Majoritalness[4]	x_1 x_2 x_3 y 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 1 1 0 0 0 1 0 1 1 1 1 0 1 1 1 1 1	
Leads not carrying logical information	—	

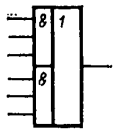
[1]The number of inputs can be any number greater than one.

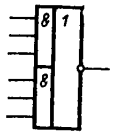
[2]The number of inputs is any number greater than one; n is a natural number not exceeding the number of inputs of the logical element, for example, the element "2 and only 2."

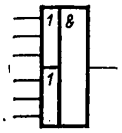
[3]The number of inputs is any number greater than one; n is a natural number not equal to one, less than the total number of inputs of the elements, for example, the logical threshold two out of four variables.

[4]The number of inputs can be any odd number greater than one, for example, three.

Some examples of the symbols for combination logical elements with equivalent inputs follows:

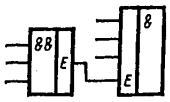
AND-OR 

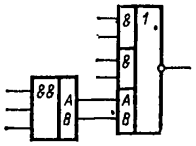
AND-OR-NOT 

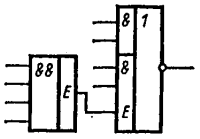
OR-AND 

Note. The number of inputs and groups can be any number.

Some examples of the representation of functional expanders follow:

The AND functional expander for AND expansion (single-terminal connection of the expander) 

Functional expander AND for OR expansion (two-terminal connection of the expander) 

Functional expander AND for AND expansion of a group of inputs (single-terminal connection of the expander) 

Note. For representation of the functional expanders and logical elements to which the expanders are connected by the separated method, the expander function symbol indicates the following: a) operation performed on the input variables of the expander, for example AND; b) function performed by the basic element on the result of the expander operation, for example, OR.

Labels Indicating the Functional Purposes of Trigger Inputs.

The input for separate setting of a trigger to the logical one state (S-input)	S*
Input for separate setting of a trigger to the logical zero state (R-input)	R
Input for setting the logical one state in a universal JK-trigger (J-input)	J
Input for setting the logical zero state in a universal JK-trigger (K-input)	K

Complementing input (T-input) T**

Information input for setting a trigger to the logical one and logical zero states (D-input) D

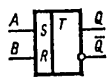
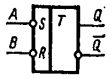
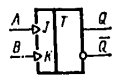
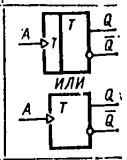
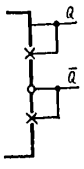
Preparatory control inputs for permitting information reception (V-input) V

Control (command) servoinput for information reception. Synchronization input (C-input) C*

*When necessary, numbers can be added to the letters, for example, S1, S2, C1, C2, C3, and so on.

**If the trigger has only one complementing input, the T label can be omitted.

Table P1-2. Symbols for elementary asynchronous triggers

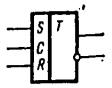
Name	Table of states[1]	Symbols[2]
RS-trigger with direct input (with separate setting of "0" and "1" states)	A B Q 0 0 Q* 0 1 0 1 0 1 1 1 H/O	
RS-trigger with inverse inputs	A B Q 0 0 H/O 0 1 1 1 0 0 1 1 Q*	
JK-trigger	A B Q 0 0 Q* 0 1 0 1 0 1 1 1 $\bar{Q}$*	
T-trigger (trigger with complementing input)	A Q 0 Q* 1 $\bar{Q}$*	
Connection to the trigger outputs of internal load resistors		

[1]The following notation is used in the table of states: Q* — storage of the trigger state; $\bar{Q}$* — changing the trigger state to the opposite; H/O — trigger state undefined.

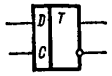
[2]The logical zero output differs from the one ouput by the logical negation indicator ($\bar{Q}$). The logical indicator at the trigger input indicates for what value of the logical variable a defined action is taken on the trigger state.

Examples of Symbols for synchronous triggers with Static Control*

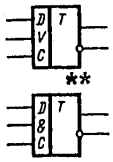
RS-trigger



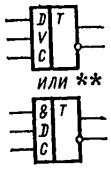
D-trigger



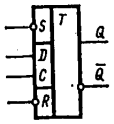
DV-trigger (controlling input AND coupled)



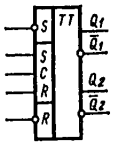
DV-trigger (information inputs AND coupled)



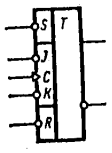
DRS-trigger with asynchronous S and R-inputs



Two-step synchronous RS-trigger with asynchronous S and R-inputs and with outputs from the first and second steps



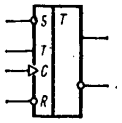
JKRS-trigger with dynamic C-input



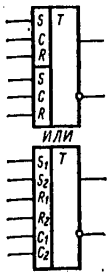
*The value of the binary valuable at the static input is received at all times that the signal at this input is in a defined state.

**OR

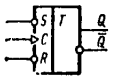
RST-trigger with synchronizing complementing input C and asynchronous S and R-inputs

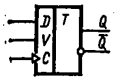


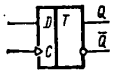
Synchronous RS-trigger controlled by two series of synchronizing signals

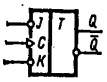


Examples of the Conventional Symbols Used for Synchronous Triggers with Dynamic Servocontrol (Synchronizing) Input*

RS-trigger 

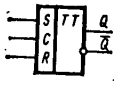
DV-trigger 

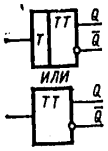
D-trigger 

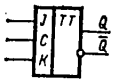
JK-trigger 

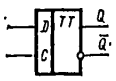
*The value of the binary variable at the dynamic input is received only in time intervals when the signal at this input varies in a defined way. In contrast to the static input the dynamic input is denoted by a triangle.

Examples of the Symbols for Triggers Constructed by the Principle of Two-Step Information Storage

RS-trigger 

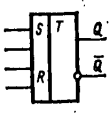
T-trigger 

JK-trigger 

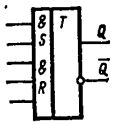
D-trigger 

Examples of Symbols for Triggers with Complex Input Logic

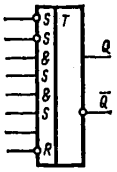
Asynchronous RS-trigger. Input in the S and R groups are OR coupled (disjunctively)



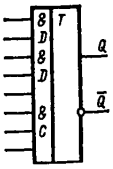
Asynchronous RS-trigger. Inputsin the S and R-groups are AND coupled (conjunctively)



Asynchronous RS-trigger having two groups of inverse S-inputs OR coupled, two groups of direct S-inputs AND coupled and one inverse R-input



D-trigger
D-inputs AND-OR coupled
C-inputs AND coupled



Symbols for the Inputs and Outputs of Decoders, Coders, Halfadders, Adders, Code Converters and Registers

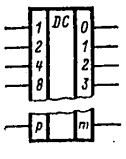
Information read input	C*
Shift input	D*
Mod 2 output	M2
"0" state setting input	R
Halfadder output, adder input or register input "mod 2 sum"; "1" state setting input	S*
Carry	P
Information reception separation input	V
Summing complementing input	+1

Coder inputs, decoder inputs and outputs are labeled by numbers depicting the code combinations: 0, 1, 2...
Coder outputs are labeled by numbers depciting binary weights: 1, 2, 4, 8.
Inputs and outputs of the code converters are denoted by arabic numbers or Latin letters.
The graphical symbols for the forward and inverse inputs and outputs of complex logical elements are distinguished by the same methods as for simpler logical elements.

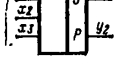
*Used jointly with numerical indices in the symbols for registers and counters.

Some examples of the construction of the graphical notation for complex logical elements are presented:

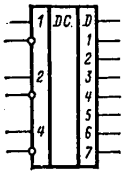
Decoder, general disignation $P = 2^{n-1}$; $m = 2^{n-1}$, where n is the number of binary bits of the decoded code



Single-bit combination adder $y_1 =$
$= x_1x_2x_3 + x_1\bar{x}_2\bar{x}_3 +$
$+ \bar{x}_1x_2\bar{x}_3 + \bar{x}_1\bar{x}_2x_3$
$y_2 = x_1x_3 + x_2x_3 +$
$+ x_1x_2$



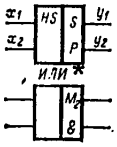
Decoder with paraphase inputs



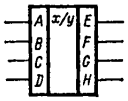
Halfadder

$y = x_1\bar{x}_2 + \bar{x}_1x_2$

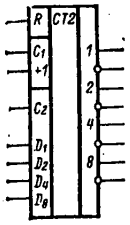
$y_2 = x_1x_2$



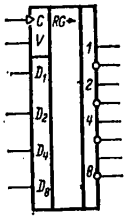
Code converter



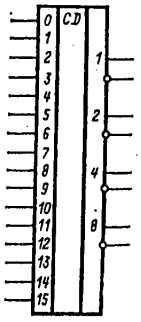
Binary counter with two-cycle synchronization, the possibility of setting the code and asynchronous input for setting the counter to the logical 0 state



Shift register



Coder



APPENDIX 2. Conversion Table for the Identification Codes of Microcircuits, the Information about Which is Included in this Handbook

Identification code by the standard in effect before introduction of the GOST*	Identification codes after introduction of GOST* 18682-73	Identification code by the standard in effect before introduction of the GOST*	Identification codes after introduction of GOST* 18682-73
	Digital integrated microcircuits		
1LI091	109LI1	K1IL141B	K114IL1B
K1LI091A	K109LI1A	K1IR141A	K114IR1A
K1LI091B	K109LI1B	1IR141B	K114IR1B
1LP141A	114LP1A	k1TR141A	K114TR1A
1LP141B	114LP1B	K1TR141B	K114TR1B
1LP142A	114LD1A	1LB151	115LYe1
1LP142B	114LD1B	1LB152	115LYe2
1LP143A	114LP2A	1LB153	115LYe0
1LP143B	114LP2B	1LB154	115LYe4
1LP144A	114LP3A	1LP151	115LP1
1LP144B	114LP3B	1LS151	115LS1
1LP145A	114LD2A	1TR151	115TR1
1LP145B	114LD2B	K1LB151	K115LYe1
1LB141A	114LYe1A	K1LB152	K115LYe2
1LB141B	114LYe1B	K1LB153	K115LYe3
1LB142A	114LL1A	K1LB154	K115LYe4
1LB142B	114LL1B	K1LP151	K115LP1
1LB143A	114LL2A	K1LS151	K115LS1
1LB143B	114LL2B	K1TR151	K115TR1
1IL141A	114IL1A	1LB211A	121LA1A
1IL141B	114IL1B	1LB211B	121LA1B
1IR141A	114IR1A	1LB211V	121LA1V
1IR141B	114IR1B	1LB211G	121LA1G
1TR141A	114TR1A	1LB212A	121LA2A
1TR141B	114TR1B	1LB212B	121LA2B
K1LP141A	K114LP1A	1LP211	121LD1
K1LP141B	k114LP1B	K1LB211A	K121LA1A
K1LP142A	K114LD1A	K1LB211B	K121LA1B
K1LP142B	K114LD1B	K1LB211V	K121LA1V

*All-Union State Standard

Identification code by the standard in effect before introduction of the GOST	Identification codes after introduction of GOST 18682-73	Identification code by the standard in effect before introduction of the GOST	Identification codes after introduction of GOST 18682-73
K1LP143A	K114LP2A	K1LB211G	K121LA1G
K1LP143B	K114LP2B	K1LB212A	K121LA2A
K1LP144A	K114LP3A	K1LB212B	K121LA2B
K1LP144B	K114LP3B	K1LP211	K121LD1
K1LP145A	K114LD2A	1LS281A	128LS1A
K1LP145B	K114LD2B	1LS282B	128LS1B
K1LB141A	K114LYe1A	1LS281V	128LS1V
K1LB141B	K114LYe1B	1LR281A	128LR1A
K1LB142A	K114LL1A	1LR281B	128LR1B
K1LB142B	K114LL1B	1LR281V	128LR1V
K1LB143A	K114LL2A	1LP281	128LD1
K1LB143B	K114LL2B	K1LS281A	K128LS1A
K1IL141A	K114IL1A	K1LS281B	K128LS1B
K1LS281V	K128LS1B	K1LR331	K133LR1
K1LR281A	K128LR1A	K1LR333	K133LR3
K1LR281B	K128LR1B	K1LR334	K133LR4
K1L281V	K128LR1V	K1LP331	K133LD1
K1LP281	K128LD1	K1LP333	K133LD3
1LB301	130LA1	K1TK331	K133TV1
1LB302	130LA2	1LB341A	134LB1A
1LB303	130LA3	1LB341B	134LB1B
1LB304	130LA4	1LB343A	134LB2A
1LB306	130LA6	1LB342B	134LB2B
1LR301	130LR1	1LB343A	134LA8A
1LR303	130LR3	1LB343B	134LA8B
1LR304	130LR4	1LB344A	134LA2A
1LP301	130LD1	1LB344B	134LA2B
1TK301	130TV1	1LR341A	134LR1A
K1LB311	K131LA1	1LR341B	134LR1B
K1LB312	K131LA2	1LR342A	134LR2A
K1LB313	K131LA3	1LR342B	134LR2B
K1LB314	K131LA4	1LR343A	134LR4A
K1LB316	K131LA6	1LR343B	134LR4B
K1LP311	K131LD1	1ZhL341	134KhL3
K1LR311	K131LR1	1TK342	134TV1
K1LR313	K131LR3	1TK343	134TV14
K1LR314	K131LR4	1TK344A	134TM2A
K1TK311	K131TV1	1TK344B	134TM2B
1LB331	133LA1	K1LB341	K134LB1
1LB332	133LA2	K1LB342	K134LB2
1LB333	133LA3	K134LB3	K134LA8
1LB334	133LA4	K134LB4	K134LA2
1LB336	133LA6	K1LR341	K134LR1
1LB337	133LA7	K1LR342	K134LR2
1LR338	133LR8	K134LR3	K134LR4

Identification code by the standard in effect before introduction of the GOST	Identification codes after introduction of GOST 18682-73	Identification code by the standard in effect before introduction of the GOST	Identification codes after introduction of GOST 18682-73
1LR331	133LR1	K1ZhL341	K134KhL3
1LR333	133LR3	K1TK342	K134TV1
1LR334	133LR4	K1TK343	K134TV14
1LP331	133LD1	K134TK4	K134TM2
1LP333	133LD3	1LB361	136LA1
1TK331	133TV1	1LB362	136LA2
1TK332	133TM2	1LB363	136LA3
K1LB331	K133LA1	1LB364	136LA4
K1LB332	K133LA2	1LR361	136LRL
K1LB333	K133LA3	1LR363	136LR3
K1LB334	K133LA4	1LR364	136LR4
K1LB336	K133LA6	1TK361	136TV1
K1LB337	K133LA7	K1LB361	K136LA1
K1LB338	K133LA8	K1LB362	K136LA2
K1LB363	K136LA3	K1TK551	K155TV1
K1LB364	K136LA4	K1TK552	K155TM2
K1LR361	K136LR1	K1ZhL551	K155AP1
K1LR363	K136LR3	K1IYe551	K155IYe1
K1LR364	K136LR4	1PM561A	156AG1A
K1TK361	K136TV1	1PM561B	156AG1B
K1LB371	K137LM1	1PM561V	156AG1V
K1LB3719	K137LM2	1UP561A	156LA6A
K1LB372	K137LYe1	1UP561B	156LA6B
K1LB379	K137LYe2	1LB561A	156LA4A
K1LB375	K137LM3	1LB561B	156LA4B
K1LB376	K137LM4	1LB561V	156LA4V
K1LB3717	K137LM5	1LB562	156LA1
K1LP371	K137LD1	1LB563A	156LA2A
K1LP372	K137LD2	1LB563A	156LA2B
K1IL371	K137IL1	1LB563B	156LA2V
K1IL372	K137IL2	1LB564A	156LD1A
KITR371	K137TR1	1LB564B	156LD1B
K1TR374	K137TM1	1LB564V	156LD1V
K1IR441	K144IR1	1LB566A	156LA5A
1LB551	155LA1	1LB566B	156LA5B
1LB552	155LA2	1LP561	156LD3
1LB553	155LA3	K1LB581	K158LA1
1LB554	155LA4	K1LB582	K158LA2
1LB556	155LA6	K1LB583	K158LA3
1LB557	155LA7	K1LB584	K158LA4
1LB558	155LA8	K1LR581	K158LR1
1LR551	155LR1	K1LR583	K158LR3
1LR553	155LR3	K1LR584	K158LR4
1LR554	155LR4	K1TK581	K158TV1
1LP551	155LD1	K1LB721	K172LM1
1LP553	155LD3	K1LB722	K172LM2

Identification code by the standard in effect before introduction of the GOST	Identification codes after introduction of GOST 18682-73	Identification code by the standard in effect before introduction of the GOST	Identification codes after introduction of GOST 18682-73
1TK551	155TV1	K1LI721	K172LI1
ITK552	155TM2	K1LR721	K172LK1
K1LB551	K155LA1	K1TR721	K172TR1
K1LB552	K155LA2	1LB781	178LM1
K1LB553	K155LA3	1LB782	178LM2
K1LB554	K155LA4	1LI781	178LI1
K1LB556	K155LA6	1LR781	178LK1
K1LB557	K155LA7	1TR781	178TR1
K1LB558	K155LA8	K1LB781	K178LM1
K1LR551	K155LR1	K1LB782	K178LM2
K1LR553	K155LR3	K1LI781	K178LI1
K1LR554	K155LR4	K1LR781	K178LK1
K1LP551	K155LD1	K1TR781	K178TR1
K1LP553	K155LD3	K1LB873	K187LM1A
K1LB8711	K187LM1B	2LB041	204LB1
K1LB874	K187LYe1A	2LB042	204LB2
K1LB8713	K187LYe1B	2NK041	204NK1
K1LB877	K187LM2A	2LI041	204LN1
K1LB8715	K187LM2B	K2TK041	K204TK1
K1LP871	K187LD1A	K2LB041	K204LB1
K1LP872	K187LD1B	K2LB042	K204LB2
K1TR872	K187TM1A	K2NK041	K204NK1
K1TR875	K187TM1B	K2LI041	K204LI1
1YaM881	188RM1	2NK051	205LP1
2LB011	201LB1	2LB051	205LYe1
2LB012	201LB2	2LB052	205LYe2
2LB013	201LB3	2LB053	205LYe3
2LB014	201LB4	2LN051	205LN1
2LB015	201LB5	2TS051	205LR1
2LB016	201LB6	2LB101	210LA1
2LB017	201LB7	2LB102	210LYe2
2LS011	201LS1	K2LB101	K210LA1
2NT011	201NT1	K2LB102A	K210LYe2B
2NT012	201NT2	K2LB102B	211LYe2A
2NT013	201NT3	2LB111	K210LYe2B
K2LB011	K201LB1	2LB112	211LYe1
K2LB012	K201LB2	2LB113	211LYe2
K2LB013	K201LB3	2LB114	211LYe4
K2LB014	K201LB4	2LB115	211LYe5
K2LB015	K201LB5	2LB116	211LYe6
K2LB016	K201LB6	2LB117	211KhL1
K2LB017	K201LB7	2LB118	211KhL2
K2LS011	K201LS1	2LB119	211KhL3
K2NT011	K201NT1	2LB1110	211LYe10
K2NT012	K201NT2	2LB1111	211LYe11
K2NT013	K201NT3	2LB1112	211LYe12

Table continued

2LN021	202LN1	2LN111	211LN1
2LN022	202LN2	2LN112	211LN2
2UI021	202UI1	2LN113	211LN3
2LS021	202LS1	2LN114	211LN4
2LS022	202LS2	2LN115	211LN5
2LS023	202LS3	2LN116	211LN6
2LS024	202LS4	2IR111	211IR1
2LS025	202LS5	2IR112	211IR2
2LS026	202LS6	2IYe111	211IYe
2LP021	202NK1	2IYe112	211IYe2
2LP022	202NK2	2TR111	211KHL4
2ND021	202ND1	2TR112	211KhL5
2ND022	202ND2	2TR113	211KhL6
2TK041	202TK1	2TR114	--
--	215LN1	2LN182	218LN2
2LS151	215LS1	2LN183	218Ln3
2LS152	215LS2	2TK181	218TK1
2UI151	215UI1	K2LB181	K218LB1
2PN151	215PN1	K2LN181	K218LN1
2PN152	215PN2	K2LN182	K218LN2
2LB171A	217LB1A	K2LN183	K218LN3
2LB171B	217LB1B	K2TK181	K218TK1
2LB172A	217LB2A	2TR211	221TR1
2LB172B	217LB2A	2LN211	221LN1
2LB173	217LB3	2LB211	221LA1
2LB173A	217LB3A	2LR211	221LR1
2LB174A	217LB4A	2LP211	221LP1
2LB174B	217LB4B	2LB231	223LYe1
2LR171	217LR1	2LB232	223LM1
2TK171A	217TK1A	2LB233	223LYe2
2TK171B	217TK1B	2IYe231	223IYe1
2TR171A	217TR1A	2ID231	223ID1
2TR171B	217TR1B	2IL231	223IL1
2NT171	217NT1	2TR231	223TR1
2NT172	217NT2	2TK231	223TK1
2NT173	217NT3	K2LB231	K223LY21
2LP171	217LD1	K2LB232	K223LM1
2LP172	217LD2	K2LB233	K223LYe2
2LP173	217NK1	K2Iye231	K223IYe1
K2LB171A	K217LB1A	K2ID231	K223ID1
K2LB171B	K217LB1B	K2IL231	K223IL1
K2LB172A	K217LB2A	K2TR231	K223TR1
K2LB172B	K217LB2B	K2TK231	K223TK1
K2LB173	K217LB3	2TK291A	229TK1A
K2LB173A	K217LB3A	2TK291B	229TK1B
K2LB174A	K217LB4A	2IL291	229IL1
K2LB174B	K217LB4B	2IL281	229ID1
K2LR171	K217LR1	2ZhL291	229LM4
K2TK171A	K217TK1A	K2TK291A	K229TK1A
K2TK171B	K217TK1B	K2TK291B	K229TK1B
K2TR171A	K217TR1A	K2IL291	K229IL1
K2TR171B	K217TR1B	K2ID291	K229ID1

Table continued

K2NT171	K217NT1	K2ZhL291	K229LM4
K2NT172	K217NT2	2IYe301A	230IYe1A
K2NT173	K217NT3	2IYe301A	230IYe1B
K2LP171	K217LD1	2IYe302A	230IYe2A
K2LP172	K217LD2	2IYe302B	230IK2B
K2LP173	K217LD3	2IYe303A	230IYe3A
2LB181	218LB1	2IYe303B	230IYe3B
2LN181	218LN1	2IR301A	230IR1A
2IR201B	230IR1B	2IL401B	240IL1B
2IR302A	230IR2A	2IS401A	240IM1A
2IR302B	240IR2B	2IS401B	240IM1B
2IP301P	230IP1A	2IYe401B	240IYeB
2PK301	230IK1	2IYe401V	240IYe1V
K2IYe301A	K230IYe1A	2LP401	240LD1
K2IYe301B	K230IYe1B	2LB431	243LA1
K2IYe302A	K230IYe2A	2LB432	243LA2
K2IYe302B	K230IYe2B	2LB433	243LA3
K2IY2303A	K230IYe3A	2LB434	243LA4
K2IYe303B	K230IYe2B	2LB435	243LA5
K2IR301A	K230IR1A	2LB436	243LA6
K2IR301B	K230IR1B	2LN431	243LN1
K2IR302A	K230IR2A	2LN432	243LN2
K2IR302B	K230IR2B	2LN433	243LN3
K2IPs01A	K230IP1A	2YaP431	243RP1
K2PK301P	K230IK1A	2UP431	243UP1
2IYe311	231IYe1	2UP432	243UM1
2LB401A	240LA1A	2UI431	243UL1
2LB401B	240LA1B	2UI432	243UL2
2LB401V	240LA1V	2UI433	243UL3
2LB402	240LA2	2LI431	243LP1
2LB403A	240LA3A	2LI432	243LP2
2LB403B	240LA3B	2LP431	243LD1
2LB403V	240LA3V	2NT431	243NT1
2LB404A	240LA4A	2NT432	243NT2
2LB404B	240LA4B	2NT433	243NT3
2LB404V	240LA4V	K2LB431	K243LA1
2LB405	240LA5	K2LB432	K243LA2
2LB406A	240LA6A	K2LB433	K243LA3
2LB406B	240LA6B	K2LB434	K243LA4
2LB406V	240LA6V	K2LB435	K243LA5
2IR401A	240IR1A	K2LB436	K243LA6
2IR401B	240IR1B	K2LN431	K243LN1
2I402A	240IR2A	K2LN432	K243LN2
2IR402B	240IR2B	K2LN433	K243LN3
2IR403A	240IR3A	K2YaP431	K243RP1
2IR403B	240IR3B	K2UP431	K243UP1
2IL401A	240IL1A		

Analog integrated microcircuits

1KT011A	101KT1A	K1KT011B	K101KT1B
1KT011B	101KT1B	K1KT011V	K101KT1V
1KT011V	101KT1V	K1KTo11G	K101KT1G

Table continued

1KT011G	10KT1G	K1UT101A	K101UT1A
K1KT011A	K101KT1A	K1UT101B	K101UT1B
K1US181A	K118UN1A	K1SS191A	K119SS1A
K1US181B	K118UN1B	K1SS191B	K119SS1B
K1US181V	K118UN1V	K1SS192	K119SS2
K1US181G	K118UN1G	K1SV191	K119Sv1
K1US181D	K118UN1D	K1US191	K119UN1
K1US182A	K118UN2A	K1US192	K119UN2
K1US182B	K118UN2B	K1UT191	K119UT1
K1US182V	K118UN2V	K1KP191	K119KP1
K1TSh181A	K118TLA	K1UE191	K119UYe1
K1TSh181B	K118TLB	K1UB191	K119UP1
K1TSh181V	K118TLV	1US231A	123UN1A
K1TSh181G	K118TLG	1US231B	123UN1B
K1TSh181D	K118TLD	1US231V	123UN1V
K1UB181A	K118UP1A	K1US231A	K1US231A
K1UB181B	K118UP1B	K1US231B	KUS231B
K1UB181V	K118UP1V	K1US231V	K1US231V
K1UB181G	K118UP1G	1KT241A	124KT1A
K1UT181A	K118UD1A	1KT241B	124KT1B
K1UT181B	K118UD1B	K1KT241	K124KT1
K1UT181V	K118UD1V	1NT291A	129NT1A-1
1DA191A	119DA1A	1NT291B	129NT1B-1
1DA191B	119DA1B	1NT291V	129NT1V-1
1GF191	119AG1	1NT291G	129NT1G-1
1GF192A	119GG1A	1NT291D	129NT1D-1
1GF192B	119GG1B	1NT291Ye	129NT1Ye-1
1GF192V	119GG1V	1NT291Zh	129NT1Zh-1
1TSh191	119TL1	1NT291Z	129NT1Z-1
1MA191A	119MA1A	1NT291I	129NT1I-1
1MA191B	119MA1B	K1NT291A	K129NT1A
1PP191	119PP1	K1NT291B	K129NT1B
1SS191A	119SS1A	K1NT291V	K129NT1V
1SS191B	119SS1B	K1NT291G	K129NT1G
1SS192	119SS2	K1NT291D	K129NT1D
1SV191A	119SV1A	K1NT291I	K129NT1I
1SV191B	119SV1B	1UT401A	140UD1A
1US191	119UN1	1UT401B	140UD1B
1US192	119UN2	1UT402	140UD2
1UT191	119UT1	--	140UD5A
1UE191	119UYe1	--	140UD5B
1KP191	119KP1	--	140UD6A
1UB191	119UP1	--	140UD6B
K1DA191	K119DA1	--	140UD7
K1GF191	K119AG1	--	140UD8A
K1TSh191	K119TL1	--	140UD8B
K1MA191	K119MA1	--	140UD9
K1PP191	K119PP1	--	140UD13
--	140UD14	--	K153UD2
--	140MA1A	--	K153UD5
--	140MA1B	1NT591A	159NT1A

Table continued

--	140KhA1	1NT591B	159NT1B
K1UT401A	K140UD1A	1NT591V	159NT1V
K1UT401B	K140UD1V	1NT491D	159NT1G
K1UT401V	K140UD1V	1NT591D	159NT1D
K1UT402A	K140UD2A	1NT591Ye	159NT1Ye
K1UT402B	K140UD2B	1NT591Zh	159NT1Zh
--	K140UD5A	K1NT591A	K1NT591A
	K140UD5B	k1NT591B	k1NT491B
	K140UD6	K1NT591V	K1NT591V
	K140UD7	K1NT491G	K1NT591G
	K140UD8A	K1NT591D	K1NT591D
	K140UD8B	K1NT591Ye	K1NT591Ye
	K140UD8V	1KT621A	162KT1A
	K140UD11	ŁKT621B	162KT1B
	K140UD13	K1KT621	K162KT1
	K140MA1	K1US671	K167UN1
	KR140UD1A	--	K167UN3
	KR140UD1B	1KT682A	168KT2A
	KR140UD1V	1KT682B	168KT2B
	142YeN1A		K170UP1
	142YeN1B		K174AF1
	142YeN1V		K174AF4
	142YeN1G		K174KhA1
	K142YeN2A		K174UR1
	K142YeN2B		K174UR2A
	K142YeN2V		K174UR2B
	K142YeN2G		K174UR3
	K148UN1		K174UN5
	K148UN2		K174UN7
1KT491A	149KT1A		K174UN8
1KT491B	149KT1B	K1US744A	K1US744A
1KT491V	149KT1V	K1US744B	K1US744B
K1KT491A	K149KT1A		K174UP1
K1KT491B	K149KT1B	LDA751	175DA1
K1KT491V	K149KT1V	1US751A	175UV1A
1UT531	153D1	1US751B	175UV1B
	153UD2	1US752B	175UV2
	153UD3	1US753A	175UV3A
	153UD4	1US753B	175UV3B
	153UD5A		175UV4
	153UD5B	k1DA751	K175DA1
	153UD6		K175UV1A
K1UT531A	K153UD1		K175UV1B
	K175UV2A	K1NT985B	K198NT5B
	K175UV2B	K1NT986A	K198NT6A
	K175UV3A	K1NT986B	K198NT6B
	K175UV3B	K1NT987A	K198NT7A
	K175UV4	K1NT987B	K198NT7B
1US771	177UP1	K1NT988A	K198NT8A
1UT771	177UD1	K1NT988B	K198NT8B
	K177UP1	2UI181	218UI1

Table continued

K1UT771A	K177UD1A	2UI182	218UI2
K1UT771B	k177UD1B	2UI185	218UI3
1KT901	190KT1	2TK181	218TK1
1KT902	190KT2	2GF181	218GG1
K1KT901	K190KT1	2GF182	218AG1
K1KT902	K190KT2	2US181	218UR1
1US981A	198UN1A	2UE181	218UYe1
1US981B	198UN1B	2UE182	218UK2
1US981V	198UN1V	2DA181	218DA1
1UT981A	198UT1A	K2UI181	K218UI1
1UT981B	198UT1B	K2UI182	K218UI2
1NT981A	198NT1A	K2UI183	K218UI3
1NT981B	198NT1B	K2%K181	K218TK1
1NT982B	198NT2B	K2US181	K218UR1
1NT983	198NT3	K2GF182	K218AG1
1NT985A	198NT5A	K2UE181	K218UYe1
1NT985B	198NT5B	K2UE182	K218UYe2
1NT986A	198NT6A	K2DA181	K218DA1
1NT986B	198NT6B	2NT192	219NT2
1NT987A	198NT7A	2GS191	219GS1
1NT987B	198NT7B	2GS192	219GS2
1NT988A	198NT8A	2GS193	219GS3
1NT988B	198NT8B	2DS191	219DS1
K1US981A	K198UN1A	2MS191	219MS1
K1US981B	K198UN1B	2MS192	219MS2
K1US981V	K198UN1V	2PS191A	219PS1A
K1UT981A	K198UT1A	2PS191B	219PS1B
K1UT981B	K198UT1B	2US191A	219UV1A
K1NT981A	K198NT1A	2US191B	219UV1B
K1NT981B	K198NT1B	2US192	219UR1
K1NT982A	K198NT2A	2US194	219UP1
K1NT982B	K198NT2B	2US193	219UN1
K1NT983A	K198NT3A		K224Ag1
K1NT983B	K198NT3B		K224AG2
K1NT984A	K198NT4A		K224AG3
K1NT984B	K198NT4B		K224GG1
K1NT985A	K198NT5A		K224GG2
	K224%P11	2US264B	226UN4B
	K224TK1	2US265A	226UN5A
	K224UP1	2US265B	226UN5B
	K224UP2	2US265V	226UN5V
K2US242	K2US242	K2US261A	K226UN1A
K2US245	K2US245	K2US261B	K226UN1B
K2US247	K2US247	K2US261V	K226UN1V
K2US248	K2&S248	K2US262A	K226UN2A
K2US2413	K2US2413	K2US262B	K226UN2B
K2US2416	K2US2416	K2US262V	K226UN2V
K2PP241	K2PP241	K2US263A	K226UN3A
K2ZhA242	K2US263B	K226UN3B	
K2ZhA243	K2ZhA243	K2US263V	K226UN3V
K2ZhA244	K2ZhA244	K2US264A	K226UN4A

Table continued

	K224PN1	K2US264B	K226UN4B
K2UP241	K224UP1	K2US264V	K226UN4V
	K224UP2	K2US265A	K226UN5A
	K224UP3	K2US265B	K226UN5B
	K224KhP1	K2US265V	K226UN5V
	K224SA3	K2D281	228KN1
	K224UN2	2PD281	228PP1
	K224UN16	2PD282	228PP2
	K224UN17	2SA281	228SA1
	K224UN18	2US281	228UV1
	K224UN19	2US283	228UV3
	K224GG1	2US284	228UV4
	K224GG2	2US282	228UV2
K2NT241A	K224NT1A	2NK281	228NK1
K2NT241B	K224NT1B	2NYe281	228NYe1
K2NT241V	K224NT1V		K228KN1
	K224NT1		K228PP1
	K224NR2		K228PP2
	K224TP1		K228SA1
	K224TK1	K2US281	K228UV1
	K224AG1	K2US282	K228UV2
	K224AG2	K2US283	K228UV3
	K224AG3	K2US284	K228UV4
2US261A	226UN1A	K2NK281	K228NK1
2US261B	226UN1B	K2NYe281	K228NYe1
2US261V	226UN1V	2DA351	235DA1
2US262A	226N2A	2DA352	235DA2
2US262B	226UN2B	2DS351	235DS1
2US262V	226UN2V	2KD351	235KP1
2US263A	226UN3A	2KD352	235KP2
2US263B	226UN3B	2MP351	235MP1
2US264A	226UN4A	2MP352	235MP2
2PA351	235PS1	2US658	265UV7
2PS352	235PS2		K265KN1
2PM351	235AP1		K265PP1
2PP351	235PP1		K265PP2
2US351A	235UV1A	K2US651	K265UV1
2US351B	235UV1B	K2US652	K265UV2
2US352	235UR2	K2US653	K265UV3
2US353	235UR3	K2US654	K265UV4
2US354	235UN4	K2US655	K265UV5
2US355	235UN5	K2US657	K265UV6
2US357	235UR7	K2US658	K265UV7
2US358	235UR8	K2US656	K265UD1
2US359	235UR9	2US721A	272UV1A
2US3510	235UN10	2US721B	272UV1B
2US3511	235UR11	2US721V	272UV1V
K2ZhA371	K237KhK1	2US721G	272UV1G
K2ZhA372	K237KhK2	2US721D	272UV1D
K2ZhA373	K237KhK3	2US721Ye	272UV1Ye
K2ZhA375	K237KhK5	2US721Zh	272V1Zh

Table continued

K2GS371	K237GS1	2US721Z	272UV1Z
K2ZhA376	K237KhK6	2US721I	272UV1I
K2US371	K237UN1	2US721K	272UV1K
K2US372	K237UN2	2US721L	272UV1L
K2US373	K237UN3	2US721M	272UV1M
K2US375	K237UN5	2US721N	272UV1N
K2KD521A	K252KT1A	2US7210	272UV10
K2KD521B	K252KT1B	2US721P	272UV1P
K2PD521	K252PA1	2US721R	272UV1R
K2PD522	K252PA2	2US721S	272UV1S
K2PD524	K252PA3	2US721T	272UV1T
K2PN521	K252PN1	2US722A	272UV2A
2KSA521	K252SA1	2US722B	272UV2B
K2ZhA521A	K252UD3A	2US722V	272UV2V
K2ZhA521B	K252UD3B	2US722G	272UV2G
	K264GF1	2US722D	272UV2D
	K264UI1	2US722Ye	272UV2Ye
2KD651	265KN1	2US722Zh	272UV2Zh
2PD651	265PP1	2US722Z	272UV2Z
2PD652	265PP2	2US722I	272UC2I
2US651	265UV1	2US722K	272UV2K
2US652	264UV2	2US722L	272UV2L
2US653	265UV3	2US722M	272UV2M
2US654	265UV4	2US722N	272UV2N
2US655	265UV5	2US7220	272UV20
2US656	265UD1	2US722P	272UP2P
2US657	265UV6	2US722R	272UV2R
2US722S	272UV2S	K2US722I	K272UV2I
2US722T	272UV2T	K2US722K	K272UV2K
2US723A	272UV2A	K2US722L	K272UV2L
2US723B	272UV2B	K2US722M	K272UV2M
2US723V	272UV2V	K2US722N	K272UV2N
2UA723G	272UV2G	K2US7220	K272UV20
2US723D	272UV2D	K2US722P	K272UV2P
2US723Ye	272UV2Y2	K2US722R	K272UV2R
2US723Zh	272UV2ZH	K2US722S	K272UV2S
2US723Z	272UV2Z	K2US722T	K272UV2T
2US723I	272UV2I	K2US723A	K272UV3A
2UA723K	272UV2K	K2US723B	K272UV3B
2US723L	272UV2L	K2US723V	K272UV3V
2US723M	272UV2M	K2US723G	K272UV3G
2US723N	272UV2N	K2US723D	K272UV3D
2US7230	272UV20	K2US723Ye	K272UV3Y2
2US723P	272UV2P	K2US723Zh	K272UV3Zh
2US723R	272UV2R	K2US723Z	K272UV3Z
2US723S	272UV2S	K2US723I	K272UV3I
2US723T	272UV2T	K2US723K	K272UV3K
K2US721A	K272UV1A	K2UA723L	K272UV3L
K2US721B	K272UC1B	K2US723M	K272UC3M
K2US721V	K272UV1V	K2US723N	K272UV3N
K2US721G	K272UV1G	K2US7230	K272UC30

Table continued

K2US721D	K272UV1D	K2US723P	K272UC3P
K2US721Ye	K272UC1Ye	K2US723R	K272UC3R
K2US721Zh	K272UC1Zh	K2US723S	K272UC3S
K2US721Z	K272UV1Z	K2US723T	K272UV3T
K2US721I	K272UV1I	K2US724A	K272UC4A
K2US721K	K272UC1K	K2US724B	K272UV4B
K2US721L	K272UV1L	K2KS724V	K272UV4V
K2US721M	K272UV1M	K2US724G	K272UV41
K2US721N	K272UV1N	K2US724D	K272UV4D
K2US7210	K272UV10	K2US724Ye	K272UV4Ye
K2US721P	K272UV1P	K2US724Zh	K272UV4Zh
K2US721R	K272UV1R	K2US724Z	K272UV4Z
K2US721S	K272UV1S	K2US724I	K272UV4I
K2US721T	K272UV1T	K2US724K	K272UV4K
K2US722A	K272UV2A	K2US724L	K272UV4L
K2US722B	K272UV2B	K2US724M	K272UV4M
K2US722V	K272UV2V	K2US724N	K272UV4N
K2US722G	K272UV2G	K2US7240	K272UV40
K2US722D	K272UV2D	K2US724P	K272UV4P
K2US722Ye	K272UV2Ye	K2US724R	K272UV4R
K2US722Zh	K272V2Zh	K2US724S	K272UV4S
K2US722Z	K272UV2Z	K2US724T	K272UV4T
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K2US725B	K272UV5B	K2SS842A	K284SS2A
K2US725V	K272V5V	K2SS842B	K28SS2B
K2US725G	K272UV5G	K2UE841A	K284UYe1A
K2US725D	K272UV5D	K2UE841B	K384UYe1B
K2US725Ye	K272UV5Ye		K284UD2
K2US725Zh	K272UV5Zh		K284UD1A
K2US725Z	K272UV5Z		K284UD1B
K2US725I	K272UV5I		K284UD1V
K2US725K	K272K	ZNSO11A	ZO1NR1A
K2US725L	K272UV5L	ZNSO11B	ZO1NR1B
K2US725M	K272UV5M	ZNSO11V	ZO1NR1V
K2US725N	K272UV5N	ZNSO11G	ZO1NR1G
K2US7250	K272UV50	ZNSO11D	ZO1NR1D
K2US725P	K272UV5P	ZNSO11Ye	ZO1NR1Ye
K2US725R	K272UC5R	ZNSO11Zh	ZO1NR1Zh
K2US725S	K272UV5S	ZNSO11Z	ZO1NR1Z
K2US725T	K272UV5T	ZNSO11I	ZO1NR1I
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K2US726B	K272UC6B	ZNSO11L	ZO1NR1L
K2US726V	K272UV6V	ZNSO11M	ZO1NR1M
K2US726G	K272UV6G	ZNSO12	ZO1NR2
K2US726D	K272UV6D	ZNSO13	ZO1NR3
K2US726Ye	K272V6Ye	ZNSo14A	ZO1NR4A
K2US726Zh	K272V6Zh	ZNSO14B	ZO1NR4B
K2US726Z	K272UV6Z	ZNSO14V	ZO1NR4V
K2US726I	K272UC6I	ZNSO14G	ZO1NR4G
K2US726K	K272UC6K	ZNSO14D	ZO1NR4D
K2US726L	K272UV6L	ZNSO14Ye	ZO1NR4Ye

Table continued

K2US726M	K272UV6M	ZNS014Zh	Z01NR4Zh
K2US726N	K272UV6N	ZNS014Z	Z01NR4Z
K2US7260	K272UV60	ZNS014I	Z01NR4I
K2US726P	K272UV6P	ZNS014K	Z01NR4K
K2US726R	K272UV6R	ZNS014L	Z01NR4L
K2US726S	K272UV6S	ZNS014M	Z01NR4M
K2US726T	K272UV6T	ZNS015A	Z01NR5A
	284KN1	ZnS015B	Z01NR5B
	284PU1	ZNS015V	Z01NR5V
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2SS842B	284SS2B	ZNS015D	Z01NR5D
2UE841A	284UYe1A	ZNS015Ye	Z01NR5Ye
2UE841B	284UYe1B	ZNS015Zh	Z01NR5Zh
	284UD2	ZNS015Z	Z01NR5Z
	K284UN1A	ZNS015I	Z01NR5I
	K284UN1B	ZNS015K	Z01NR5K
	K284KN1	ZNS015L	Z01NR5L
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Set of n-p-n transistors	243NT1, 243NT2, 243NT3	305
Set of combined elements	204NK1, K204NK1	239
Set of n-p-n transistors	217NTL, K217NT1, 217NT2, K217NT2,	260
	217NT3, K217NT3	260
Diode assembly	217NK1, K217NK1	259
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