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USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 1/82)

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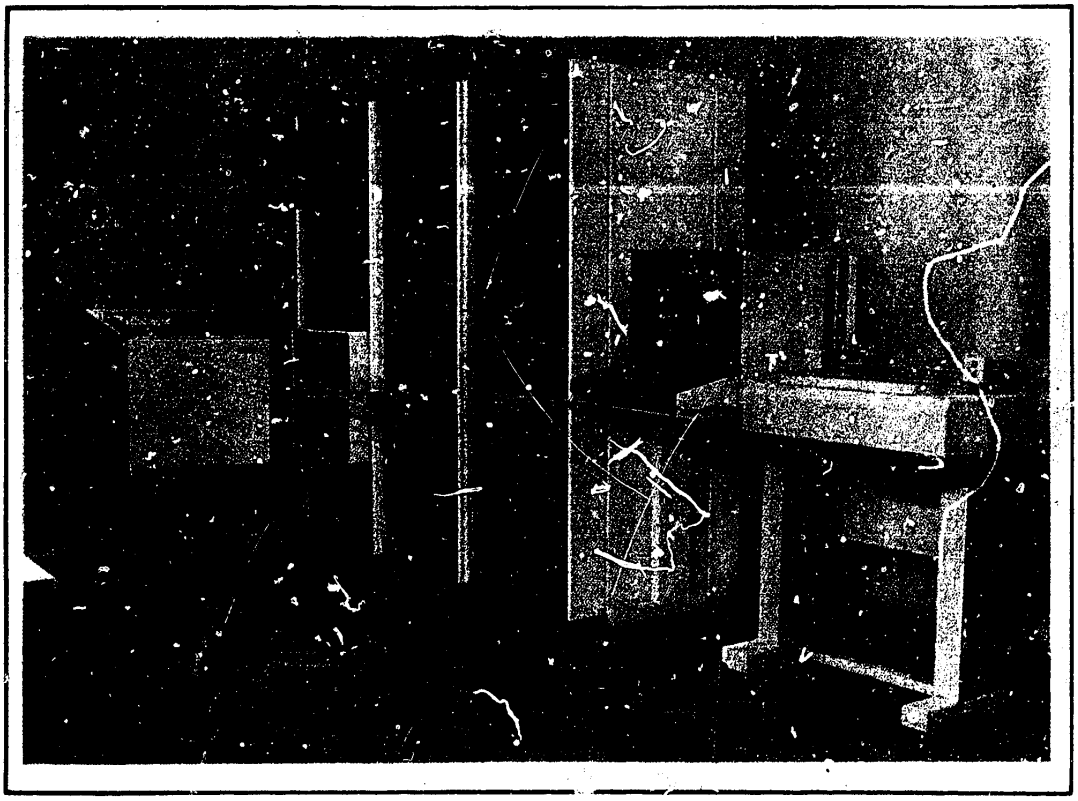
PUBLICATIONS

HARDWARE

SM-2M MASTER COMPUTER COMPLEX

Kiev ELEKTRONNOYE MODELIROVANIYE in Russian No 6, Nov-Dec 81 inside front cover



[Text] The SM-2M master computer complex (an updated version of the SM-2 computer complex) was developed by the Severodonetsk Scientific Research Institute of Control Computers and by the "Impul's" Scientific-Production Association. It is used in complex automated production process control systems, in automated scientific experimentation systems requiring high productivity and reliability, in the top level

of the hierarchical control systems managing the work of complex machine units, shops and production operations, in systems used to test complex equipment, to process medical data and so on.

11004
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SELECTION OF STRUCTURE OF ONE CLASS OF THRESHOLD ELEMENT MEMORIES

Kiev ELEKTRONNOYE MODELIROVANIYE in Russian No 6, Nov-Dec 81
(manuscript received 20 Feb 81) pp 88-89

[Article by Eduard Yur'yevich Kirsanov, engineer-designer, Kazan']

[Text] Creation of complex information processing systems, computers and computer systems in particular, has resulted in broader research and development in information storage technology. One of the promising methods for creating effective memories is to develop new memory structures based on threshold logic.

Among the various kinds of memories, there are superoperational memories characterized by grouped serial recording, small capacity and high speed. In this case the presence of serial recording and the possibility for both random and serial read-out allow us to view such superoperational memories as learning pattern recognition systems in which learning is equivalent to recording and recognition is equivalent to read-out.

Figure 1 is a general block diagram of such a pattern recognition system; $x(n)$ is a multivariate process representing an input sequence of patterns equivalent to the address signals of superoperational memories. Signal $\varepsilon(n)$ is defined as the teacher's statement that the current pattern belongs to a certain class; in this case code $\bar{\varepsilon}$ is equivalent to the code of the current information word to be recorded. Multivariate output vector $x_k(n)$ is formed in the form of the pattern recognition system's data indicating that the current image belongs to a certain point in the solution space, and it is equivalent to the information word being read out. In this case $\bar{x}_k = \bar{\varepsilon}$.

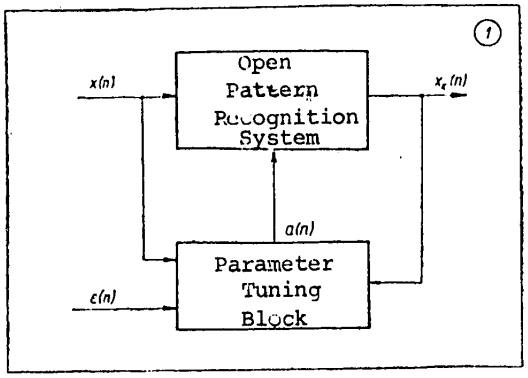

Figure 1

The parameter tuning block outputs vector $a(n)$ of the values of tuneable parameters of the open pattern recognition system--that is, it supports a process equivalent to recording.

When analyzing the architecture of a superoperational memory, it is convenient to represent the latter as a system of N^* pattern recognition systems falling into two classes, where N^* is the length of the recorded information words $\bar{\varepsilon}$. This approach simplifies analysis in synthesis of a digit recognition system, and it is easier and more effective to make a modular superoperational memory consisting of a set of identical digit recognition systems recognizing two classes.

A superoperational memory is typified by change in the composition of the recorded information in each cycle of grouped recording, which requires each fixed digit recognition system to realize a universal hypersurface which would satisfy any class distribution of L points with coordinates represented by N-digit code addresses (patterns) in a multidimensional address space X, which is impossible. However, the following assertion may be introduced: The initial space X can always be transformed into a secondary space X' with L' vectors of rank N' ($L'>L$, $N'>N$), which contains a set of L patterns divisible by one hypersurface into two classes in the presence of any 2^L combinations of unidimensional vectors of teacher statement $\bar{\varepsilon}$. It follows from this that the structure of a superoperational memory must always contain a vector code converter transforming $\bar{x}$ into $\bar{x}'$.

From 4 to 16 information words are usually written for a superoperational memory with capacity L. Therefore we can always obtain a secondary space X' in which there are L vectors $\bar{x}'$, divisible by one linear surface no matter what their distribution, as we can see below. A superoperational memory would best consist of a digit recognition system composed of one logical threshold element having the capacity for learning in response to inputs during formation of the optimum hypersurface, which is a function of the memory.

The output signal of the logical threshold element is defined as the sum of the products of the unity digits of the code of vector $\bar{x}'$ times the weight coefficients a_i of the corresponding inputs (1)--that is, by the size of the logical threshold element's input,

$$\sum_{i=1}^{N'} a_i x_i,$$

where $i = 1,2,\ldots,N'$. In this case the threshold θ for a learning logical threshold element must be chosen in relation to the initial values of the weight factors $\bar{a}$ in such a way as to satisfy the following conditions:

$$x_k = 1, \quad \text{if} \sum_{i=1}^{N'} a_i x_i \geqslant \theta;$$

$$x_k = 0, \quad \text{if} \sum_{i=1}^{N'} a_i x_i < \theta.$$

It follows from these expressions that if there is to be a fixed threshold, all codes x' of the sequence of addresses with length L must have the same constant number of units--that is, active digits, for example 50 percent of N'. Thus if we are to build a superoperational memory out of identical logical threshold elements with a fixed threshold, addresses $\bar{x}'$ must be fed in parallel to all digit logical threshold elements with N' learning inputs; in this case the address codes must have a standard constant active length. This simplifies the structure of the superoperational memory and the logical threshold element, making it easier to build them.

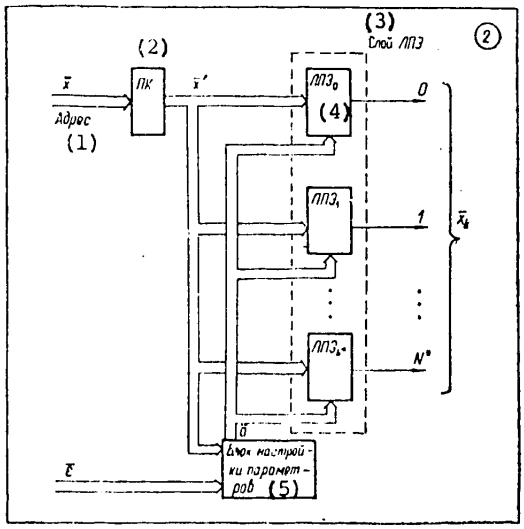

Figure 2

Key:
1. Address
2. Code converter
3. Logical threshold element layer
4. Logical threshold element
5. Parameter tuning block

With a superoperational memory, the recording and reading of information known *a priori* proceeds in the same time scale and in the same object, and it coincides in space. A pattern recognition system performing the function of a superoperational memory must function in real time; in this case a parameter tuning block must be included in its physical structure so as to permit tuning in a closed loop system (2).

To support learning in a logical threshold element, it would be best to use one-step learning algorithms, for example like the learning algorithms of perceptrons (3), in order to ensure high speed, and particularly to reduce recording time, which is equivalent to learning time. The correctness with which the optimum hypersurface develops in the course of recording (learning) need not be monitored, since it is ensured by the structure itself of the learning algorithm. Therefore the tuning block is built as a one-step learning algorithm, and there is no feedback for monitoring transmission of a recording from the recognition system's output to the tuning block.

Figure 2 shows the basic diagram of a superoperational memory based on logical threshold elements accounting for the requirements described above. A model of such a superoperational memory was built in the form of a program for a YeS computer. The program was written in PL/1. Experiments with this model confirmed the correctness of the premises suggested here concerning structural organization, and made it possible to obtain data to be used in further research with the purpose of increasing the capacity and speed of the superoperational memory.

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11004
CSO: 1863/49

DEVICE FOR MEASURING STEADY-STATE PARAMETERS OF MIS LSI-CIRCUIT COMPONENTS

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 8, Aug 81 pp 26-27

[Article by engineers L. S. Ganopol'skiy, V. V. Zhukov and V. Ye. Novosel'tsev: "Device for Measuring Steady-State Parameters of MIS LSI-Circuit Components"]

[Text] The instrument-manufacturing industry has now been seeing a sharp increase in the volume and nomenclature of the integrated circuits (IC) in production, such as, for example, BIS [large-scale integrated (LSI) circuits] used in the production of timepieces and microcalculators, for which MIS components form the basis.

In designing IC and monitoring the process of their manufacture it is necessary to have information on the electrophysical parameters of the material, the geometry and the distribution of impurities etc. Unfortunately, however, not all this information can be obtained by simple and easily employed methods. Most of them require precision physical procedures and complex apparatus. Indirect methods of measuring the parameters of semiconductor structures are therefore assuming particular importance. The electrical measurement method is the simplest of these.

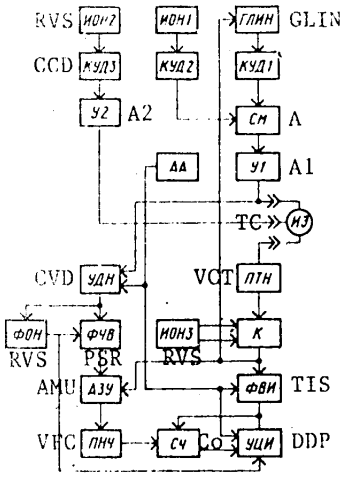
The physical properties and electrophysical parameters of LSI circuits are studied by electrical methods on specially designed test structures [2]. The results of these studies then provide the basis for modeling the functioning of an LSI circuit, establishing the inter-relationship between output parameters and design and production factors and evaluating its stability with respect to the effect of various operational factors.

There now exist a variety of control and measuring apparatus for measuring steady-state and dynamic parameters as well as for functional monitoring [3, 4]. The general-purpose nature of this apparatus, however, and, accordingly, its high cost and the complexity of its architecture and operation make it unsuitable for use in measuring test structures. The development of a simple, specialized apparatus has therefore become a matter of urgent importance.

This category of apparatus would include a digital apparatus for measuring steady-state IC parameters designed to determine threshold MIS-transistor voltages, leakage currents and the resistances of the diffusion junctions and contact windows of IC manufactured on the basis of p- and n-channel MIS technology.

A structural diagram of the instrument is shown in the figure. Breakdown and threshold voltages are determined by measuring the instantaneous value of the linearly variable voltage (LVV) applied to the test component (TC) at the moment the current flowing through component TC reaches the selected value. The master oscillator for the linearly

variable voltage OLVV generates a voltage of constant amplitude, while its polarity may be either positive or negative. In the absence of component TC, the oscillator OLVV output voltage takes the form of an isosceles triangle. A code-controlled divider CCD1 makes it possible to obtain a discrete series of amplitudes of the voltages supplied to the first adder A input. The reference-voltage source RVS1 and code-controlled divider CCD2 form a discrete series of amplitudes of constant voltage, which is supplied to the second adder input and forms a "pedestal," that is, that level of constant voltage at which the LVV pulse begins and ends. Voltage, amplified by amplifier U1, is fed from adder A output via an output connector to the component TC. The current passing through the latter becomes the input current to the voltage-current transformer VCT, the output signal of which is fed to the input of dual comparator C. Fed as reference voltages to the comparator from the output of reference-voltage source RVS3 are two signals equal in modulus but opposite in sign.



The comparator changes its state if the output signal of the transformer VCT exceeds with respect to absolute value the positive or negative reference voltage depending upon the direction of the current through the component under study. Since the input resistance of the transformer VCT is negligibly low as compared with the resistance of the given component TC, it may accurately enough be considered that the full voltage of amplifier A1 is being applied to the component TC. This voltage is also supplied to the controlled voltage divider CVD, which breaks the measured voltage down into ranges. Together with the reference-voltage shaper RVS, the phase-sensitive rectifier PSR converts the signal to unipolar voltage, which is then fed to an analog memory unit AMU. As long as the current across the component TC is low and the comparator C remains in its initial state, this unit AMU functions in a follower mode. When the current across the component TC reaches the desired level, the comparator C changes its state and the memory unit AMU switches to its storage mode.

At the same time, the LVV drops rapidly, while the time-interval shaper TIS permits pulses to pass from the voltage frequency converter VFC to a counter Co. Following the counting process the result is illuminated on a digital display panel DDP. An amplitude analyzer AA selects the transmission coefficient of the divider CVD, the time interval of the shaper TIS and the position of the point on the display panel DDP. Information on the polarity of the measured voltage is supplied to the display panel DDP from the shaper RVS. Voltage shaped by reference-voltage source RVS2, code-controlled divider CCD3 and amplifier A2 is used to study transistors for current drain.

Measurement of resistances does not require the introduction of additional units into the instrument circuit. When the comparator C is switched on, the output voltage U_o of the transformer VCT equals the reference voltage U_c of the comparator: $U_o = kI_i = kU_x/R_x = U_c$, where k is the transformation coefficient of the transformer VCT, I_i the input current of the transformer VCT (that is, the current across the component TC) and U_x and R_x the voltage applied to the component TC and its resistance respectively.

From this expression we obtain $R_X = (k/U_C)U_X$.

Accordingly, the measurement of resistances also reduces to calculation of the values of voltages applied to the component TC at the moment the comparator begins to function.

Specifications of the measuring device

Range of LVV control, V	-200 to +200
LVV buildup time, s	5
Designated current levels, μA	1; 2; 5; 10
Range of resistance measurements, kΩ	1-10; 10-100
Range of voltage-drain control, V	-50 to +50
Basic relative error in current-level setting, %	±5
Basic reduced measurement error, %:	
resistance	±3
voltage	±2.5
Supply voltage	220±22 (50 Hz)

The measuring device has a printer which records the digital result of the measurement, the value measured and the current value at which threshold voltage (breakdown voltage) is calculated. It is also possible to control the instrument remotely. When made compatible with a desktop computer, the measuring device permits statistical analysis and determination of the parameters of the distributions of the measured values.

The instrument was developed by the Penza branch of VNITIpribor [All-Union Scientific-Research Technological Institute of Instrument Making]. Practical experience in using this measuring device in one of the industry's enterprises has demonstrated its simplicity and ease of operation.

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8963
CSO: 1863/36

PULSE-SEQUENCE PHASE-SHIFT INDICATOR

Moscow PRIBORY I SISTEMY UPRAVLENIYA in Russian No 8, Aug 81 pp 27-28

[Article by engineers E. V. Rakhov and Yu. S. Savchenko: "Phase-Shift Indicator of Pulse Sequences"]

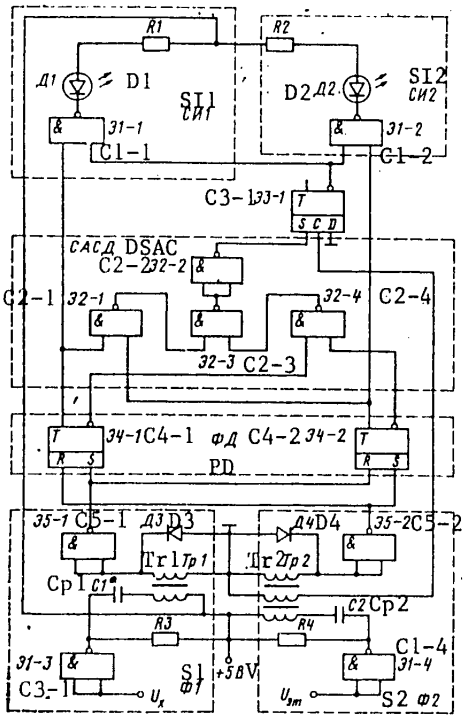
[Text] Imperfections in the design of electromechanical systems of magnetic-tape storage (MTS) constitute one of the most widespread causes of phase distortion in record channels and in the reproduction of discrete information. Gap scatter, a shift of the magnetic head unit relative to the axis perpendicular to the direction of tape travel, tape skew etc. cause impermissible phase shifts of pulse sequences, which distort MTS information. MTS phase shifts are normally eliminated with the use of control and measuring equipment, which, while offering a number of advantages in adjusting storage systems under plant conditions [1], proves, however, inconvenient and ineffective in adjustments connected with checking the phase state of MTS channels.

Pulse-sequence phase indicators may be employed in accomplishing this maintenance. The literature on phase-measuring equipment describes a number of these devices, but they either require additional expenditures to insure compatibility with the component base [2] or have a complex circuit control.

In the present article the authors propose a device indicating pulse-sequence phase shift having high resolution. A schematic diagram of the indicator is shown in the figure. The positively polarized pulse sequence U_x under analysis is supplied to the inputs of shaper S1, a standard positively polarized pulse sequence U_s to the inputs of shaper S2. Short pulses generated along the leading edge of the input pulses are transmitted from the outputs of components C5-1 and C5-2 to the inputs of phase discriminator PD, which is based upon flip-flops C4-1 and C4-2.

If the pulses of the analyzed sequence lead in phase those of the standard sequence, then during each period the pulses from the output of component C5-1 enter the S-input of flip-flop C4-1 and the R-input of flip-flop C4-2, setting the first in the logical "1" state , the second in the logical "0" state. A pulse from the output of component C5-2 lagging behind by part of a period, a phase shift, is fed to the R-input of flip-flop C4-1 and the S-input of flip-flop C4-2, setting them in the opposite states respectively.

The process of comparing phases over the period of a single pulse sequence is thus complete when the phase discriminator PD supplies a resolving voltage to component C1-2 of the sign-indication circuit SI2 and an inhibiting voltage to component C1-1 of indicator circuit SI1. Since to the No. 2 inputs of components C1-1 and C1-2 is fed resolving voltage from the inverse output of flip-flop C3-1, which has been set to the



Schematic circuit diagram of pulse-sequence phase shift indicator: C1, C2, C5 and C3, C4 - K155LA8, K155LAZ, and K155TM2 microcircuits respectively; D1, D2 - AL102B LEDs; D3, D4 - KD407A LEDs; Tr1, Tr2 - TIM-26 pulse transformers; R1-R4 - OMLT resistors (R1=P2=150 Ω; R3=R4=22 kΩ); Cp1*≅Cp2= = 910 pF - KDM capacitors.

logical "0" state by a positively polarized pulse from transformer winding Tr2, a current flows through LED D2. LED D2 illumination corresponds to the "lead" indication.

If the pulses in the sequence under analysis lag behind those in the standard sequence, the state of the phase-discriminator flip-flops changes to its opposite; the resolving voltages are now fed for most of the period to component C1-1, the current accordingly flowing through LED D1. LED D1 illumination now corresponds to the "lag" indication.

If the analyzed and standard pulse sequences are in phase and the time characteristics of the shapers are identical, the pulses from components C5-1 and C5-2 coincide with respect to both time of leading-edge formation and duration. The phase discriminator flip-flops are therefore to be found in a state which is characterized as indeterminate; by means of two AND-NOT gates (components C2-1 and C5-2), the discriminator-state-analysis circuit DSAC in this instance records the identity of discriminator flip-flop states, while the zero signal from the output of the analysis circuit inverter C2-2 is fed to the S-input of flip-flop C3-1, switching it to a logical "1" state. An inhibiting voltage is fed from the inverse output of flip-flop C3-1 to the inputs of components C1-1 and C1-2 and LEDs D1 and D2 de-energized. The absence of LED illumination indicates that the analyzed and standard pulse sequences are in phase.

The phase-shift indicator functions throughout a broad range of pulse-sequence frequencies, the frequency characteristics of the shapers and flip-flops of the phase discriminator constituting the factors limiting the upper frequency. The device registers phase shifts from a minimum corresponding to the resolving capability of the indicator to 360°. It should be pointed out, however, that ambiguous indication at low pulse-sequence frequencies and with phase shifts exceeding 30-40° are characteristic of this system. This phenomenon is to be explained by the indicator's lack of a selection of time intervals corresponding to the magnitudes of the phase shifts and is being eliminated by minor modification of the circuit controlling flip-flop C3-1.

The resolution of the device is governed primarily by the identity of channel-former characteristics, the duration of the pulses fed to the inputs of the phase discriminator and by the frequency characteristics of the discriminator flip-flops.

This phase-shift indicator design has been developed for a specific application, but the device's range of functional capabilities is much broader: it may also be employed

as a comparator for comparing pulse durations, as a component of a direct-conversion phase meter and, given a channel-forming capability, for recording phase shifts in any form of periodic oscillation.

The authors have fabricated a working model of the phase-shift indicator, which has been tested on a YeS5012-01 MTS unit. It has been employed to make preventive checks and adjust the azimuth of a magnetic head unit and to test and compensate for phase shift during "record" and "playback" operations. The experimentally established resolution of a device incorporating series-155 microcircuits does not exceed 40 ns, that is, less than 1° at a frequency of MTS timing-pulse sequence of 64 kHz.

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8963
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SPECIAL-PURPOSE PROCESSOR FOR RAPID FOURIER TRANSFORM

Leningrad ORGANIZATSIYA VYCHISLITEL'NYKH STRUKTUR I PROTSESSOV: PROYEKTIROVANIYE SISTEM VVODA-VYVODA EVM in Russian No 8, 1981 (signed to press 31 Dec 80) pp 113-115

[Article by V. I. Gorelik, "Special-Purpose Processor for Rapid Fourier Transform", from collection "Organizing Computer Structures and Processes: The Design of Computer Input/Output Systems", edited by Z. I. Tsar'kova, Izdatel'stvo Leningradskogo universiteta, 2449 copies, 184 pages]

[Text] Most rapid Fourier transform algorithms (Kuli-T'yuki, Senda-T'yuki [transliterated] and others [1, 2]), which are employed to realize rapid spectral decomposition of signals under study, make it possible to obtain decomposition coefficients whose sequence is doubly inverse with respect to the true [sequence]. This slows the researcher's work considerably, which is most undesirable in real-time problem solving, and in the case of large blocks makes it impossible (impossible are direct projection of the spectrum on the oscillograph CRT and use of a plotter to plot the graph of the spectral function).

The task of sorting the Fourier coefficients obtained from a rapid Fourier transform in accordance with the double inversion rule is conventionally accomplished as follows. Indices, the ordinal numbers of the elements of the input blocks, are represented in the form of n-dimensional binary vectors

$$K = \{k_1, k_2, \ldots, k_n\} ,$$

where $n = \log_2 M$, M - the dimensions of the input block, $k_i \in \{0,1\}$.

Thus stored in memory is a rectangular matrix with dimensions M X n. The columns of this matrix are then rearranged in accordance with the rule of the double inversion of their numbers, that is, to a mirror image with respect to the mean matrix vertical, and new index values calculated as binary sums

$$J = \sum_{j=1}^{n} \bar{k}_j 2^j ,$$

where $\bar{k}_j$ is the value of the j-th order of the number of the transformed matrix.

Addresses are then, finally, assigned to the elements of the input block in accordance with the principle of indirect addressing

$$\Phi(i) = Z(J) , \quad i = 1,2,\ldots,M ,$$

where Z - an unordered array of Fourier coefficients,

Φ - an ordered array of these coefficients.

This algorithm suffers the drawbacks of large memory consumption (both matrices occupy a volume of M X n cells each) and the extended time required to generate these matrices.

The proposed method of ordering coefficients is free of these shortcomings; it requires that a secondary array of numbers be found of the dimensions M X 1. This permits a great reduction in the storage required and an acceleration of the sorting process, which contributes greatly to accelerating accomplishment of the task of determining the spectrum of a signal as a whole.

The algorithm for processor operation consists essentially in the following. A reference block

$$z(1)=0,\quad z(2)=2,\quad z(3)=1,\quad z(4)=3$$

is written into memory. The first four elements of the secondary block (ordinal numbers of the desired block) are determined as follows:

$$l(i)=z(i)2^{(n-2)},$$

where i = I,2,3,4; $n=\log_2 M$ (for a specific M). The next element of the secondary block is then analyzed:

$$l(m,j)=2^{(n-3)},$$

where m - number in sequence of the element of the secondary block (m= 5,6,...,M);
j - the number of the secondary block element under analysis among the block elements under analysis.

Let us now look at two cases.

a). If $l(m,j)=1$ the remaining elements of the secondary block are obtained by adding to each preceding element of the secondary block, beginning with the second, the units:

$$l(m+1)=l(2,j)+1, l(m+2)=l(3,j)+1,\ldots,l(2m-2)=l(m-1,j)+1.$$

b). If $l(m,j)=N\neq 1$, then to each preceding element of the secondary block, beginning with the second, we add the number N:

$$l(m+1)=l(2,j)+N, l(m+2)=l(3,j)+N,\ldots,l(2m-2)=l(m-1,j)+N$$

and again analyze the following element of the secondary block (its number among the elements analyzed will be j+1, while among the elements of the secondary block following in order it will be $2m - 2 + I = 2m - I$.)

The formula used to analyze this element is as follows:

$$l(2m-1,j+1)=\frac{l(m,j)}{2}. \qquad (1)$$

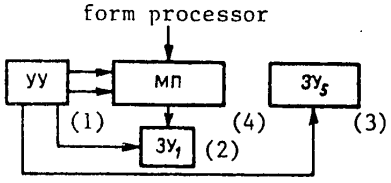
If this analyzed element equals 1, case a) is repeated and computation of the elements

of the secondary block discontinued, following which we make the next assignment (ordering):

$$y(\xi) = x(l(\xi)) , \qquad (2)$$

x - initial block, y - the unknown block and $\xi = 1,2,3,\ldots,M$.

If the analyzed element is not equal to 1, however, we repeat case b). The analyzed element is then computed in accordance with formula 1. The analysis continues until the analyzed element does not equal 1. We then repeat variant a) and assign in accordance with (2).



The figure is a structural diagram of the processor performing these operations. Its operation consists in the following. At a signal from the control unit (1) the reference block

$$x(1)=0 , \quad x(2)=2 , \quad x(3)=1 , \quad x(4)=3 .$$

is written into memory (2). The nonordered coefficients are transferred to the memory of the special processor ($ЗУ_2$) [as published; possibly (3) in diagram] from the processor realizing the rapid Fourier transform of the signal. The control unit transmits the signal to begin operation and controls the operation of the microprocessor (4) in accordance with the algorithm presented above. The Fourier coefficients are then ordered as follows:

$$y(i)=x(l(i)) , \quad i=1,2,3,\ldots,M .$$

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DESIGNING SPECIAL-PURPOSE MICROPROCESSOR COMPUTERS

Moscow PROYEKTIROVANIYE SPETSIALIZIROVANNYKH MIKROPROTSESSORNYKH VYCHISLITELEY in Russian 1981 (signed to press 13 Apr 81) pp 2-8, 160-161

[Annotation, introduction and table of contents from book "Special-Purpose Microprocessor Computer Design", by Yuriy Fedorovich Mukhopad, USSR Academy of Sciences, Siberian Division, Izdatel'stvo "Nauka", 4500 copies, 161 pages]

[Text] This work deals with theoretical and engineering problems associated with the design of computers with a specific functional algorithm. A unified LSI circuit or IC micro-assemblies are the components of execution. The book establishes applicability for processing information on high-speed processes, real-time production control, signal filtering and enhancing the productivity of general-purpose computers.

The book is intended for specialists in the fields of computer science and cybernetics and could also be useful to graduate students as well as students in upper-level courses.

Introduction

An orientation toward raising the qualitative level of the planned development of various branches of socialist industry, increasing the degree of automation and the achievement of higher levels of efficiency [1] dictates a comprehensive, integrated development of computer technology, which is governed not only by the quantity of general-purpose computers and their accompanying software, but also by the availability of microprocessor systems for computer information input and output and by the development of special-purpose computer equipment and systems.

Present-day high-productivity computer systems incorporate 4-6 general-purpose processors and 12-20 special-purpose processors [2] to control information input and output, plotters, displays, "automatic" text editors [3], automatic readers etc. On the other hand, the development of powerful associative information-processing systems confronts designers with the necessity of creating an homogeneous optoelectronic system, each component of which should essentially play the role of a special-purpose processor.

The employment of special-purpose computers and systems is also dictated by the need to develop systems for real-time control of facilities and processes, where even with the use of special programs the use of general-purpose microprocessors would be impossible because of the requirements for high operating speeds and, at times, for reliability, size and availability as well. In these systems, microprocessors may play the auxiliary role of an advanced arithmetic-logic unit, although simultaneously with the incorporation of parallel systems for high-speed execution of special functions, high-speed execution of multiplication operations, special interfaces and control devices [4].

The availability of microelectronic LSI circuits for working and permanent storage, programmed logic matrices, microprocessors, analog-digital converters etc. has made it possible to develop specialized computer hardware and systems with high levels of standardization, while at the same time maintaining an effective problem orientation as dictated by a particular sphere of application and requirements for specific features [5].

The trend toward specialization has also emerged in consequence of the fact that the increasing degree of component integration poses the problem of optimizing the correlation of software programs and hardware and permits a number of subsystems (emulators, translators etc.) to be fabricated in the form of special-purpose LSI-circuits.

Many tasks in the spheres of management and control require no calculations with accuracies greater than 0.1-0.5 per cent because of inaccurate raw information or error characteristic of the particular control servo components involved. A relay or analog-digital system functionally equivalent to the program as compiled, the general-purpose structure and its execution proves in this instance to be operationally faster and more reliable (above all because of the smaller number of components).

The need to search for a more generalized structure for computer hardware without leaning upon general-purpose digital-computer structure has also arisen with the development of analog-digital devices and their incorporation of the sequential principle of operation. This trend has now made its appearance in the specialized sphere of analog-to-digital information conversion, what with the fact that with coding comes the combination of the analog and digital noise-smoothing functions, functional scaling, information storage etc.

The use of functional converters (both analog and digital) in analog-digital and special-purpose devices eliminates the necessity of indicating the operation code, it being in this instance sufficient to indicate only the fact of access to the functional converter. A fundamental change is taking place in conception of the inter-relationship between converters and memory. In place of the traditional sequence of AU-ZU-AU [arithmetical unit-memory-arithmetical unit] transfers, the system now under discussion requires only that we insure the proper transfer of information between functional converters with storage of only a very limited number of intermediate results.

The concept "computer system" today is probably as broad as that of "computer hardware." As applied to microelectronic equipment this term may be understood to refer to multiprocessor computer systems (particularly those combining 4, 8, 16 or more microprocessors) with parallel computers or a system of digital and analog hardware including microelectronic versions of analog-code and code-analog converters, a microprocessor, working and permanent storage, an input/output control system and special units controlling the operation of the system as a whole.

Advances in the field of microelectronics permit utilization of the primarily hardware realization by virtue of the low cost, small dimensions and reliability with a comparatively complex circuit in a single crystal. This book therefore deals primarily not with problems in programming serial microprocessors in special-purpose systems, but rather with those involving the development of a system of devices employing a variety of microelectronic LSI-circuits, the principles governing optimum design of functional expanders for microprocessor systems and with problems in the design of control devices for special-purpose microprocessor systems.

We will be using the term "computer" to refer to a physical device consisting of information converters linked in a space-time relationship and realizing its functional purpose

of information processing through sequential movement of input information toward output terminals via converters with switching of converter functions if part of them can be set to perform a certain set of elementary conversions.

A computer must obviously consist of at least two basic units. A device consisting of only a single unit would be simply an elementary information converter. In this instance, when the physical form, scale or codes of any two converters interacting in the process of shifting information from input to output are not compatible, there must be intermediate information converters matching the varying forms in which the information is represented.

To define the structure of a system as the method of combining and inter-relating parts within a whole with reference to computers requires that we answer the following questions: what do we mean by a "part of a system"; what kind of links are there between these parts; and what law governs the changes in these links in both space and time. Computer components comprise converters of information and the links between them.

An elementary information converter would be a system F performing the function of mapping $x = \{x_1 x_2, \ldots, x_m\}$ into set $y = \{y_1 y_2, \ldots, y_n\}$, where m and n are the numbers of inputs/outputs of the elementary converter. Performing the function of an elementary converter may be a flip-flop, a register, an adder, logical m, n terminal, a more complex functional converter or any computer, a microprocessor (or microprocessor system), for example, whose internal structure we are not looking at, that is, it is incorporated into the computer as a simple component which at this stage of the analysis will not be broken down into simpler ones. Functional diode converters, components with discretely controlled parameters etc. constitute the elementary converters for hybrid computers.

The operator of an elementary converter determines its functional characteristics. In the case of the logic circuit this is a system of logical relationships, conversions of the e^x, sin x variety etc.

A unit capable of in turns performing the functions of several elementary converters we will refer to as a multifunction information converter.

Links between components may be spatial (connections between inputs and outputs), time links (via memory and reading at the required moment) and space-time links (when the result of conversion is stored in the converter itself).

The structure of a computer comprises a set of inter-connected information converters. A structural description would thus include the operators of all elementary information converters, an enumeration of the input and output variables for each converter and information on both space and time converter links.

The block diagram would consist of the various converters and the spatial links between them, while the structure emerges with additional information on the time relationships between the converters, in the form, for example, of the flow diagrams of programs, microprograms etc.

We will be distinguishing between structures with static and dynamic links. Structures with static links comprise that number of elementary converters which is sufficient to represent the entire mapping sequence by means of the elementary converters and the system of spatial links between them. Structures with static links correspond to the case of functional decomposition. These would include analog and hybrid systems etc.

Structures with dynamic links have only a limited number elementary converters and require repeated temporary access to them in the process of computer conversion of the information.

The process of switching from structural description to operator (analysis) is unambiguous. In a number of instances the operator cannot be fully determined, since that depends upon a specific value of a number of parameters (contents of program memory, for example). In this instance, however, the structure will be taken as given if the component operators are given and we know the algorithm for interaction between components in both space and time.

A reverse switch from the computer operator to the structure (synthesis) is multivalued and poses the problem of optimizing the switch, the criterion for which is the simplicity of the resulting structure and the elementary converters, decision time, the minimum of converters of a specific type etc.

We will be identifying the concept of the structure of a piece of computer hardware with that of the structure of a computer with dynamic links. The term "special-purpose computer" reflects the optimum adaptation (in terms of operational speed, for example) of a structure for solution of a specific category of problem.

This work generalizes the experience in designing special-purpose computers gained by the computer science department of the Eastern Siberian Technological Institute. The author wrote Sect. 2.4 together with V. K. Popkov and A. I. Fedchenko; 2.5 with V. A. Molodkin; 3.5 with K. A. Sharov; 4.1 with V. K. Popkov; 5.1 with T. S. Badmayev and 5.6 with L. O. Berezkov. Professor V. B. Smolov helped to formulate many of the problems dealt with in the book. This book could not have appeared without many years of support on the part of A. A. Nerchenko, candidate of technical sciences. The author expresses his deep appreciation to M. V. Mokhosoyev, doctor of technical sciences, and Professor D. Sh. Frolov for creating conditions favorable for scientific work.

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IMAGE-COMPARISON PROCESSOR

Moscow PROYEKTIROVANIYE SPETSIALIZIROVANNYKH MIKROPROTSESSORNYKH VYCHISLITELEY in Russian 1981 (signed to press 13 Apr 81) pp 139-140

[Section 5.3 from book "Special-Purpose Microprocessor Computer Design", by Yuriy Fedorovich Mukhopad, USSR Academy of Sciences, Siberian Division, Izdatel'stvo "Nauka", 4500 copies, 161 pages]

[Text] The image-comparison system constitutes an important control component in connection with the control of rolling mills, systems automatically navigating ships in areas of complex bottom relief, aerial photography, in automatic reading machines as well as in other extreme-correlation systems [96-99]. These systems have two kinds of storage (a unit storing references and unidentified images), a correlator, an image input and coding system, an address unit and a control unit. Let us look [97-99] at a version of a processor for comparing images on a photomatrix and using counters (with reference to coordinates x and y) in a microprocessor (Figure 71).

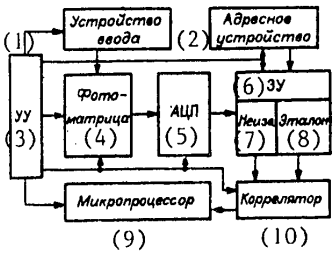

Figure 71: 1 - input unit; 2 - address unit; 3 - control unit; 4 - photomatrix; 5 - analog-digital converter; 6 - storage; 7 - u/i image; 8 - reference; 9 - - microprocessor; 10 - correlator.

If the field of an unidentified image A having dimensions m X n is larger than that of reference B, having dimensions p X q, $p \leqq m$, $q \leqq n$, the problem consists not only in determining the presence of one of the standards B_1, B_2, ..., B_3 in the unknown image, but also in establishing its location (with respect to coordinates x and y) in field A. In accordance with one strategy or another [96], the address unit should accordingly scan field B with reference to field A; each time a section of the unidentified image of dimension B is compared with coordinates x_k, y_r, the microprocessor should compare the value of the correlation function from the preceding comparison x_{k-1}, y_{r-1}. By looking at a specific reference B_j it can be decided that it is present in field A if the correlation function for B_j has a larger value.

In this solution the microprocessor performs the function of a logic unit (the operation of selecting the maximum of the correlation function and recording coordinates x_k, y_r); the control and address units are realized independently, while the information component constitues the series of inter-related units from the input unit to the correlator.

The realizability of the processor as a whole is governed by successful design of the structural and functional components of the control and address units, the correlator and the coding unit, the remaining components being available from industry in the form of off-the-shelf LSI-circuits.

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4K MEMORY UNIT BASED UPON PLANE MAGNETIC DOMAINS

Moscow MODELIROVANIYE I OPTIMIZATSIYA SLOZHNYKH SISTEM UPRAVLENIYA in Russian 1981 (signed to press 8 Jun 81) pp 247-250

[Article by S. I. Kasatkin from collection "Modeling and Optimizing Complex Control Systems" edited by Ya. Z. Tsypkin, USSR Academy of Sciences, Izdatel'stvo "Nauka", 2350 copies, 265 pages]

[Text] The device here proposed is a memory unit on plane magnetic domains, the memories on which are being developed by the Institute of Problems in Control. The magnetic matrix in which information is written, transferred and read is a thin permalloy ferromagnetic film applied to a glass substrate.

In the magnetic matrix are formed regions of weaker coercive force (channels) relative to the primary region (array). The information carriers are plane magnetic domains (PMD), which are formed, propagated and then destroyed in the low-coercivity channels. All these operations occur as a result of external magnetic fields generated by conductor systems etched in foil or wound coils. A number of methods of transferring information within the matrix have now been proposed, and each naturally has its drawbacks and advantages. The method upon which is based the device proposed here offers the following features: high information density, high operational clock frequency, lower power consumption, no wound shift coil, simpler conductor and matrix topology and, accordingly, greater technological efficiency and ease of integration. The open registers, which require the rewriting of information read, must be considered a drawback. Its basic elements include write selection, domain shift and read selection. These operations are described below.

General description. The chip consists of a magnetic matrix on a glass substrate with two layers of conductors on two-sided foil integrated with the matrix. All of this is contained in a standard package.

Chip capacity	4 kbits	Maximum input (f = 50 kHz)	4 W
Number of registers	32	Maximum current	600 mA
Length of 1 register	128 bits	Redundancy	5-fold
Maximum clock frequency	50 kHz	Read signal	1 mV
Maximum data-transmission speed	1.6 mbit/s	Package dimensions	30X48 mm^2
Number of contacts	46	Substrate dimensions	30X46 mm^2

The registers are open; reading therefore requires rewriting. Information is preserved when power is disconnected.

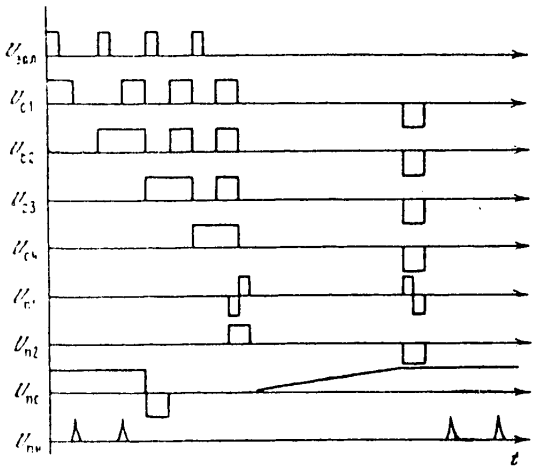
A method similar to the Broadbent method is employed to shift domains in the matrix. It consists in the following: it uses two layers of conductors having the form of a meander and shifted relative to one another the width of one conductor. Selection of the pulse sequence makes it possible to obtain unidirectional domain movement while generating traveling waves of the transfer and erase fields along the channel.

Let us assume we have a domain in a low-coercivity channel and equal in length to the width of two buses. If we supply a positive pulse to the 1^+ bus and a negative pulse to the 2^+ bus, the part of the domain under the 2^+ bus is erased; the part of the domain under the 1^+ bus is preserved and the domain is shifted under the 2^- bus (in this part of the 2^- bus the current has the opposite direction because of the shape of the conductor). The domain is not shifted further, since the magnetic field in bus 1^- holds the domain. We see after the 1st cycle that, having preserved its dimensions, the domain has been shifted one bus width. The second cycle requires negative pulses to buses 1^+ and 2^+, the 3d cycle a negative pulse to bus 1^+ and a positive pulse to bus 2^+. Finally, in the 4th cycle positive pulses are supplied to both buses 1^+ and 2^+. This is a 4-cycle system.

The chip has 32 registers. Write-read selection is employed because of the large number of contacts and the impossibility of accommodating 32 induction read coils. All registers are combined into groups of 4. For each group there is 1 write bus and 1 read coil.

Four selection buses (for the entire chip) are required for read selection. This works as follows. Write and selection bus currents are selected such that to write a domain in a channel is possible only if the currents in both buses coincide (the selection bus lies above the write bus). The topology of the channels is such that the domain write regions are shifted with respect to one another within each group of four; above each write region is only one selection bus and a common write bus for the group as a whole. Immediately behind the selection buses are the shift meanders. For clarity's sake let us designate the selection bus nearest the meanders S1, the one behind it S2 etc. Domain write occurs initially in the register above which lies an S1 bus. A positive pulse is supplied to S1 (see figure). If 1 is to be written, a positive pulse is supplied to the write bus. The points coincide, and the domain, which constitutes an informational unit, is written. If 0 must be written, no pulse is fed to the write bus and the domain is not written. This channel state corresponds to an informational null. Nothing occurs in the remaining registers, since in these registers the write bus does not coincide with S1. A positive pulse is then fed to S2 as well. The write bus functions in the same way as described above. Information is written in the 2d register. Once again, nothing changes in the remaining registers. Following termination of the write pulse a positive pulse is fed to S1 (the pulse continues to give effect in S2). By the pulse supplied to S2 the domain reaches the shift meanders. In the 3d cycle a positive pulse is fed to S3, while following the termination of the write pulse positive pulses are supplied to both S1 and S2. In the 4th cycle, a positive pulse is fed to S4, while following termination of the write pulse positive pulses are fed to S1, S2 and S3. Then, as the domains reach the regions of the shift meanders, shift pulses are supplied to these meanders. The magnetic fields draw the domains under the buses, that is, the information-transfer process now begins.

As has been pointed out above, 1 group of registers (4 registers) has 1 read coil. Read signals are selected by means of the difference in the length of the channels from the meander to the read coils and, accordingly, by the different path traveled by the domains in the different registers of the group. (The read signal is induced in the read coil by the demagnetizing fields of the top of the domain; it is therefore clear that the presence of the signal corresponds to 1, its absence to 0.) The delay time between



signals on one coil is approximately 2 μ and may vary in either direction. Induced in the read coil each cycle is a packet of four pulses, each of which lags behind its neighbor by some 2 μs.

The magnetic matrix consists of direct low-coercivity channels expanded to write and read domains. Each register comprises 5 identical channels, which makes it possible to increase the read signal and enhance the operational reliability of the device, since it will still be able to function with faulty channels. (The read portions are separated.) The low-coercivity channels are 25 μ wide.

The layer of conductors nearest the matrix consists of write buses, a shift meander and read coils. This layer has 34 contacts. The repetition interval of the meander buses is 300 μ

The second layer of conductors has selection buses, a shift meander and a read shift and erase coil. This layer has 12 contact area. Their dimensions are approximately 1 mm.

Part of the foil is bent aside so as to destroy the vertical component of the shift magnetic field in the read coil, which produces interference. The topology of the coil is such that this bending forms two identical portions with vertical components of opposite directionality.

The chip has 15 control circuits: 8 write circuits, 4 selection circuits, 2 shift meanders and 1 shift coil for reading. There are 8 read channels functioning simultaneously. In addition to the write circuits, each circuit requires the generation of doublet pulses up to 0.6 A in amplitude. A pulse diagram for f = 50 kHz is shown in the figure. To function the chip requires 8 read amplifiers with a sensitivity of 0.5-1 mV.

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SOFTWARE

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FOKAL-1975 ALGORITHMIC LANGUAGE INTERPRETER FOR SARATOV-2 COMPUTER

Leningrad ORGANIZATSIYA VYCHISLITEL'NYKH STRUKTUR I PROTSESSOV: PROYEKTIROVANIYE SISTEM VVODA-VYVODA EVM in Russian No 8, 1981 (signed to press 31 Dec 80) pp 34-41

[Article by P. G. Kolin'ko, "FOKAL-1975 Interpreter of FOKAL Algorithmic Language for SARATOV-2 Computer", from collection "Organizing Computer Structures and Processes: The Design of Computer Input/Output Systems", edited by Z. I. Tsar'kova, Izdatel'stvo Leningradskogo universiteta, 2449 copies, 184 pages]

[Text] Introduction. The FOKAL-1975 interpreter is an improved modification of the FOKAL-1969 interpreter and the FOKAL-8K version of it which has been developed to maximize exploitation of the capabilities offered by the SARATOV-2 computer:
individual devices to control the high-speed punched-tape reader, tape punch and i/o via an electric typewriter;
an auxiliary arithmetical unit performing the operations of fixed-decimal multiplication and division;
an internal storage capacity of 32K words (eight fields).

The individual addresses for exchange with the punched-tape reader, tape punch and electric typewriter, which make it difficult to operate the FOKAL-1969 interpreter with the SARATOV-2, are used in the FOKAL-1975 to organize the simultaneous operation of these devices.

With comparatively minor modifications in the unit interpreting floating-decimal operations, the auxiliary arithmetical unit has made possible substantial reductions in computing time, reaching 40 per cent in the case of some tasks.

The internal storage capacity, which has been enlarged eight-fold as compared with earlier models of the SARATOV computer, makes it possible to allocate individual 4K-fields not only for the FOKAL program, as is done in the FOKAL-8K interpreter, but also for the variable table and the set of programs interrupting and operating the computer's external devices. The volume of the variable table in the FOKAL-1975 interpreter can thus be enlarged to 817, that is, more than four-fold as compared with the FOKAL-8K. The place freed in the memory field occupied by the FOKAL interpreter has been used to augment the capacity of the latter.

Work on improvement of the FOKAL interpreter has proceeded in three directions:
1) expansion of the input language;
2) modernization of the set of programs handling interruptions with a view to more efficient utilization of the external devices of the basic system;
3) providing a capability for unlimited extension of the number of service peripherals, means of processing information from them etc. without intervention in the interpreter (an "external function" device).

The FOKAL-1975 interpreter may be operated with the SARATOV-2 or an analogous computer with an internal memory capacity of at least 16K in the absence of external functions, at least 32K with use of the latter; the set of i/o devices includes the electric typewriter (address 03 for input, 04 for output, the high-speed reader (address 01) and the tape punch (address 02).

For full utilization of the capabilities of the interpreter it is also desirable to have an alphanumeric plot printer (ATsPU) (address 66) and a timer with a 0.2 s pulse transmission frequency (address 15).

The interpreter capabilities and features described below are given in accordance with the version of this device dating from 25 July 1977.

Expansion of input language. The input language of the FOKAL-1975 interpreter has been expanded over that of the FOKAL-1969 by introducing an auxiliary operator L in twelve modifications and additional control symbols and capabilities in a number of other language operators. Program compatibility was insured so as to permit programs prepared for the FOKAL-1969 interpreter to be executed by the FOKAL-1975 without any modifications. The following are the major modifications and additions to the input language:

a) modifications making it more convenient to work with the interpreter. These include: operator L:, which cuts off the computer's colon print with number input by operator ASK; operator L=, which cuts off output of the equal sign with number print by operator TYPE; a capability for printing parts of the variable table, which is provided by operator T$A, where A is the name of the variable (with index, perhaps) beginning with which the table is to be printed; a capability for translating lines of the electric typewriter print without return of the carriage, which is delayed by the control symbol # in operator TYPE or ASK and a capability for preserving a previous variable value by executing input operator ASK. Rather than inputting a number, this now requires input of the symbol "TABULATOR" and the interpreter prints out the value of the stored variable in the operative format; if operator ASK inputs a number, the interpreter will ignore all symbols up to the first decimal point, digit or "minus" sign; the FOKAL-1969 interpreter, on the other hand, accepts these symbols as an input boundary and takes zero as a variable, and it is impossible to correct an error without repeating the execution of operator ASK from the beginning. This capability offered by the FOKAL-1975 interpreter not only neutralizes the effect of extended user error due to the printing of numbers in the wrong register, but also permits the input from punched tape of numbers supplied it by operator TYPE. Operator L N is used to establish the number input mode to be employed in the FOKAL-1969 interpreter, which is necessary to input information in text form; operator L (without suboperators) supplies the electric typewriter the current storage allocation of the FOKAL program and the variable table; the symbol "TRANSLATE LINE" must be entered twice to print a line to the end while working with operator MODIFY. The new number which will be assigned the line in storage may be printed in the space between the two translations of the line. The line with the former number in the form in which it was before it was changed is at the same time preserved in program storage. This makes it possible to renumber lines, reproduce them, divide them into parts etc;

operators L, D and W may each have a number of arguments divided by commas, which is equivalent to executing a sequence of operators with one argument. When the program lines and line groups indicated in it are fed to the keypunch machine, the operator W 2, 1.3, 8.4, 17 thus formulates the output in the form of a single region set off by an asterisk, whereas operators W 2; W 1,3; W 8.4; W 17 cannot, first, be written in a single line and second, they formulate the output in the form of four separate regions;

b) Timer operation. The timer is controlled by the operators
L Z - time counter reset;
L T - time counter print and
L T A - assigment of current time value in seconds to indicated variable A.

The time counter is operated by the program handling interrupts from the timer. The counter functions only when the interpreter performs calculations in accordance with the program and stops if the interpreter is waiting for a free output or the next instruction from the user;

c) Actual-output unit setting. The FOKAL-1975 language has no special means of supplying information to any unit other than the electric typewriter. But by switching the address of the actual output, the operators controlling output to the electric typewriter will supply information to other units of the computer system.

The following operators are used to switch these units:
L P - set output to keypunch machine;
L A - set output to alphanumeric plotter;
L D - set output to display (reserve);
L K - set output to electric typewriter with simultaneous cancellation of the result of operator action L =,L: and L N (see above).

Regardless of which of these devices has been designated the output unit, the electric typewriter will be supplied an echo print of input information, an asterisk indicating transfer of control to the user, a colon indicating anticipation of number input by operator ASK; results of MODIFY operator functioning and information that computation has been interrupted because of user error.

Following a report of information on an error, the electric typewriter will always be the actual output unit.

Operators L K and L A have modification L K n and L A n, where n is a whole decimal number and regulate the width of the print field for n positions. If n is not specified the field is set for the standard width: 80 symbols for the electric typewriter, 64 symbols for the alphanumeric plotter;

d) Access to external functions. This is controlled by the operators
L R name (arguments) or
L W name (arguments). These are described below in a separate section.

Interrupt handling. A set of interrupt-handling programs services the peripheral devices of the basic computer system. Information is exchanged with all peripheral devices via cyclic buffers specially allocated in internal storage. When information is transferred to several buffers, the corresponding components function simultaneously. When information is fed to the electric typewriter and alphanumeric plotter, a count is made of the number of symbols printed in a line. If the number of symbols exceeds the width of the print field, they automatically advance to a new line.

Timer operation consists in adding the value of the timer interval to a special counter recording the expenditure of machine time. The computer reacts to interruptions from the timer only if it is performing program calculations. An interrupt from the timer is blocked during waits for a peripheral unit to be freed in the case of buffer overflow or for instructions from the user. Time counter capacity is approximately 37 hours.

During the processing of input from the electric typewriter, the program handling interrupts identifies and processes the directive symbol codes. Directives are given from the electric typewriter in the form of Latin-register letters with the "kontrol'" key depressed. In addition to the kontr./s directive, which indicates an interruption of calculation from the control console, FOKAL-1975 also accepts the following directives:
1) Kontr./S - determine status of computer.
The machine prints information on its status at the moment the directive is given:
SChET - program computations;
STOP - awaiting user instructions;
ATsPU - hung up on ATsPU flag query; awaiting free ATsPU buffer;
PFL - same - for PFL [tape punch].

Printed in the line following one of these reports is the number of the program line to be executed and the last symbol scanned in this line. The directive permits determination of the status of the machine without interrupting computation;
2) Kontr./Z - (equivalent to operator L Z);
3) Kontr./T - print time counter contents (equivalent to L T);
Kontr./P - start tape punch;
Kontr./A - start alphanumeric plotter.

The last two directives are used in the case of hangup in querying the flag of the corresponding units, which frequently occurs when they are switched on in the process of interpreter operation.

The interrupt-handling program also identifies unrecognized interruptions with printout of the addresses of the units corresponding to them, resets flags and inhibits interruption from all peripheral units except system components and controls the restart.

Together with the facilities for expanding the FOKAL language, the interrupt-handling program permits the functioning of the interpreter without any correction of its contents from the computer console. This is a condition necessary for several users to use the FOKAL-1975 interpreter in the time-sharing mode, which requires only the replacement of several blocks of the interrupt-handling program.

External functions unit. The unit connecting external functions is the most important and essential feature of the FOKAL-1975 interpreter, one making it indispensable for automating scientific experiments with external devices developed for use with the Saratov computers and machines identical to them. With a minimum of limitations and given certain arrangements for communications, the external functions unit permits users to compile and switch to the FOKAL-1975 interpreter programs providing exchange of information with the widest variety of units and exploit the full potential of FOKAL language to compile programs to process information obtained from these devices.

The FOKAL program makes external functions available with the use of the operators
L R name (argument 1, argument 2, ..., argument n) or
L W name (argument 1, argument 2, ..., argument n).
The number of arguments is arbitrary, but it will be not less that 2 and no greater than 22. The first argument must be a variable (with or without index). It is the first component of the exchange file. The second and subsequent arguments must be expressions. A zero argument may be omitted and only the comma following it retained. The second argument gives the number of elements in the exchange file. If it equals zero, the exchange file consists of a single element. When operator L R calls up a function, the exchange file is transferred from a special buffer zone to variable-table storage (read function); with a call by operator L W it is transferred from variable storage to the buffer zone (write function). The FOKAL-1975 interpreter handles both forms of access in an identical manner in all other instances as well.

The name of the function, consisting of any electric typewriter symbols, with the exception of the signs for arithmetical operations, spaces, brackets, periods, commas and equal signs (expression limiters), is converted to a 12-character binary code, which is transmitted to the first cell of the argument buffer. Values of the second and subsequent function arguments are transferred to the remaining cells. As are the elements of the exchange file, these values are transmitted in a form with a floating decimal point in another code. The interpreter analyzes neither the name of the function nor the meaning of the arguments. After transmission of the arguments (and for the write function, of the exchange file), control is transferred to the first cell of the zone of external function mediums, where must be initiated the program identifying the name of the function and transferring control to it. Two interpreter inputs are provided for return from a functional medium: one for normal return, the other for emergency return. In the case of normal return, the interpreter accepts the exchange file (for the read function) and continues with that pass of the program. In an emergency return the interpreter gives the standard error message. The program executing the external function must transmit a code symbol via the computer accumulator, which will be printed on the electric typewriter and serve to specify the error detected. In particular, if the function called up is not on the list of those available in memory, the code for symbol Z must be transmitted to the interpreter.

One of the names reserved for a null function is the name ARR. When it finds this name the name-recognition program should immediately return control to the interpreter. The functions L RARR (name, quantity) and L WARR (name, quantity) thus generated enlarge interpreter capacity. They can be used to provide functions employing the exchange file as both input and output information. Buffer exchange-file storage may also be used to expand variable-table capacity, to store information when the variable table is erased, to rename files, to reduce two files to one and vice versa etc.

The greatest limitation imposed upon the use of external devices in external-function mediums is the need to take into account the specific nature of the operation of the computer interrupt system: any device which can cause interruption must be serviced during an illegal interruption. After leaving the external function the interrupt must be permitted, while the device is brought to a state in which it cannot cause interruptions. Use of basic system components is not recommended.

The interpreter places two subprograms at the disposal of developers of external function programs: one for output of a symbol for actual output and one for freeing output buffers. The latter program has to be called up if interruption has to be inhibited for comparatively long periods of time.

To identify possible departures from the interface convention on the part of external function library developers, the interpreter provides a capability for diagnosing the correctness of store-indicated transfers and an instruction to stop at the first cell of the interpreter memory field. A stop or identification of an illegal store-indicated transfer means that there has been an improper return to the interpreter or a malfunction of it. Departures from the rules governing use of the interrupt mode are identified by the interrupt-handling program, which prints out on the electric typewriter the address of the units causing the illegal interrupts, after which it inhibits interrupts from all units except those of the basic system.

The FOKAL-1975 interpreter described here thus substantially enhances the possibilities offered by the use of the SARATOV-2 computer, which is becoming not simply an autonomous computer, but a fairly powerful scientific research tool for developing automated control systems as well.

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APPLICATIONS

AUTOMATION OF SCIENTIFIC RESEARCH IN GEOPHYSICS

Apatity AVTOMATIZATSIYA GEOFIZICHESKIKH ISSLEDOVANIY in Russian 1980 (signed to press 26 Dec 80) pp 3-19

[Article by I. A. Kuz'min from collection "Automation of Geophysical Research", edited by Candidate of Physicomathematical Sciences I. A. Kuz'min, Kol'skiy filial AN SSSR, 300 copies]

[Text] Modern development of geophysics in the area of solar-terrestrial relations is determined by broad development of complex research at all levels of the space being studied. To understand the physical mechanisms of the origin of phenomena, the modern investigator must use all accessible types of observations of processes occurring in interplanetary space and in the earth's magnetosphere and ionosphere. Information about phenomena of solar-terrestrial physics comes from interplanetary space apparatus, from artificial earth satellites, from drifting balloons, from rockets and from ground observation points. Thus, geophysical research is related by its nature to large volumes of recorded information. Unlike physical experiments, a great abundance of received information is observed in geophysics, which inevitably occurs due to the impossibility of predicting the most important period of observations. Each phenomenon in geophysical research is unique in its nature and there is no repetition of recorded phenomena. If similar situations occur, then they develop under different conditions. The volume of data received increases continuously with regard to the fact that investigators are interested in the finer time and spatial structure of phenomena and this leads to a proportional increase of the amount of data.

The problem of digital recording and storage of geophysical data is now becoming acute. It should be noted that time-sharing of the data gathering process and data processing frequently leads to the fact that these data are not generally processed. Therefore, the problem of data gathering and processing in real time using measuring-calculating systems based on computers arises in geophysics in automation of scientific research.

The most important problem of automation of scientific research is development of operational software for all computer systems. A great deal of attention should be devoted to developing methods of numerical modelling of geophysical processes, which has recently begun to find broad application [1]. A check of models directly on data obtained during geophysical experiment is especially interesting.

Besides development of real-time information gathering and processing systems, autonomous information recorders for gathering data under field expeditionary conditions should be developed. These recorders should be used as magnetic tape information carriers and should have the capability of processing this information with a high time-transformation factor at the regional center [2].

The problem of tying measurements to a single accurate time is of important significance to the entire automated data gathering network.

Existing systems for automation of experimental investigations. There are now different versions of organization of systems for automation of scientific research of large academic institutes. An example of the branched structure based on a multimachine complex is the Collective-Use Experimental Computer System (EVS KP), Latvian SSR Academy of Sciences, which is a multilevel hierarchical system that combines programming and specialized macro-, mini- and micromachines into a unified computer complex that makes available all equipment, information support and software for collective use by scientific workers of the Latvian SSR Academy of Sciences [3]. The EVS KP consists of three main parts (Figure 1): a central computer complex, communications channels and subsystems of the institutes.

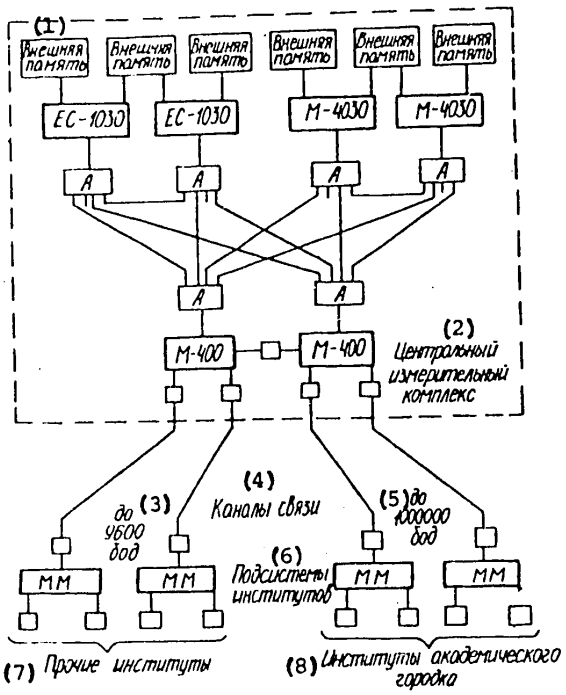

Figure 1. Experimental Collective-Use Computer System of Latvian SSR Academy of Sciences

[Key on following page]

[Key continued from preceding page]:

1. External storage
2. Central measuring complex
3. Up to 9,600 bauds
4. Communications channels
5. Up to one million bauds
6. Subsystems of institutes
7. Miscellaneous institutes
8. Institutes of Akademgorodok

The central computer complex (TsVK) includes an information-computer and buffer subsystem. The basis of the first subsystem are four macromachines: two YeS-1030 type computers and two M-4030 ASVT [Modular system of computer technology] type computers. The presence of these two types of computers permits the system nucleus to work with any type of operating systems or even with two operating systems simultaneously. The capability of the M-4030 computer to work both with the DOS [Disk operating system] of the ASVT and the OSES [Operating system of the unified computer system] provides this possibility. The buffer part of the complex consists of two minimachines of type M-400 and makes connections through the communications channels of the institute subsystem. The macromachines are joined to each other by the common field of the external storage and to the buffer minimachines by means of special multichannel adapters (A).

The communications channels (KS) are divided into two groups: high-speed over telephone lines with twisted pairs at a distance up to 3 km at transmission speed up to one million bauds per second and low-speed over ordinary telephone subscriber channels with speed of 9,600 bauds per second over any distance.

The institute subsystems are the lower level of hierarchy of the EVS KP and are developed on the basis of mini- and micromachine complexes (MM). Connection is made to the central computer complex through communications channels. Any institute subsystem can also utilize all the capabilities of the central computer complex. It may consist both of a simple user console with display and of a multimachine complex of mini- and microcomputers. The main characteristic of the lower level is the obligatory presence of the dialogue mode between machines and users, which permits the user to effectively work with the complex directly without excess expenditure of the machine time of the central computer complex. The importance of this mode is that it ensures efficient use of the creative capabilities of the users and the logic, information and computer capabilities of a large system and eliminates intermediaries between the investigator and computer equipment--operators and programmers. As indicated by practice, a dialogue is extremely effective in practice in all problems at any level (debugging, calculation checking, printout of results and interpretation and so on).

The multimachine system of the LIYaF [Leningrad Institute of Nuclear Physics], USSR Academy of Sciences, is also organized on the hierarchical principle [4]. The first measuring-computer multimachine complexes were put into operation in 1969. A design for a multimachine automated complex has now been developed and introduced. The project will require 8-10 years for total fulfillment. The substitution for new computer equipment is also proceeding by evolution, i.e., already existing multimachine systems will be included as users of new systems to support operations during the transitional period.

The multimachine automated complex being designed will also have a hierarchical structure with the capability of even greater autonomy of collective-use multimachine laboratory systems (SKP) that service experiments in the basic directions of fundamental research at the institute. All the SKP will be connected through a computer-concentrator to the main computers of the complex (BESM-6 and YeS-1060 computers). Each SKP includes remote measuring stations (UIS) and terminals for operational work with data banks (TOP). A typical UIS consists of mini- or microcomputers, integration apparatus in the CAMAC standard and information display devices. An example of a collective-use system based on the M-4030 ASVT is the SKP for servicing experiments conducted using a type VVR-M type reactor (Figure 2). The existing system (IVTs-67) that supports a group of experiments in nuclear physics and solid-state physics has been connected directly to the baseline computer. The measuring stations (UIS) are connected to the baseline M-4030 computer by apparatus in the CAMAC standard and a buffer minicomputer of type M-400. This organization of communications with the lower level of the system is independent of the type of computer of the remote station and provides the capability of easy expansion of the system. A subsystem based on the YeS-1010 computer is designed for input and editing of information related to the activity of the data center of LIYaF.

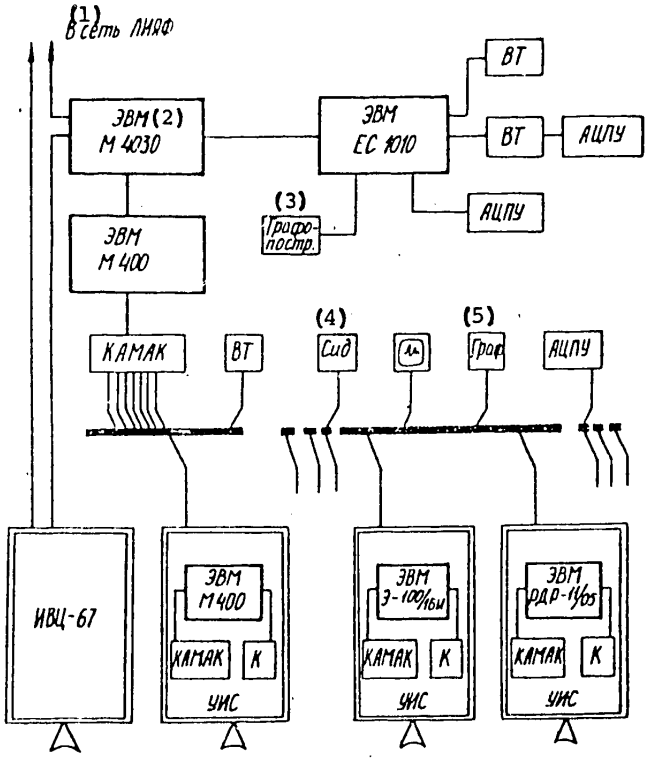

Figure 2. Collective-Use System of Neutron Research Laboratory, Leningrad Institute of Nuclear Physics, USSR Academy of Sciences

[Key on following page]

[Key continued from preceding page]:

1. To LIYaF network
2. Computer
3. Graph plotter
4. Sid
5. Graph

The automatic scientific research systems of the Physics Institute, USSR Academy of Sciences, are constructed on this principle [5, 6]. The computer system is created on the basis of a mini- and microcomputer network without the use of a central computer complex based on macrocomputers. All the processors of the system are equivalent and calculations are exchanged and organized through an exchange mainline by communications controlled by special processor. A model of the system for automation of large research installations, where the two remote subsystems constructed on the principle of a sequential ring mainline are shown, is shown in Figure 3. The message exchange mainline and sequential ring mainline were realized in the CAMAC standard. The processors of individual subsystems are connected to each other on the "driving-driving" principle, thus forming a multiprocessor system operating with a common user field. The computer resources are distributed by sequential data-transmission mainlines. The considered model is the basis of the design on which a system for automation of the powerful laser installation Del'fin was developed at FIAN [Physics Institute imeni P. N. Lebedev, USSR Academy of Sciences] to investigate problems of thermonuclear fusion [7].

The principle of constructing the typical structure of scientific research automation complexes based on the use of a standardized machine-independent mainline information exchange system (UMSO) between the computers, specialized external devices and experimental data gathering equipment contained in the complex [8, 9] was developed at the Institute of Automatics and Electrometry (IAiE) and the Special Design Office for Scientific Instrument Building (SKB NP), Siberian Department, USSR Academy of Sciences. The UMSO consists of a communications processor that supports interaction between users. Each user is represented in the UMSO by a standardized user controller and by his own user interface. The system functions on the "request-answer" principle in the systems-user controller interaction mode. According to [9], the use of the UMSO has the following advantages:

adoption of the machine-independent standard made it possible to limit oneself to development of a single version of the system structure;

use of the UMSO makes it possible to simplify development of systems software since any of the computers contained in this system regards the entire aggregate of remaining components as a single active external device, the rules of exchange with which have been standardized;

the use of UMSO to organize multimachine complexes permits step by step development of systems with gradual build-up of specialized equipment and software;

the system is "homogeneous" in hardware with data gathering systems fulfilled in the CAMAC standard since it utilizes the design principles of this standard.

Extensive investigations on automation of geophysical information gathering and processing are being conducted at the Kaliningrad Observatory of IZMIRAN [Institute

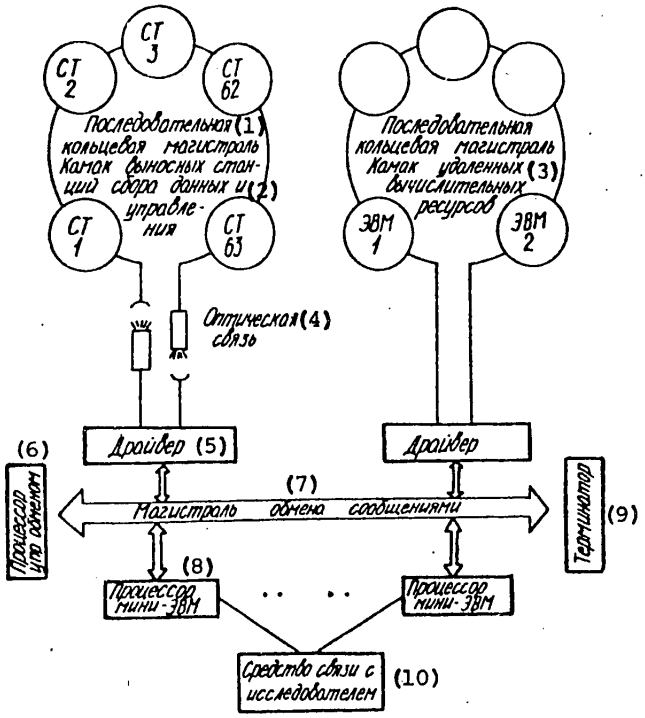

Figure 3. Model of Automation System of Physics Institute imeni P. N. Lebedev, USSR Academy of Sciences

Key:
1. Sequential ring mainline
2. CAMAC portable data gathering and control stations
3. CAMAC of remote computer resources
4. Optical communications
5. Driver
6. Exchange control processor
7. Message exchange mainline
8. Mini-computer processor
9. Terminator
10. Device for communicating with investigator

of Terrestrial Magnetism, the Ionosphere and Radio Wave Propagation, USSR Academy of Sciences] [10, 11]. The KIM IZMIRAN ionosphere diagnostic complex (IDK), which is based on two YeS-1010 and YeS-1020 computers, has been developed there. The designation of the IDK is partial or complete automation of such processes as digitization and entry of the data from complex sensors into the computer, filtration, spectral and correlation analysis of signals, calculation of convolutions, threshold processing and control of data gathering and processing, observatory service for standard processing of observational data (calculation of indices and generalized parameters), calculation of diagnostic parameters on the converted

signals of sensors and preparation of measurement results for comparison to calculations. The IDK includes a measuring complex of sensors, observational data gathering and computer-entry device, a computer and its software.

Purposeful work was begun in 1973 on automation of scientific research at the Arctic Geophysics Institute. The experimental geophysical information gathering, processing, storage and operational printout system LANI-1 (Laboratory for Automation of Scientific Research) was developed as a result of the investigations [12, 13, 14]. The system consists of a real-time geophysical information gathering and preliminary processing subsystem based on the Nairi-3 computer. Modernization of this real-time subsystem is described in [15]. The second subsystem, designed for information storage, sorting and recording to the geophysical data base, was realized on the basis of the Ruta-110 computer complex. The system was connected to the user channel of a long-distance line through a data transmission multiplexer which was contained in the complex and could be connected to terminals, as which teletypes were used. The number of terminals could be brought up to 30. The processed geophysical data could be printed out on request in the form of tables and graphs. The Ruta-110 computer complex has now been replaced by a more powerful M-4030 computer and a regional center for geophysical data gathering and processing has been developed on its basis, which will be discussed in more detail below.

The system for real-time observation of phenomena in solar-terrestrial communications SELDADS, developed in the United States, is of great interest [16].

SELDADS (The SEL Data Acquisition and Display System) is a space laboratory data gathering and display system. The system itself and the information sources are shown in Figure 4. A large information flow about the parameters of interplanetary space and the earth's magnetosphere come in from satellites of the SMS/GOES system, ITOS and TIROS-N weather satellites and from satellites of the SOLRAD HI program. Part of the information arrives by telemetry directly to the laboratory, is decoded,processed in real time and entered into the data base of the system. Data on the network of magnetometers operating by the MIM program are transmitted to the system via weather satellites. Messages about solar activity in the optical and radio band come in directly from observatories. Data on high-latitude stations on the components of the geomagnetic field are also transmitted from a network of riometers by teletype every 15 minutes. Both special air force communications systems and ordinary commercial channels are used for data transmission. All data come into the computer system of the data base, which performs all functions of information gathering, processing, storage and display both directly to the duty operator of the forecasting center and to remote users over communications channels.

The data base computer system consists of three computers. Two minicomputers of type Nova-1200 joined to each other by a special multiprocessor communications adapter is used to gather data and to organize the real-time data base. Each computer has an internal storage with capacity of 32 K words, magnetic disk external storage with capacity of 58 megabytes and a nine-track magnetic tape store. Both computers have the capability of data transmission and reception over telephone and standard telegraph communications channels. The basic language for the external users of the system connected through communications channels is BASIC

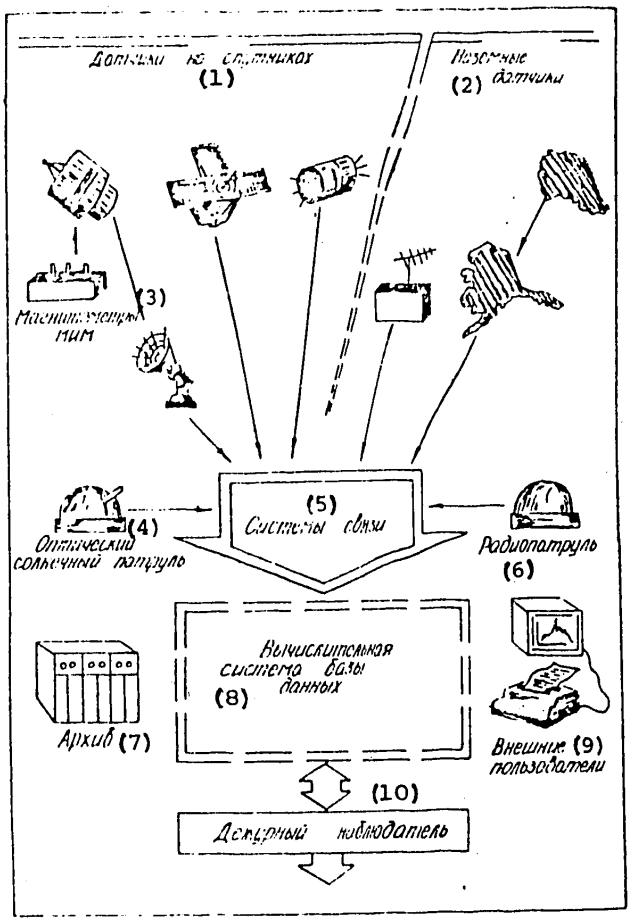

Figure 4. Data Gathering and Display System

Key:

1. Sensors on satellites
2. Ground sensors
3. MIM magnetometers
4. Optical solar patrol
5. Communications systems
6. Radio patrol
7. Archives
8. Data base computer system
9. External users
10. Duty observer

programming language. The third computer is compatible in language and data formats with the NOVA-1200 minicomputer, but has expanded arithmetic due to realization of operations with floating decimal by the schematic method, higher speed, larger internal storage and a large set of information display devices. This computer is designed for organizing work by different users with the data base. It is used to display information on displays, to print tables, to display information in graphical form and also to print out information to remote users over communications channels. Communications with a large computer system based on computers of CDC 6600 type are maintained through a third computer.

The entire system functions in the following manner. Information on different communications channels comes into the system in real time. After preliminary processing, the information is fed to a data base (BD) and is simultaneously recorded on magnetic tape in the data archives. A specific lifetime of the data in the data base, during which data can be obtained operationally both directly in the forecasting center and over communications channels, has been established for each type of data. The one-minute values of data are usually stored for four days and five-minute and higher values are stored for one calendar month. At the end of this deadline, the data can be obtained only through the archives with a time delay. Formats for printing out data and methods of data display on paper, teletype, on a display screen and so on have been developed for all types of data.

Structure of the system for automation of scientific research at the Arctic Geophysical Institute. Taking the specifics of geophysical research, the experience of developing experimental and geophysical information gathering and processing systems and recommendations of the Council on Automation attached to Presidium of the USSR Academy of Sciences into account [17], a project for automation of scientific research was developed at the Arctic Geophysical Institute, Kola Branch, USSR Academy of Sciences. Selection of the structure of the automation system for PGI [Arctic Geophysical Institute] is related to the configuration for location of automatic facilities. The geophysical observatories and observation stations of PGI are located tens and hundreds of kilometers from each other and from the regional center. A subsystem consisting of measuring-computer complex designed for gathering, preliminary processing and display of recorded information in real time, has been established at each observatory and complex observation station due to the absences of special communications equipment between these stations to transmit digital information at a high speed. Operational information is transmitted over a standard telegraph subscriber channel (AT) to the regional geophysical data center upon the initiative of the regional center. The main volume of geophysical data comes into the data base of the subsystem on magnetic disks and is recorded on magnetic tape. The entire volume of data is transmitted to the regional center by transmission of magnetic tape during specific periods. Each information gathering subsystem can store all the data on magnetic tapes (the subsystem archive) and has operational access to the data base of the subsystem, the period of data storage to which comprises one week (a different storage period can also be selected). Thus, the researcher, being in the observatory or at the observation station, has the capability of analyzing the data coming in both in real time and all the data received up to this moment of time. Any data stored in the subsystem can be transmitted operationally from the regional center when required and the amount of data is limited only by the carrying capacity of the telegraph channel. Thus, for example, the telegraph channel must be occupied for one minute to transmit the minute values of the hourly interval of a single magnetic field component; the daily interval is transmitted within 24 minutes and so on. Instructions to convert the subsystems to other information gathering modes and to transmit them to the regional center can be transmitted to the subsystems over the same channel at the initiative of the regional center. There is also the capability of transmitting information from a central data base upon the initiative of the subsystem, but the priority of communications remains with the regional center. A version of service and scientific information exchange is possible between subsystems over the same subscriber telephone channel. It is desirable to have two subscriber telegraph channels in each subsystem but this is not obligatory.

The regional center is constructed on the basis of a multiprocessor complex joined by means of a standardized information exchange mainline where all machines play the part of equivalent partners. The regional center has minicomputers to provide communications with subsystems over subscriber telegraph, minicomputers with external magnetic disk and magnetic tape storage for organization of the data archive and the central data base (TsB), minicomputers for decoding and processing of telemetry information coming from drifting balloons and satellites and also to digitize and enter information into the central data base from autonomous information recording devices and other digital devices (for example, digitizers or devices for reading information from movie film) and medium- or high-productivity computers to carry out calculating operations on data, for numerical modelling and for working in a collective-use system and so on. The regional center should have good information display equipment both in alphanumeric and in graphical displays, on graph plotters and on digital printers.

The hardware of the system. A survey of existing systems for automation of experimental information gathering showed that apparatus in the CAMAC standard is most promising and simplest to use for these purposes. Taking the requirements placed on the experimental information gathering and processing system into account, serially standardized measuring-computer complexes (IVK-1 and IVK-2), which contain a full set of minicomputers of the SM-3 or SM-4 type and apparatus in CAMAC standard already integrated with computers, were developed and produced [18]. Software which consists of the following parts is delivered together with the complex:

papertape operating system (PLOS);

disk operating system (DOS) with Fortran-IV, Assembler and Macroassembler programming languages;

real-time disk operating system (DOS RV) with program preparation in Assembler, Macroassembler, Fortran-IV and real-time Fortran and so on;

software for access to CAMAC modules.

A typical CAMAC crate contains the following functional modules:

input register (type 305) that permits entry of digital information in parallel code;

output register (type 350) that permits output of digital information to any device;

analog-digital converter (type 711) for entry of analog information into the complex;

digital-analog converter 2TsAP10 for output of information in analog form, for example, on a graph plotter or automatic recorder;

teletype interface (type 500A) which can be used to transmit information over subscriber telegraph lines;

relay multiplxer (type 750) for connection of several analog signals to the analog-digital converter;

pulse counter (type 401);

timing pulse generator or timer and so on.

Moreover, several hundred different modules which can be used in any system have already been developed in the CAMAC standard.

The given set of modules satisfies most requirements on information converters to digital form in geophysical investigations. Thus, an information-computer complex of type IVK-1 or IVK-2 is selected at observatories and observation stations as the basis of the data gathering subsystems. The difference of these two complexes includes different productivity of the processors.

The structure of the information gathering, preliminary processing and display subsystem is shown in Figure 5. The geophysical information sensors are connected through CAMAC models. The additional external devices not contained in the IVK set are connected by special modules. The subsystem is joined to the subscriber telegraph channel by an integration module. Two magnetic tape stores (NML) and an additional magnetic disk store are connected to the complex in addition to the magnetic disk store (NMD). One (or several) microcomputer of the Elektronika-60 type, used as a specialprocessor to calculate statistical and spectral characteristics of geophysical processes, is connected by the CAMAC apparatus to expand the calculating capabilities of the complex. Incoming data are recorded on magnetic tape for subsequent transmission to the regional center and on magnetic disk for transmission to the data base of the subsystem (BD). The data stored on disk are accessible for operational review. The data storage time in the data base comprises no more than one week. The subsystem has the capability of reviewing the information data available in the base simultaneously with information gathering and also of displaying the information in the form of graphs on a graph plotter or graph display (if it is available). Moreover, information about current time and the state of the system is shown on the duty operator's display and instructions to the operator can essentially be issued.

A block diagram of a regional center is shown in Figure 6. According to the selected structure, the regional center consists of four subsystems joined to each other by a machine-independent standardized mainline exchange system (UMSO) controlled by a communications processor KP. The first subsystem based on the IVK-1 is used to organize communications and information reception from the information gathering and preliminary processing subsystems. It also exchanges information with all remote users. The second subsystem based on the IVK-2 is used for entry and preliminary processing of telemetry information through the telemetry information decoder (URTI), for processing geophysical information recorded on a slow analog tape recorder, to digitize ONCh signals, for digitization and preliminary processing of information presented on movie film and so on. The second subsystem has a direct communications channel with the telemetry information receiving station from satellites in order to process the signal during reception of the information. Installation of a minicomputer directly at the satellite information

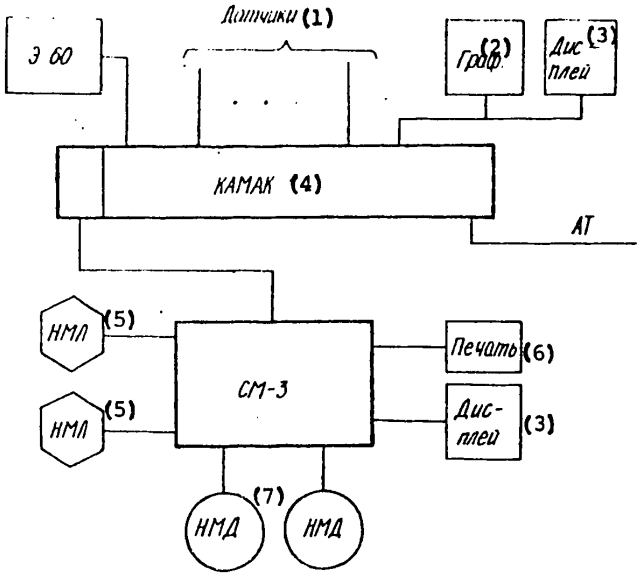

Figure 5. Structure of Real-Time Data Gathering Subsystem

Key:
1. Sensors
2. Graph
3. Display
4. CAMAC
5. Magnetic tape store
6. Printout
7. Magnetic disk store

receiving station is planned in the future. The third subsystem based on a minicomputer of type SM-1 and graph display (SIGDA) permits the investigator to work with data presented in graph form. As shown by practice, the effectiveness of analyzing the results increases when it is displayed in graph form. Historical data obtained as a result of information processing was initially presented on a digital printer and was then constructed manually and then evaluated. Graph plotters then appeared. Graph displays which in combination with a computer with sufficiently high speed display graphical information are now used extensively and they can be controlled by the operator by means of a keyboard and light pen. The required information is fixed on the graph plotters after review and correction of the data received. The fourth subsystem is based on the M-4030 ASVT and is the main computer equipment of the regional geophysical information gathering, processing, storage and display center.

Besides stationary observation stations and observatories, geophysical observations are also made under temporary field and expeditionary conditions and also in difficultly accessible locations where there is no possibility of installing automated information gathering subsystem. Autonomous magnetic tape geophysical information recorders have been developed for these purposes jointly with the Institute of Physics of the Earth, USSR Academy of Sciences [2]. There are two essentially

different methods of recording information on magnetic tape. These are recording an analog signal directly and using different methods of modulation without time quantification and recording information in digital form. Both these methods have their advantages and disadvantages. The greatest density of information recording is achieved when an analog signal is recorded on magnetic tape and as a result longer recording is possible. The accuracy of recording and time resolution can be regulated during digitization and processing of the information. The recording tape recorder is simpler in mechanical design and electronic circuits and is more reliable. The disadvantage is that a rather complex information digitizing and computer entry device is required. Digital recording of information has the advantage that it is easier to enter into the computer for processing and no special input devices are required when information is recorded on magnetic tape in a computer standard; a magnetic tape cassette need only be installed on a standard magnetic disk store contained in the computer. The disadvantage of digital tape recorders is the great complexity of the mechanical and electronic units and the fact that accuracy and time resolution are limited by the selected quantification during recording. Both directions are used at PGI in developing autonomous geophysical information recorders. A description of a slow analog tape recorder (MAM) and digital step tape recorder (TsShNML) is given in [2].

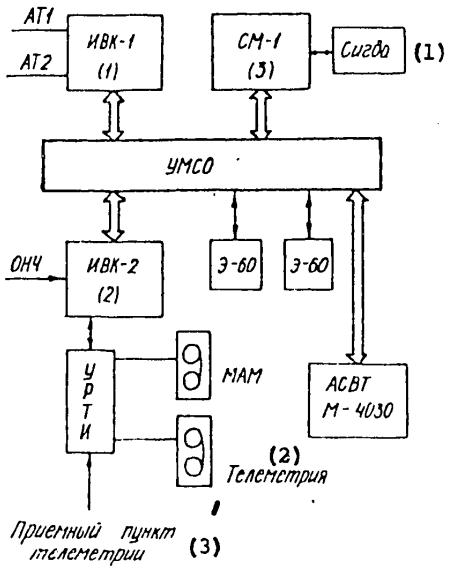

Figure 6. Structure of Regional Center

Key:
1. SIGDA
2. Telemetry
3. Telemetry receiving station

A project to automate the geophysical research of PGI is in the realization stage. A real-time data gathering and processing system based on the Nairi computer, on

which geophysical data processing algorithms are being completed, is undergoing experimental operation. A gathering subsystem based on the measuring-computer complex IVK-1 is now being developed. An M-4030 ASVT--the main computer device of the future regional center--was installed in 1978. A telemetry information decoding device (URTI) operates in combination with the M-4030 ASVT [19]. Methodical investigations are being conducted on digitization and spectral-time analysis of ONCh-signals [20]. A new camera has been developed for photographing the aurora borealis with regard to further processing of information from movie film in an information digitization and input system to a computer [21].

Development and introduction of automation systems in planned in stages by the degree of readiness of the type of observation for entry and processing of data in real time in the gathering subsystem. Existing systems will be modernized by evolution, parallel with the new system being developed prior to its being put into operation and information will be processed in the old system.

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MICROPROCESSORS IN CONTROL SYSTEMS OF ELECTRIC TRACTION DEVICES

Moscow TRUDY VSESOYUZNOGO ORDENA TRUDOVOGO KRASNOGO ZNAMENI NAUCHNO-ISSLEDOVATEL'-SKOGO INSTITUTA ZHELEZNODOROZHNOGO TRANSPORTA: MIKROPROTSESSORY V SISTEMAKH UPRAVLENIYA ELEKTROTYAGOVYKH USTROYSTV in Russian No 643, 1981 (signed to press 19 Mar 81) pp 3, 76

[Preface by Deputy Director of Institute, Doctor of Technical Sciences V. G. Inozemtsev and Head of Railway Electrification Division, Candidate of Technical Sciences A. L. Lisitsyn and table of contents from the collection "Transactions of All-Union Order of Red Banner of Labor Scientific Research Institute of Railway Transport: Microprocessors in Control Systems for Electric Traction Devices", edited by Candidate of Technical Sciences G. V. Faminskiy, Izdatel'stvo "Transport", 820 copies, 80 pages]

[Text] Microprocessors and microcomputers make it possible to automate the control of those processes in electric traction devices which were previously impossible to automate due to the extremely high cost of the equipment, its cumbersomeness and the comparatively low reliability for continuous operation. The results of investigations in this field, conducted at the All-Union Scientific Research Institute of Railway Transport (VNIIZhT) are outlined in the given collection. The advantages of using microprocessors and microcomputers for automatic control are most obvious. Therefore, basic attention is devoted in the collection to developments in this field. At the same time some possible directions for using microprocessors and microcalculators to automate the simpler production processes in electrical supply devices are investigated.

We request that comments and remarks on the materials of the collection be sent to the address: 129851, Moscow, Third Mytishchinskaya ulitsa, 10, Editorial-Publishing Department, VNIIZhT.

Contents

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REGULATING SUBWAY TRAIN TRAVEL TIME USING MICROCOMPUTERS

Moscow TRUDY VSESOYUZNOGO ORDENA TRUDOVOGO KRASNOGO ZNAMENI NAUCHNO-ISSLEDOVATEL'-SKOGO INSTITUTA ZHELEZNODOROZHNOGO TRANSPORTA: MIKROPROTSESSORY V SISTEMAKH UPRAVLENIYA ELEKTROTYAGOVYKH USTROYSTV in Russian No 643, 1981 (signed to press 19 Mar 81) pp 17-26

[Article by Candidate of Technical Sciences V. I. Astrakhan and Engineer Ye. G. Faminskaya from the collection "Transactions of All-Union Order of Red Banner of Labor Scientific Research Institute of Railway Transport: Microprocessors in Control Systems for Electric Traction Devices", edited by Candidate of Technical Sciences G. V. Faminskiy, Izdatel'stvo "Transport", 820 copies, 80 pages]

[Excerpt] Bringing actual train speed closer to the permissible speed increases the acceleration reserve compared to existing conditions. To evaluate this reserve, comparative traction calculations were made for one of the Moscow subway lines. The calculations were made on a YeS-1030 computer from a program developed at VZIIT [All-Union Correspondence Institute of Railroad Transportation Engineers] [1]. The calculated acceleration reserve time found when one-time and multiple connection of traction motors was compared in the case of fulfilling limitations on the permissible traffic speed comprises an average of 4-6 seconds per wayside.

The time expended for train traffic on the deceleration track of the station depends on the rate of the beginning of braking. Time stability for braking should be provided under intensive traffic conditions during "peak" hours by maintaining a given train speed upon coming into the station by using the ASR [Automatic speed control] subsystem. The stability of the length of deceleration does not play such an important role during hours of a load decrease. Therefore, the speed of the beginning of deceleration may be different.

Monitoring fulfillment of the train traffic schedule is easy by using microcomputers which will calculate the required train travel time under traction on a given block section, obtaining information about the time the train passes the ends of the block sections. If the length of the sections is sufficiently short when the difference in travel time with and without current is less than the permissible deviation, a microcomputer will determine the train traffic conditions over the entire section by the sign of deviation alone, i.e., it can determine only whether the train on the section is under current or is coasting in order to fulfill the programmed time of arrival at the next section.

One or several (without regard to redundancy) microcomputers, specifically microcomputers constructed on a microprocessor of series K589, can be used to control wayside travel time [2]. This microcomputer is similar in output to universal computers of type M6000 and realizes expanded arithmetic instructions and special instructions introduced by the user so that two control memory files are provided in it. The microcomputers (overall dimensions of 450 X 482 X 220 mm) contain, in addition to the processor, an interface block and also internal storage blocks, display block, power supply block and control console. The maximum capacity of the internal storage is 32,000 words and the time required to fulfill an addition operation is 3.5 microseconds. The number of input-output devices connected to the microcomputer may reach 56.

The considered multiprocessor system can be realized either as a concentrated system (all universal computers are located on a central control console) or as a distributed system (the universal computers are installed at each station while a central universal computer is installed on the central control console). The number of channels between the central control console and the stations is increased in the first version, but the following advantages appear: the number of microcomputers decreases, the capability of simple redundancy upon failure of one of the machines becomes possible, it becomes possible to organize a common memory for the multisystem using magnetic disks, which is very important during power outages and failures of the universal computer, the volume of peripheral equipment for the system as a whole is reduced considerably, the problem of documentation and monitoring of its operation is facilitated, the system servicing conditions are improved and the operational nature of introducing changes to the program and operating algorithm is enhanced.

With the second version of constructing a distributed computer system, each station central computer can control train traffic on one or several waysides based on information about actual train traffic on the wayside and information on the traffic schedule transmitted from the central universal computer. The volume of information transmitted between the central control console and the stations to control train traffic is reduced in this version and it becomes possible to use the central computer to determine deviations in train traffic by stations and to display these deviations for the engineers on a display board and also to solve other local control problems. The second version of designing a computer system achieves additional advantages when microcomputers of different capacity are used, including small computers, which may be used effectively both for control purposes and to process and transmit information, i.e., as specialized programmable microdispatchers.

Selecting a specific version for designing a multiprocessor system depends on the characteristics of the lines to be automated, their length, the scope of traffic, prospects for development and so on.

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SEARCHING FOR FRAGMENTS OF SECTION MNEMONIC CIRCUIT USING A MICROCALCULATOR

Moscow TRUDY VSESOYUZNOGO ORDENA TRUDOVOGO KRASNOGO ZNAMENI NAUCHNO-ISSLEDOVATEL'-SKOGO INSTITUTA ZHELEZNODOROZHNOGO TRANSPORTA: MIKROPROTSESSORY V SISTEMAKH UPRAVLENIYA ELEKTROTYAGOVYKH USTROYSTV in Russian No 643, 1981 (signed to press 19 Mar 81) pp 45-49

[Article by Doctor of Technical Sciences N. D. Sukhoprudskiy and Candidate of Technical Sciences V. P. Molchanov from the collection "Transactions of All-Union Order of Red Banner of Labor Scientific Research Institute of Railway Transport: Microprocessors in Control Systems for Electric Traction Devices", edited by Candidate of Technical Sciences G. V. Faminskiy, Izdatel'stvo "Transport", 820 copies, 80 pages]

[Text] The mnemonic circuit of energy sections on mosaic panels is usually fulfilled in a very simplified manner. At the same time the energy dispatcher must have the power supply circuit, number of tracks and semaphores in front of him when organizing work at stations with extensive branching of tracks. A device was developed for this purpose that reproduces in detail as needed one or another fragment of the mnemonic circuit. It includes a slide projector with line mechanism of fragment feed and control unit made on integrated circuits and transistors. Because the control unit to provide faster search for the fragment should have a memory device, data input and output device and resolving unit (that determines the difference of the numbers of the fragments and its sign), the devices was rather complex and cumbersome.

It is more effective to use a microcalculator as the basis of the control unit. It is sufficiently compact and has a built-in resolving device with microprogram control and memory registers. There should be special input-output devices to supplement it. In this case the microcalculator can be used by the dispatcher by direct designation as well (any calculations can be made if needed). Microcalculators of various types can essentially be used in the device under consideration. A description of the device (Figure 1) is given below, based on the Elektronika BZ-26 microcalculator.

The difference and its sign are displayed on a fluorescent display of type P252V in the Elektronika BZ-26 microcalculator and the "minus" sign is fixed by coincidence of the nine-digit pulses of the output register of the microprocessor and the anode M of the display. The outputs of the microprocessor to the display anodes are high-resistance; therefore, taking signals from them to avoid shunting

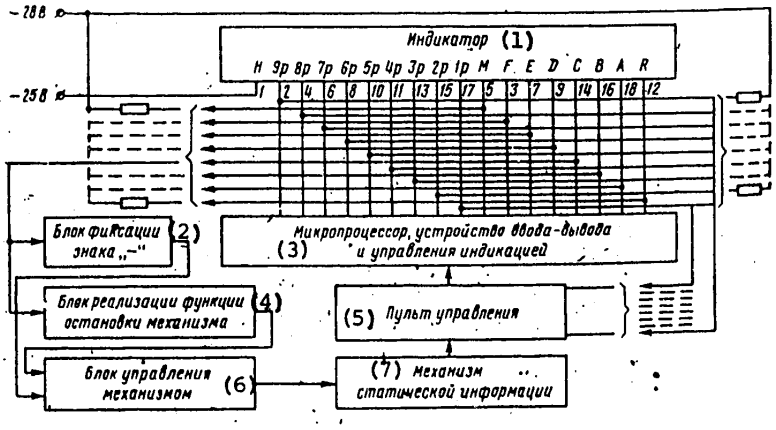

Figure 1. Energy Dispatcher Information Display Device (a) and Location of Display Anodes (b)

Key:
1. Display
2. "Minus" sign fixation unit
3. Microprocessor, input-output device and display control
4. Mechanism stopping unit
5. Control console
6. Mechanism control unit
7. Static information mechanism

of the anodes is possible only if high-resistance logic components are used. K1LB781 and K1LI781 microcircuits of series 178 were used in the given device.

A coincidence circuit of the signal from anode M and display and from the output of the ninth digit of the microprocessor register (output 9p) based on microcircuit K1LI781 is used to tap the sign "minus" (Figure 2). Since the corresponding signals of anode M and output 9p have a positive potential, they are first inverted by means of microcircuit K1LB781.

Positive pulses with length of 0.2 milliseconds appear periodically in sequence at intervals of 1.9 milliseconds at the outputs of the microprocessor register 9p-1p (see Figure 1). If segments (anodes) of the numbers at the inputs are extinguished, there are no positive pulses and a zero potential appears at output 7 of microcircuit K1LB781. The AND circuit on microcircuit 1 of K1LI781 emits a signal that authorizes movement of the "Forward" mechanism. If a positive signal appears on anode M and if the corresponding "minus" sign appears on the display screen, the coincidence circuit is triggered, issuing instructions to the mechanism control unit to move the "Backward" mechanism.

As noted above, the difference of the numbers of previously established and summoned positions must be determined to find the required fragment. This difference determines the number of steps of moving the mechanism. A one is read at each

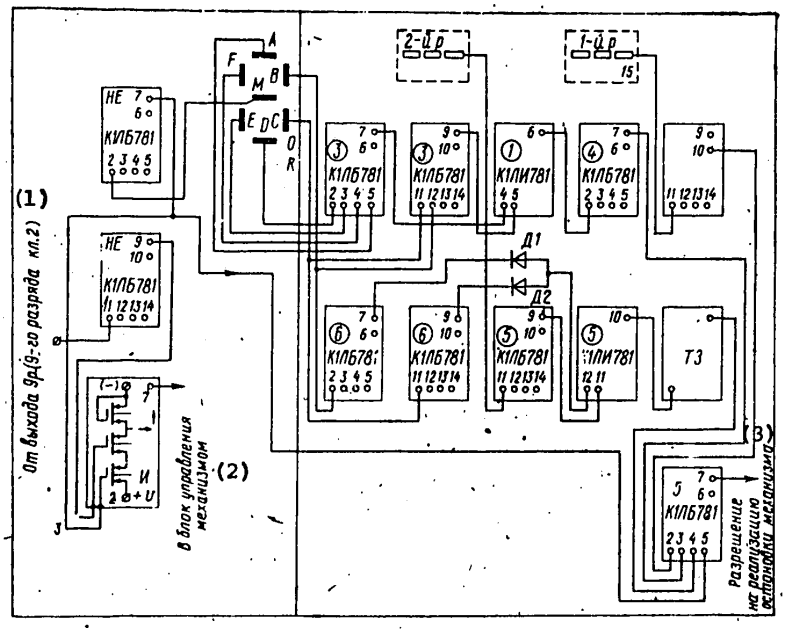

Figure 2. Diagrams of Units for Fixing "minus" Sign and Realizing Mechanism Stopping Function

Key:
1. From output 9p (ninth digit, class 2)
2. To mechanism control unit
3. Authorization for stopping mechanism

step of the derived difference during motion. The mechanism should be stopped when a zero is obtained as a result of subtracting the ones. All the display segments, with the exception of segment M (see Figure 1) which lights up when the number 8 appears, light up in the least digit. However, the appearance of the number 0 in the least digit is not a sufficient feature to deliver instructions for stopping the mechanism. It is also necessary that none of the segments be lit up (no information was reproduced) in the top digits. Thus, a prohibition to stop the mechanism should be provided both when the number 8 is displayed only in the least digit and when the number 0 is displayed together with numbers in the top digits.

Components with high input impedance--microcircuits of series 178 that perform logic functions at negative potentials--are also used in the circuits for realizing the function of stopping the mechanism (see Figure 2).

The six display anodes (with the exception of anode M) are connected to two microcircuits 3 (7) and 3 (9) that realize the OR-NOT function. The outputs of these microcircuits are connected to the inputs of microcircuit 1 (6) that perform the AND-NOT function.

When a number besides the number 0 is lit up in the least digit at the inputs of microcircuits 3 (7) and 3 (9) connected to unlit anodes, there is one or several negative potentials. Accordingly, positive potentials that prohibit the operation of microcircuit 1(6) appear on their outputs 7 and 9. The negative potential on the output is retained in this case. An authorizing positive potential appears at output 6 of microcircuit 1 only if the two negative potentials at its input coincide. A positive potential from its output is fed through inverter 4(7) to one of four inputs of the AND-NOT circuit 5(7). The second input of this circuit is connected to the input of the first digit of the display. Consequently, the forbid potentials are taken from the corresponding two inputs of microcircuit 5(7) only at the moment the pulses at the output of the first digit and at the output of microcircuit 4(7) that fixes the zero display in this digit coincide.

Instructions to stop the mechanism can be issued only if none of the numbers from 1 to 9 do not light up in the second digit. Authorization for stopping is issued by two groups of components acting on inputs 4 and 5 of microcircuit 5(7).

The first group of components is microcircuits 6(7) and 6(9); they are connected to the anodes of segments B and C of the display since some of them must be lit up if any of the numbers from 1 to 9 is lit up. The outputs of microcircuits 6(7) and 6(9) are connected through uncoupling diodes D1 and D2 that perform the OR operation to the input of microcircuit 1(10) that performs the AND-NOT operation.

Numbers are reproduced on the display by the dynamic principle. Pulse signals alternately detour the outputs of digits of 9 through 1. Simultaneously with them, signals also come into the anodes of the segments according to the number which should be reproduced in the given digit. Although the all the segment-displays of the same type in all the digits are connected in parallel, only those of them which correspond to the digit having a signal at the input coinciding with the signals at the outputs of the segments begin to light up. Therefore, a second group of components--microcircuits 5(9) and 1(10) and delay line TZ--is provided to forbid stopping of the mechanism if there is a number in the second digit. The output of the second digit of the display is connected to the second input of microcircuit 1(10) through inverter 5(9). Thus, a signal appears at the output of circuit 1(10) only if the signals on segments B and C and at the output of the second digit coincide.

Each signal arrives alternately at the inputs of the display within 0.2 millisecond. A signal initially appears at the output of the top digit and only then appears in the least digit. Therefore, to record the presence of a zero in the first digit in the absence of a number in the second digit, these two events must be combined in time, which is accomplished by means of component TZ that delays the signal from circuit 1(10) by 0.2 millisecond. An authorizing signal comes from component TZ to input 4 of microcircuit 5(7). The authorizing signal is fed through inverter 2(7) to its input 5 only if no segment of anode M lights up in the least digit (i.e., a 0 rather than an 8 is reproduced).

If the signals on all four inputs of microcircuit 5(7) coincide, a signal to stop the mechanism appears at its output, i.e., a positive pulse from the output of the unit for stopping the mechanism (see Figure 1) is fed through the control unit to

the static information mechanism. The mechanism is stopped and this completes the total cycle of switching it for finding the object.

Both the keyboard of the microcalculator and the control console with buttons, each of which corresponds to a specific object, can be used as the control console in the device.

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RECONSTRUCTING HEXAPOD GAITS

Moscow MODELIROVANIYE I OPTIMIZATSIYA SLOZHNYKH SYSTEM UPRAVLENIYA in Russian 1981 (signed to press 8 Jun 81) pp 205-216

[Article by D. N. Zhikharev and I. G. Zhestkov from collection "Modeling and Optimizing Complex Control Systems" edited by Ya. Z. Tsypkin, USSR Academy of Sciences, Izdatel'stvo "Nauka", 2350 copies, 265 pages]

[Text] 1. *Brief description of hexapod.* In this article the authors examine a number of the locomotive modes of a hexapod which has been developed at Moscow State University's Institute of Mechanics. The model of this walking machine comprises a body fitted with six legs. The legs of this machine constitute a kinematic loop with six degrees of freedom, a diagram of which is presented in Figure 1. A leg's first three degrees of freedom, angles of rotation relative to axes 1-3, are controlled. Orthogonal and nonintersecting, angles 1 and 2 form the "hip joint" of a leg, segments 4 and 5 its "femur" and "tibia." Axis 3 is parallel to axis 2. An electromechanical servosystem produces movement through each of the controlled degrees of freedom. A three-degree Cardan foot suspension fitted with a surface-contact sensor is mounted on the tibia.

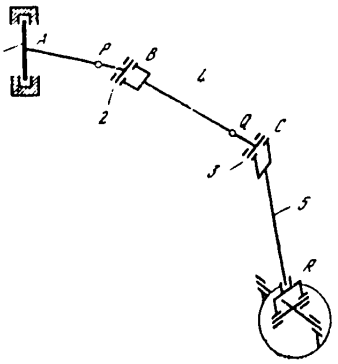

Figure 1.

The motion-control system generates control signals producing the machine's movement with automatic adaptation to small surface irregularities upon command from the operator (or a higher level of the control system) determining the motion of the body of the machine and the basic characteristics of its locomotion. Figure 2 is a functional block diagram of the control system.

It consists of the following major components:
- the set of controlled stepping-cycle generators (GS) comprises six identical generators forming closed space-time curves of the stepping cycle (i.e., the trajectory traced by the end of the leg) of each leg in the plane of the several auxiliary Cartesian coordinates. The generators are interconnected such that the desired relationships are maintained between the phases of the stepping cycles, which insures the required form of movement. Signals from the foot surface-contact sensors constitute the inputs into this component. Component parameters are assigned by the operator (or a higher level of the control system); component outputs are fed to the input of the linear converter;

- the linear coordinate converter (LC) converts the output from the generator unit for geometrical coordination of the stepping cycles with the body and extremities of the machine as well as their scaling. Converter parameters are assigned by the operator (or a higher level of the control system); component outputs are fed to the input of the maneuvering unit;

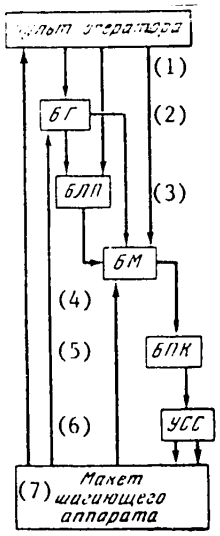

Figure 2: 1 - - operator panel; 2 - GS; 3 - LC; 4 - MU; 5 - CCC; 6 - SSA; 7 - model of walking machine.

- in accordance with commands from the operator (or a higher level of the control system), the maneuvering unit (MU) modifies the stepping cycles of the legs so as to produce the required spatial position and motion of the body of the machine. Outputs from the linear coordinate converter and the sensor signals constitute the inputs into this unit. Its outputs are fed to the input of a component set of converters of Cartesian into angular coordinates;

- the component converting the Cartesian coordinates (CCC) of the ends of the legs into the angular coordinates of the segments of the legs consists of six identical three-dimensional nonlinear servosystems which convert the outputs of the maneuvering and signal-generation unit into inputs into the servosystem amplifier unit (SSA) and take into account the limits of the working ranges of the legs.

In this article the authors study five-legged modes of machine locomotion and the possibility of designing a control system realizing these modes.

2. *The problem formulated.* We will be looking at the machine in only uniform rectilinear forward motion such that throughout the period of movement $AC \parallel O_1O_2$ and $BD \parallel O_3O_6$ (Figure 3). We will assume that the rectangular body of the machine *ABNDCM* (Figure 4) lies in a plane parallel to horizontal plane $O_1O_2O_3O_4$ and at a distance S from it. The six legs of the machine are attached according to the numeration in Figure 3 at points $A_1B_1M_1N_1C_1P$. As the machine moves, the projections of the ends of the legs fall along parallel curves O_1O_2 and O_3O_4, relative to the body the ends of the legs in the support phase moving along support segments b_1a_1, b_2a_2, ..., b_6a_6. The support segments are symmetrical with respect to the footholds.

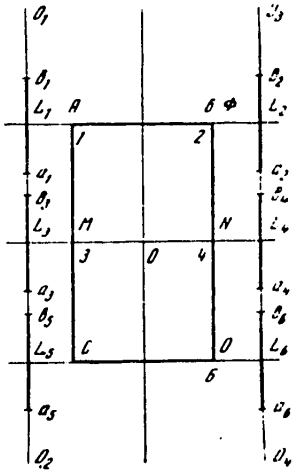

Figure 3.

The machine is 0.705 m long (AC = 0.705 m), 0.21 m wide *ср* and weighs 18 kg. The mass of a single leg is 1.9 kg. This mass is distributed as follows: concentrated at point Q is a mass of 0.75 kg and at points P and R 1 kg and 0.15 kg respectively (AP = 0.047 m, BQ = 0.08 m, CR = 0.175 m (see Figure 1); mass values are measured with an accuracy to within 10 per cent).

The projections of the ends of the legs in the support phase onto horizontal plane $O_1O_2O_3O_4$ form a polygon, which we will refer to as the support polygon.

The state of the machine will be referred to as stable if a projection of its center of gravity onto horizontal plane $O_1O_2O_3O_4$ lies within the support polygon. By z let us designate the minimum distance the projection of the center of gravity can be from boundary of the support polygon, that is, the margin of stability.

The term "hexapod gait" will be understood to refer to the process by which the machine moves in a uniform and stable rectilinear manner, in the course of which its legs execute movements which are identical and periodic but perhaps different in phase. The interval of time during which all legs of the machine are in the support phase is constant.

Let us now introduce the following parameters:

T_0 - time during which a leg is in the support phase;

T_n - time during which a leg is in the transfer phase;

H - step length;

V_0 - machine velocity, equal to the velocity of the end of a leg relative to the body in the support phase;

$H/T_n=V_n$ - velocity of the end of a leg in the transfer phase relative to the body of the machine;

T_6 - time during which all legs are in the support phase; in the case of a hexapod, T_6 is the time for which six legs are in the support phase and, accordingly, for a five-legged machine five legs. We will take the moment at which the first leg moves into the transfer phase as zero. The time elapsing from this moment until the moment at which the i-th leg passes into the transfer phase we will designate as T_i = = $(T_1 = 0)$.

Let k represent the number of different T_i; in the case of the "treshka" [literally "three-ruble note"] gait, for example, $k = 2$; $L_6 = V_0T_6$ is the distance the machine travels over time T_6.

Let us now demonstrate that, given these assumptions, the relationship

$$T_0 = kT_6 + (k-1)T_n. \tag{1}$$

is satisfied for any gait. Formula (1) is easily checked for $k = 2$ (Figure 4). In

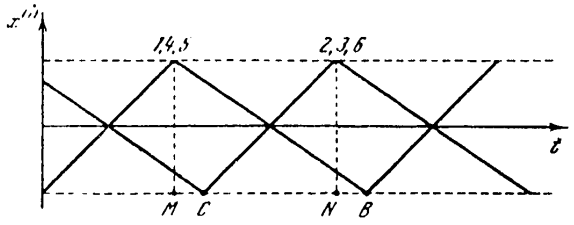

Figure 4

Figure 4, time is plotted along the horizontal axis; along the vertical axis, the relative horizontal coordinates of the ends of the legs; $MC = T_6$; $NB = T_6$; $CN = T$, but $T_0 = MB = CB+MC$; hence $T_0 = 2T_6+T_n$. The proof is analogous for $k = 3$, 4, 5 and 6.

The gait of a hexapod is determined by the set of numbers T_i, T_0, T_n and H. Let us stipulate that the "type" of gait is governed by the sequence in which legs go into the transfer phase. We will designate the gaits of a particular type with a series containing the numbers of the legs of the machine (beginning with any leg) in the order in which they enter the transfer phase. Thus 1,4,5—2,3,6 (following the commas are the numbers of the legs simultaneously entering the transfer phase) is the notation for the "treshka" gaits (the notation 2,3,6—1,4,5 would be its equivalent).

Let us now formulate our basic problems.

1. Organization of five-legged locomotion. Finding different types of five-legged locomotion.

2. Study of various transitions from one gait to another.

3. Theoretical development of a control-system unit making it possible to maintain the desired type of gait and then reconstruct it.

3. *Organization of five-legged locomotion. Construction of various types of five-legged walking-machine gaits.* Let us search for these five-legged gaits assuming that the legs are weightless and let T_6 be zero for all types of five-legged gaits.

A. Let leg 1 not participate in the locomotion. Let us now look at gaits involving the remaining five legs.

1. Let us note that to insure that the desired five-legged gait is stable, the transfer phase of leg 2 may occur only when legs 3 and 4 are in the support phase; the ends of legs 3 and 4 must then in this instance be on segments b_3L_3 and b_4L_4 respectively (see Figure 4). This observation substantially limits the number of stable types of the desired gaits. The combination ..., 3, 4—2, ... will appear in the notation for each of them.

2. If $T_3-T_4\neq 0$, then $|T_3-T_4|=\Delta\neq 0$ and the ends of legs 3 and 4 are simultaneously on segments b_3L_3 and b_4L_4 respectively for time $T = 0.5T_0-\Delta T$. If leg 2 is in the transfer phase for time T, then $V_n = H/(0.5T_0-\Delta T)$; $T_n \leqq T$ to insure stability. Let us note that the design of the machine imposes substantial limitations upon parameter V_n since the maximum speed of the joint actuators is limited. So in constructing our five-legged gaits we will be trying to decrease V_n. V_n will have its lowest value when $\Delta T=0$; $T_n = 0.5T_0$, that is, $T_3 = T_4$; $k = 3$ (from formula (1)).

3. Taking into account 1 and 2, let us now write the types of gaits possible using legs 2—6.

1) 3,4—2,6—5; 2) 3,4—2,5—6 and 3) 3,4—2—5,6.

Let us look at the first type. During the interval of time in which legs 2 and 6 are in the transfer phase, legs 3, 4 and 5 are in the support phase with the ends of legs 3 and 4 on segments b_3L_3 and b_4L_4 (see Figure 4). A projection of point 0 is thus to be found within a triangle formed by projections of the ends of legs 3,4 and 5, that is, the machine is stable. Supporting legs 2, 3 and 6 provide stability for the period of time during which leg 5 is in the transfer phase. When legs 3 and 4 are in the transfer phase, the machine loses its stability, since a projection of the end of leg 2

falls on segment L_2a_2 (see Figure 4), a projection of the end of leg 5 falling accordingly on segment L_5a_5; the stability of gait types 2 and 3 is checked in similar fashion, in the case of both types the machine becoming unstable only when legs 3 and 4 are in the transfer phase. To insure the stability of these types of gait it is sufficient to shift the track of leg 2 to the left $L_2\Phi$=0.15 m (see Figure 4). Let us note that within the limits of our accepted definition, it will be impossible to construct a stable gait using legs 2-6 without altering the track of some leg.

Let us observe that we have not been looking for gait types in which k = 4, because in the case of these types of gait V_n is 1.5 times greater than with types where k = 3.

B. Let us now look at gaits employing legs 1, 2, 4, 5 and 6. We will construct these types of gait on the basis of analogous considerations.

1. Let us note that for the interval of time during which leg 1 is in the transfer phase, the end of leg 5 must necessarily be on segment b_5L_5, and (analogously) when leg 5 is in the transfer phase the end of leg 1 must be on segment L_1a_1. As in the previous case, decreasing V_n requires that k = 3. The ends of legs 4, 5 and 6 or 1, 2 and 4 (see Figure 4), moreover, cannot form a stable support polygon; thus, $T_1 \neq T_2$ and $T_5 \neq T_6$. It is easily shown that if $T_1 = T_4$ or $T_5 = T_4$, the gait types thus obtained are all the more certainly unstable, that is, there remains one possible type of gait:

2,5—1,6—4.

2. The stability of this type of gait is tested as was done in *A*3. For the interval of time in which legs 2 and 5 are in the transfer phase, legs 1, 4 and 6 are in the support phase; the ends of legs 1 and 6 are in this instance on segments L_1a_1 and L_6a_6 and provide stability in a manner analogous to that during the period in which legs 1 and 6 are in the transfer phase. When leg 4 is in the transfer phase, the support polygon formed by projections of the ends of legs 1, 2, 5 and 6 provides stability, that is, this type of gait is stable.

B. The types of gait obtained thus far are stable assuming that the legs are weightless for any T_0 and T_n associated with relationship (1) when k = 3 and T_6 = 0. Now let us assume that the legs have weight. To insure that throughout the time of motion we satisfy the relationship

$$z > z_{min}, \qquad (2)$$

we introduce a time interval during which all legs are in support. The specific values of T_6 and L_6 required to satisfy relationship (2) are functions of the dimensions of the machine, the dimensions of its track, its step, the mass of the machine and its distribution among the segments of its legs and its required minimum margin of stability. With a track of the order of 0.2 m, L_6 = 0.05 m when z_{min} = 0.02 m is sufficient to satisfy relationship (2) for all previously mentioned five-legged gaits. Diagrams of all these gaits are presented in Figure 5; time is plotted along the horizontal axis, the coordinates of the ends of the legs relative to the body of the machine along the vertical.

4. *Restructuring the gait.* Let us now look at transitions from five-legged gaits to the "treshki" gait and from the "treshki" gait to five-legged gaits.

Gaits should be restructured as quickly as possible; relationship (2) must be satisfied in the course of the restructuring process; and the control algorithm should be simple.

Realization of transitions from one gait to another in the least time possible requires control of the speed of the end of a leg in the transfer phase V_n and transition to the transfer phase from any point of the support phase. To simplify the algorithm controlling the restructuring process we will assume that parameters V_0 and L_6 remain unchanged in the new gait and that the transition of the extremities into the transfer phase can occur only at moments 0, T_n+T_6, $2(T_n+T_6)$, $3(T_n+T_6)$, ..., (time is counted from the beginning of the restructuring process.)

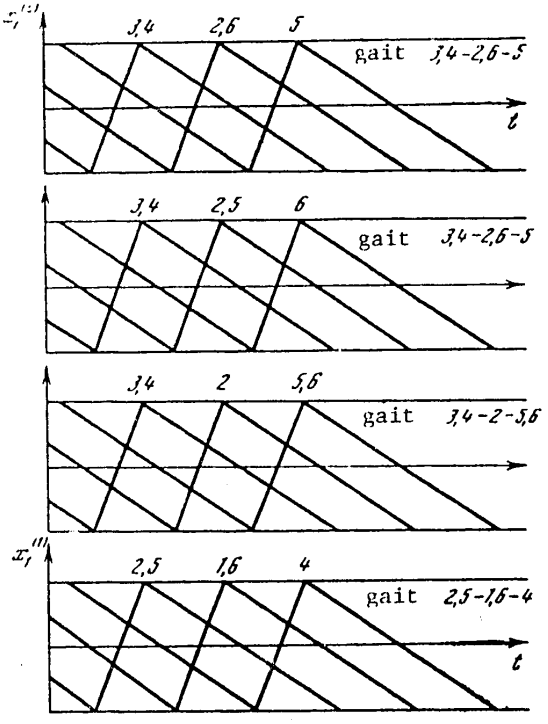

Figure 5

Let us note that, generally speaking, there are many methods of making the transition from one gait to another. The limitations imposed in this section reduce their number substantially, although, as before, the problem has more than one solution.

5. *Realization of proposed gaits and transitions.* Let us note at the outset that we can realize only those gaits, and the transitions of one of these gaits to another, which we already know to be stable.

Let us now examine in greater detail the operation of the step-cycle generators. As has already been said, the step-cycle generators form the trajectory of the motion of the ends of the legs of the machine in the plane of auxiliary coordinates $\sigma_1^{(i)}$ and $\sigma_2^{(i)}$, where i is the number of the generator corresponding to the number of the leg (see Figure 4). A specific type of step-cycle trajectory is not essential to the realization of a given gait or of the transition from one particular gait to another. What is important is that the movement of the end of a leg with respect to σ1 determined by the step-cycle generator is governed by the values of parameters T_0, T_n, V_0, V_n, T_6, a and b; the importance of parameters a and b will become clear below. The step-cycle generator is designed such that movement along axis $b_1^{(i)}$ is governed by the solution of the differential equation

$$\frac{d\sigma_1^{(i)}}{dt} = V_n^{(i)}\left[\frac{1+\operatorname{sgn} u^{(i)}}{2}\right] - V_0\left[\frac{1-\operatorname{sgn} u^{(i)}}{2}\right], \qquad (3)$$

where $u^{(i)}$ - control; in the transfer phase $u^{(i)} > 0$, in the support phase $u^{(i)} < 0$; V_0 - component of the velocity of the end of a leg in the support phase along axis σ_1; $V_n^{(i)}$ - component of the velocity of the e of a leg in the transfer phase along axis σ1 (these may be different for different legs of the machine). Let us now show that

with our selection of the function $u^{(i)}$ and of $V_n^{(i)}$ in (3) we can reduce the problem of maintaining a particular type of gait and of realizing the transition of one type of gait to another to the problem of formulating a timetable for the transitions of the extremeties of the machine to the transfer phase. Let us assume that

$$u^{(i)} = [a - \sigma_1^{(i)}(t)]\left[\frac{1+\operatorname{sgn} u^{(i)}}{2}\right] - [b + \psi^{(i)}(t)]\left[\frac{1-\operatorname{sgn} u^{(i)}}{2}\right],$$
$$\psi^{(i)} = \begin{cases} 0, & \text{if } t \neq t_p^{(i)}, \\ -(a+b), & \text{if } t = t_p^{(i)}, \end{cases} \tag{4}$$

where a is the programmed value of the maximum extension of the end of a leg of the machine in the direction of its movement along axis σ_1 ($a>0$); b - programmed value of the extension of the end of a leg of the machine in the direction counter to its movement along axis σ_1 ($b>0$); $t_p^{(i)}$ - previously assigned moments of transition of the extremities from the support phase to the transfer phase, i being the number of the leg, p the number of the step. As can easily be seen, the sign of $u^{(i)}$ will then change from "-" to "+" at the previously determined moments $t_p^{(i)}$, while the sign of $u_p^{(i)}$ will change from "+" to "-" when $\sigma_1^{(i)}$ reaches the desired value (a). To insure that the sign of $u^{(i)}$ changes from "+" to "-" at the desired moments $[t_p^{(i)} + T_n]$ requires that in time segment $[t_p^{(i)}, t_p^{(i)}, + T_n]$ the value of $V_n^{(i)}$ = const in equation (3) be assigned such that $\sigma_1^{(i)}(t_p^{(i)} + T_n) = a$. We can show that the required value for $V_n^{(i)}$ may be found from the relationship

$$V_p^{(i)}(p) = V_n\left[1 - \frac{\Delta\sigma_1^{(i)}(p)}{a+b}\right],$$
$$\text{where } V_n = \frac{a+b}{T_n}; \quad \Delta\sigma_1^{(i)}(p) = b + \sigma_1^{(i)}(t_p^{(i)}). \tag{5}$$

The equation describing the operation of the step-cycle generator along axis σ_1 may thus be written in the form

$$\frac{d\sigma_1^{(i)}}{dt} = V_n\left[1 - \frac{\Delta\sigma_1^{(i)}(p)}{a+b}\right]\left[\frac{1+\operatorname{sgn} u^{(i)}}{2}\right] - V_0\left[\frac{1-\operatorname{sgn} u^{(i)}}{2}\right];$$
$$u^{(i)} = [a - \sigma_1^{(i)}]\left[\frac{1+\operatorname{sgn} u^{(i)}}{2}\right] - [b + \psi^{(i)}(t)]\left[\frac{1-\operatorname{sgn} u^{(i)}}{2}\right], \tag{6}$$
$$\text{where } \psi^{(i)}(t) = \begin{cases} 0, & \text{if } t \neq t_p^{(i)}, \\ -(a+b), & \text{if } t = t_p^{(i)}, \end{cases}$$
$$\Delta\sigma_1^{(i)}(p) = b + \sigma_1^{(i)}(t_p^{(i)}).$$

The problems of maintaining the desired type of gait and of realizing a transition from one type of gait to another have accordingly been reduced to the problem of formulating a timetable for transitions of the extremeties to the transfer phase ($t_p^{(i)}$). If for $t_p^{(i)}$ we assign a certain sequence, $\sigma_1^{(i)}(t)$ will have the form shown in Figure 6.

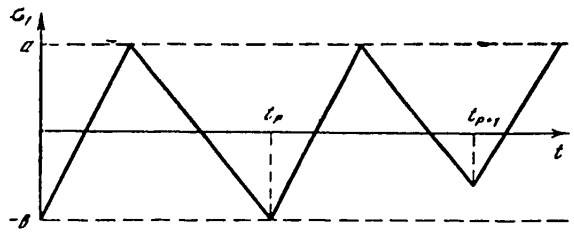

Figure 6

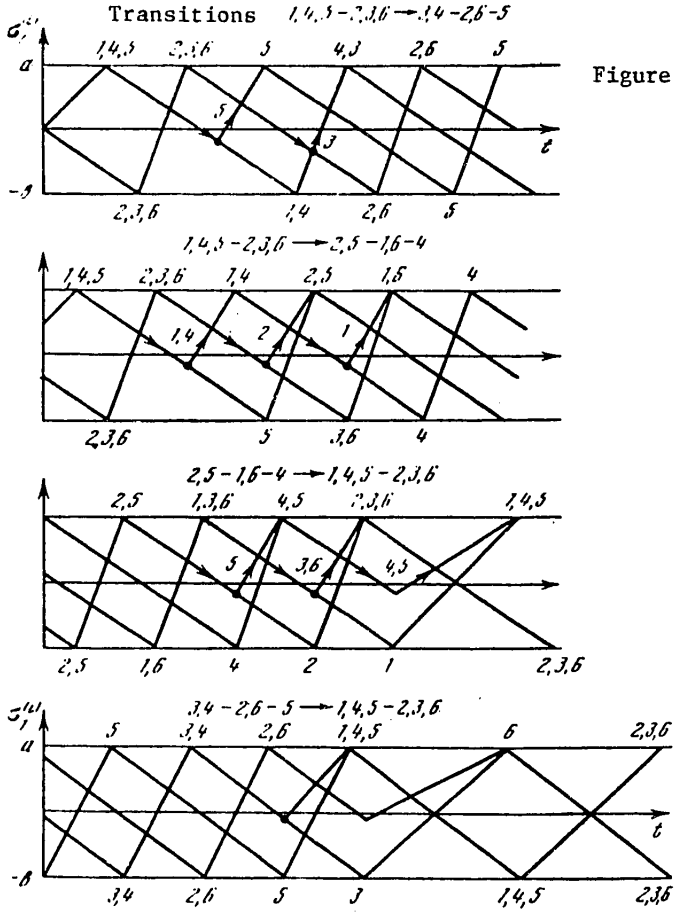

Figure 7

One of the components of this apparatus is the "rhythm" generator, which generates a periodic signal with a period of $T_T = T_n + T_6$. Let us note that from Section 4 it follows that $T_i = n_i (T_n + T_6) = n_i T_1$, where $n_i = 0,\ldots, k\text{-}1$ for all previously described gaits. This allows us to assign a sequence of moments $t_p^{(i)}$ by means of the "rhythm" generator, since the movement of each of the machine's extremities is regular with a period of $T_y = kT_T$ (k - gait parameter), while, as pointed out above, the movements of the different extremities vary in relation to one another by values T_i, which are multiples of T_T. A pulse distributer is used to assign sequence $t_p^{(i)}$ in the walking machine's motion control system. It operates as follows: pulses from the "rhythm" generator (T_T) are fed to one of its inputs, pulses with a period of T_y to the other. From each of its six outputs come signals with period T_y, T_T the time elapsing between the moments of the occurrence of pulses at its j-th and $(j+1)$-th outputs. The six outputs correspond to a maximum value of $k = 6$.

If the type of gait has been determined, it is sufficient to realize it to connect the step-cycle generators to the appropriate pulse-distributer outputs. The output signals will then regulate the moments at which the sign of $u^{(i)}$ of the corresponding step-cycle generators changes from "+" to "-" (4); the transition of the extremities from the support phase to the transfer phase will thus occur in accordance with the timetable corresponding to the desired type of gait.

Values of the parameters n_i are employed to determine the step-cycle generators corresponding to the various pulse-distributer outputs. Thus $N_i = n_i + 1$ represents the number of the pulse-distributer output, i the number of the step-cycle generator. Realization of the desired algorithms for transition from one gait to another thus requires: 1) formulation of the values of parameters T_T, T_y and V_n corresponding to the new gait; 2) changing the order in which the inputs of the step-cycle generators are connected to the pulse-distributer outputs.

6. Description of the step-cycle generator control unit. Figure 8 is a block diagram of the system permitting realization of desired gaits and transitions from one gait to another.

In developing this block diagram it was proposed that each gait the machine is to execute and transition from one gait to another be assigned an appropriate value of parameter P, a gait and transition identifier. The block diagram contains as component 1 an operator control panel or an interface with a higher level of the machine's control system. Parameters V_0, a, b, H, L_6 and values of gait and transition identifier p are the outputs of this unit;

- unit 2 conforms the set of values of parameters $A1$, $A2$, $A3$, $A4$, $A5$, $A6$ and k to the value of the gait and transition identifier supplied to its input. The values of these parameters are the signals controlling the switches (components 9-14); k is the gait parameter;

- unit 3, to the inputs of which are supplied the values of parameters V_0, H and L_6 from the output of unit 1 and of k from the output of unit 2, generates the values of V_n in accordance with the formula

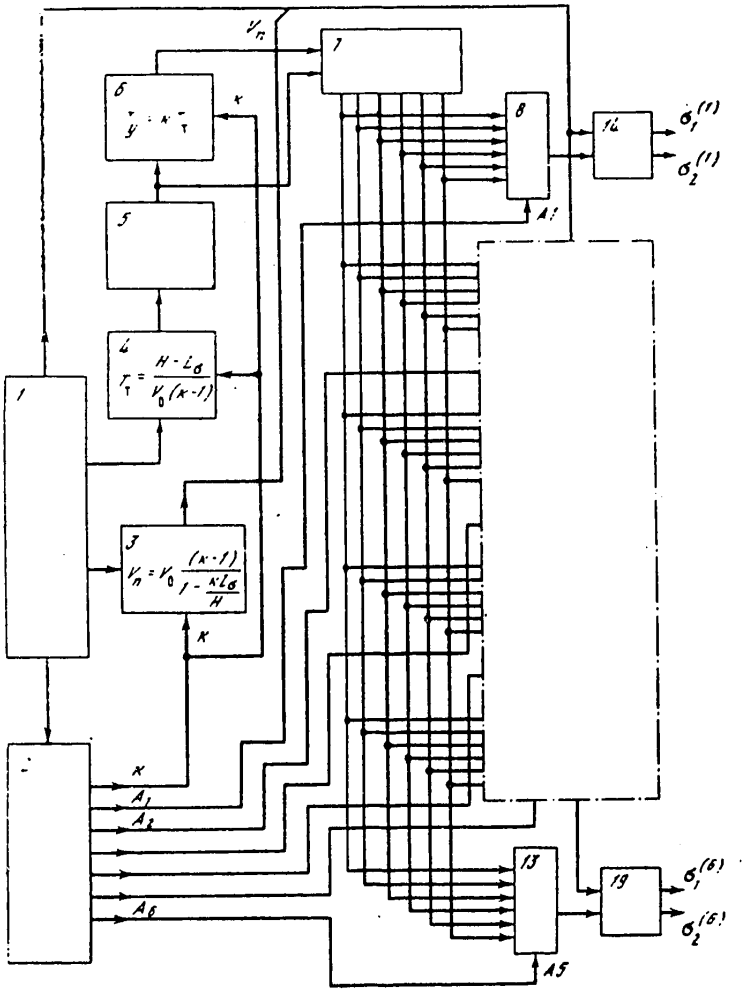

Figure 8

$$V_n = V_0 \frac{(k-1)}{1 - \frac{kL_6}{H}};$$

- unit 4, to the inputs of which are supplied the values V_0, H and L_6 from the output of unit 1 and k from the output of unit 2, generates the value of parameter T_n in accordance with the formula

$$T_n = \frac{H - L_6}{V_0(k-1)};$$

- unit 5 is the rhythm generator. It converts the value of parameter T_T into a sequence of pulses with period T_T;

- unit 6 converts the signal supplied from the output of the rhythm generator into a pulse sequence of period $T_y = kT_T$. The value k is supplied from the output of unit 2;

- unit 7 is the pulse distributer. Its functioning has been described in Section 5;

- units 8-13 are the switches *6* in *1* controlled by signals from the outputs of unit 2;

- units 14-19 are the step-cycle generators.

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PUBLICATIONS

MODELING AND OPTIMIZING COMPLEX CONTROL SYSTEMS

Moscow MODELIROVANIYE I OPTIMIZATSIYA SLOZHNYKH SISTEM UPRAVLENIYA in Russian 1981 (signed to press 8 Jun 81) pp 2-3, 263-265

[Annotation, foreword and table of contents from book "Modeling and Optimizing Complex Control Systems", edited by Ya. Z. Tsypkin, USSR Academy of Sciences, Izdatel'stvo "Nauka", 2350 copies, 265 pages]

[Text] This collection treats the subjects of identification and optimum control, computer and large industrial robot systems and medical, biological and technical problems in control.

The book is intended for scientific, technical and engineering personnel.

Foreword

The concepts of automatic control and systems theory have now gained extensive currency in biology, medicine, economics, sociology etc. New problems generate new theoretical ideas, which not infrequently lead to advances in control theory. Of interest in this connection are publications dealing with application of the methods of control theory to a variety of problems. The present collection is precisely this kind of publication.

The first part of the collection deals with general theoretical problems concerning the modeling and optimization of systems controlling complex objects. Attention here is devoted primarily to problems arising in connection with the study of specific nonstandard tasks. A feature characterizing most of the methods of analysis and synthesis discussed consists in their orientation toward the employment of computers.

A great deal of attention is given to consideration of such factors as incompleteness of information and random perturbations of parameters and signals. The modern mathematical apparatus of random-process theory is employed to develop adaptive algorithms and (optimum or almost optimum) filtering procedures.

The second part of the collection is devoted to analysis of specific problems. An algorithm for precise or an approximate solution of a problem is in many instances the result. The problems studied are among the category of new problems associated with the planning and design of automatic and man-machine control systems, enhancing control system reliability, economic and production planning and the development of new control technologies.

Taken as a whole, the material contained in the collection provides a fairly complete picture of the present status of a number of central problems as well as of the promise and basic directions of scientific progress in the field of control.

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Identification and Optimum Control

Computer Systems

Large Systems

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UDC 621.3:681.3

DESIGN OF COMPUTER INPUT/OUTPUT SYSTEMS

Leningrad ORGANIZATSIYA VYCHISLITEL'NYKH STRUKTUR I PROTSESSOV: PROYEKTIROVANIYE SISTEM VVODA-VYVODA EVM in Russian No 8, 1981 (signed to press 31 Dec 80) pp 2, 173-175

[Annotation and table of contents from collection "Organizing Computer Structures and Processes: The Design of Computer Input/Output Systems", edited by Z. I. Tsar'kova, Izdatel'stvo Leningradskogo universiteta, 2449 copies, 184 pages]

[Text] This issue of the collection surveys the latest results of studies on structural development and the organization of external computer devices and channel systems, interfaces and converters. It deals with the organization of computer processes in present-day special-purpose and minicomputers. The works contained here also discuss the problems of the reliability and accuracy of these devices.

The collection is intended for specialists in systems organization and in the planning and design of computers, facilities and systems.

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HILBERT OPTICS

Moscow GIL'BERT-OPTIKA in Russian 1981 (signed to press 13 Mar 81) pp 2-6

[Annotation, table of contents and foreword from book "Hilbert Optics", by Lev Markovich Soroko, Izdatel'stvo "Nauka", 3400 copies, 160 pages]

[Text] This monograph is devoted to Hilbert optics, which constitutes an independent branch of Fourier optics. Following the mathematical introduction it sets forth the theory underlying methods of visualizing optical irregularities; it describes the operating principles and categorization of shadow-indication instruments and presents algorithms employed in computer modeling of Hilbert optical systems and in analyzing the results of measurements. The Hilbert optical instruments described in the book, part of which the author helped to develop, provide high image contrast and make maximum use of light flux; they are characterized by uniform sensitivity throughout the range of spatial frequencies; they are simple to use and and may be combined with holographic devices.

A book on Hilbert optics fills the gap in the scientific literature between books on optical theory and texts of an applied nature.

Illustrations - 80; tables - 1; bibliography - 82 titles.

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Foreword

The term "Hilbert optics" refers to a branch of optics which uses the Hilbert transform on functions of two spatial coordinates on a plane. The Hilbert transform permits the visualization of optical irregularities with a maximum degree of contrast simultaneously for all spatial frequencies transmitted by the optical system [1]. Realization of the Hilbert transform in optics involves the use of Fourier optical devices, as well as devices unique to Hilbert optics: optical plates with a step whose height corresponds to a phase jump of 180° for a certain light wavelength, diffraction gratings with irregularity and composite double-refracting plates. Like Fourier optics [2], the field of Hilbert optics is still quite new. Neither Fourier nor Hilbert were opticists and made no direct contribution to optics. The universality of the Fourier and Hilbert integral transforms nevertheless proved higher than the barrier separating different branches of science; these transforms thus found their way into the field of optics, where they are used, among other things, to describe mathematically the processes occurring in different systems of Hilbert optics.

David Hilbert (1862-1943) was the leading mathematician of his day. His name has been given to many discoveries made in mathematics: the Hilbert space, the Hilbert transform, the Hilbert subgroup and others [3]. His work exercised an influence on many branches of science allied with mathematics: on the spectral theory of signals [4], statistical radio engineering and in physics. In the field of integral equations he generalized the theory of spectral decomposition. The Hilbert transform, which constitutes only a small Hilbert's mathematical legacy, is widely employed in signals theory, linear circuit theory as well as in optics and physics.

The Hilbert transform in optics was first realized in its pure form in 1967 by Lowenthal and Belvaux [5], who used for this purpose a spatial-frequency filter in the form of an optical plate with a step creating a phase shift of 180°. It was demonstrated experimentally that use of the Hilbert transform made it possible to detect abberations of a higher order than permitted by the shadow-indication device with the Foucault knife. In 1971 Belvaux and Lowenthal realized the Hilbert transform in white light using two composite double-refracting plates, which were positioned in the plane of the spatial frequencies of an achromatic Fourier-optical system. In 1971 L. M. Soroko and V. A.

Suyetin [7] fabricated and studied a new optical device for work in Hilbert optics: a diffraction grating with an irregularity, or phase jump. A diffraction grating of this construction is a universal half-wave phase filter of Hilbert-optical spatial frequencies and permits realization of the Hilbert transform for any wavelength of light from a monochromatic source without any further adjustment. This is what distinguishes it from the conventional half-wave phase optical filter, the step in which corresponds to a phase shift of 180° for only a specific light wavelength. In 1973 Eu and Lohmann [8] realized an isotropic Hilbert transform using a ring light source by averaging the unidimensional Hilbert transforms with respect to an angle in coherent and noncoherent light. In 1974 L. M. Soroko and V. A. Suyetin [9] showed that a diffraction grating with a number of phase discontinuities distributed across the visual field of a shadow-indicating device with a defocussed diaphragm gives a contrasting a easily interpreted picture simultaneous visualization of optical irregularities for a number of narrow spectral lines fairly widely distributed throughout the spectrum. In 1975 V. A. Arbuzov and V. A. Fedorov [10] realized an isotropic Hilbert transform using point and cruciform light sources. This work concluded the first phase in the development of Hilbert optics.

The possibilities offered by Hilbert optics have yet to be adequately understood, and the sphere of application of Hilbert optics is not limited only to systems for visualizing optical irregularities. The present book illustrates the application of Hilbert optics in image-recognition systems and in the solution of other problems in information theory using the example of an optical system for recognizing characters in standard type, the number of whose optical channels has been increased from one to eight. Together with the Fourier transform, several types of Hilbert transforms [11] and combined Hilbert-Fourier transforms are employed for this purpose.

Hilbert-optical devices are simple in construction; they offer high levels of immunity to interference with indifferent use, while the pictures of the visualization of optical irregularities can be easily interpreted by an operator having no special training. Systems controlling optical-component quality which incorporate Hilbert-optical devices should see extensive utilization in research institutes as well as in plant laboratories and shops.

In conclusion the author expresses his deep appreciation to V. A. Suyetin, together with whom he conducted his studies in Hilbert optics, to T. A. Strizh for computer calculations, to Yu. V. Chuguy for creative collaboration and to V. A. Fedorov for discussing achromatic Hilbert optical systems.

The author is also grateful to V. A. Zverev, corresponding member of the USSR Academy of Sciences, for his valuable comments in reviewing the manuscript.

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ABSTRACTS OF ARTICLES IN JOURNAL 'AUTOMATIC EQUIPMENT AND COMPUTERS', SEPTEMBER-OCTOBER 1981

Riga AVTOMATIKA I VYCHISLITEL'NAYA TEKHNIKA in Russian No 5, Sep-Oct 81 pp 95, 97, 99

UDC 681.324

INTEGRATED OPTIMIZATION OF THE LOCATION OF COMPUTER CENTERS AND INTERCENTER DATA-TRANSMISSION NETWORKS

[Abstract of article by Bober, V. I. and Yanbykh, G. F.]

[Text] This article defines the problem and proposes an algorithm employing the "branch and bound" technique for optimizing the location of interlinked computer centers (CC) and an intercenter data-transmision network (IDTN). Subscribers are linked to a CC via radial data-transmission networks. Minimum expenditures for setting up and operating the network constitutes the criterion of optimization. The work proposes a three-level system of strategies to be employed in the branching process. Strategy S1 would be employed to select the location of the CC, S2 the configuration of the IDTN and S3 the number of communication channels on each branch of the IDTN. The results of a computerized machine experiment are also presented. Illustrations - 1; bibliography - - 5 titles.

UDC 681.325.5

ANALYSIS OF THE EFFECT OF COMBINING PROCESSOR AND MEMORY FUNCTIONS IN MULTIPROCESSOR SYSTEMS

[Abstract of article by Sokol, Yu. M.]

[Text] A multiprocessor system with a common memory module in which processor operation is partially combined with that of the memory module is discussed. Determinate and stochastic mathematical models, for which are obtained expressions making it possible to calculate the efficiency of a multiprocessor system, are used to study the efficiency of this system. On the basis of the relationships established, comparative analysis is undertaken of the operational efficiency of a system with combined processor and memory functions and of a system without this combination. The work studies the effect obtained with combination as a function of the number of processors in the system, the degree of the combination and of memory loading by a single processor. Parameter relationships are obtained which yield the maximum effect. It is shown that the maximum effect is achieved with the determinate model and equals 100 per cent, while in the stochastic model the effect does not exceed 33 per cent. Illustrations - - 6; bibliography - 4 titles.

UDC 517.9

ADAPTIVE ALGORITHM FOR SYNTHESIZING LINEAR-THRESHOLD NETWORKS

[Abstract of article by Sychev, A. N.]

[Text] An algorithm for synthesizing linear-threshold networks is proposed which permits realization of an arbitrary Boolean function on a single threshold element with the addition of a simple linear unit comprising the aggregate of module-2 adders. The algorithm permits the use for synthesis of threshold elements realizing strictly threshold functions. It employs only arithmetical operations on coefficients of the spectra of the given functions and matrix operations. The article describes a method of factoring a matrix constituting an orthonormal basis for Walsh functions ordered in a Carnot basis. The proposed algorithm therefore requires only minimal computer resources and may have good machine interpretation. Illustrations - 5; bibliography - 5 titles.

UDC 681.324

STUDY OF THE EFFICIENCY OF MULTIPROCESSOR SYSTEMS WITH INTERNAL MEMORY UNITS

[Abstract of article by Kornev, M. D., Kreynin, A. Ya., Sokol, Yu. M. and Kazantsev, P. N.]

[Text] A multiprocessor system including common memory modules and homogeneous-processor modules is examined. The modules are linked together via a common bus. Each processor has an internal memory unit accessible via the common bus to any system processor and, via another output, to its own processor. The system's entire memory constitutes a single address space. On the basis of analytical calculations and the results of statistical modeling, the work establishes the operational efficiency of the system as a function of the number of processors in the system, the probability of reference to an individual internal memory and the probability of reference to common memory modules as well as of the relationship between servicing times in an individual internal memory unit and in the common bus. It is shown that an important gain in efficiency is achieved by an increase in the frequency with which individual memory units are queried and a decrease in the time required to service these queries. Combination of processor and memory functions also yields a substantial advantage. Tables - 1; illustrations - 5; bibliography - 7 titles.

UDC 681.324

USE OF NUMERICAL PROGRAMMED CONTROL DEVICES IN MULTIMICROPROCESSOR SYSTEMS

[Abstract of article by Mazilkin, I. G., Petrov, G. A. and Pulkis, G. O.]

[Text] This work examines the possibility of employing numerical programmed control systems (NPC) with multimicroprocessor systems (MMPS). It proposes parallel NPC algorithms and evaluates their productivity. It discusses the design of one version of an MMPS along with algorithms controlling the realization of subtasks and selecting the data required for their execution. Illustrations - 6; bibliography - 6 titles.

UDC 519.7

EQUIVALENT CONVERSIONS FOR A SYSTEM OF DIRECT-COUPLING EQUATIONS

[Abstract of article by Matrosova, A. Yu.]

[Text] A special category of systems of direct-coupling equations is examined. The concept of the equivalence of these systems is introduced. The complexity of a system is determined and an algorithm proposed for changing from a given system to an equivalent system of lesser complexity. This task may find application in modeling asynchronous series-connected devices. Bibliography - 2 titles.

UDC 519.718

AN ESSENTIAL CRITERION FOR A TEST SEQUENCE

[Abstract of article by Sklyarevich, A. N.]

[Text] It is shown that a given sequence of input sets of combination automatic equipment is a test of the check of its operating efficiency in the case of a given category of malfunctions if because of malfunctions of this type the automatic equipment cannot realize a single one of the functions, the values of which differ from corresponding values of the output function of a properly operating machine only on part or all input sets in the given sequence. The work presents examples of the use of the criterion for direct determination of a test or to establish the possibility of using the test found for a broader category of malfunctions. Bibliography - 1 title.

UDC 681.322:519.854

A METHOD OF FORMING PSEUDORANDOM BINOMIAL SEQUENCES

[Abstract of article by Litikov, I. P.]

[Text] Digital frequency computers belonging to a category of digital analogs find application in control of stepwise motion along continuous trajectories: in controlling metal-cutting machines, robots, graph plotters and gas cutting machines. Development of an effective system of test diagnostics, which must include a pseudorandom binomial sequence generator, plays an important role in insuring the operational effectiveness of these devices. The task of synthesizing such a generator as a basis for digital-frequency decision elements is complicated by the fact that they have no shift register. This work proposes a method of forming pseudorandom binomial sequences by a generator, the basis for whose design is the basic component of digital-frequency equipment--the binary demodulator. Elements of probability theory, Galois fields and finite automatons are employed to prove the analogy of the analyzed with random sequences. The following conclusions are accordingly drawn. Realization of the generator design does not require the incorporation of shift registers, which substantially preserves the uniformity of design of digital frequency structures, while, in contrast to the M-sequences in the period $2^{2n}(1-2^{-n})$, the sequences formed by this generator have an equal number of zeros and ones. The generation and then "jumbling" of n independent M-sequences makes it possible, with the use of additional equipment, to obtain analogs of known schemes on shift registers. Illustrations - 2; bibliography - 2 titles.

UDC 519.713

SYNTHESIS OF GENERAL-PURPOSE SYMMETRICAL SYSTEMS

[Abstract of article by Dulepov, Ye. G.]

[Text] A method of synthesizing general-purpose symmetrical systems with parallel adjustment--a triad method--is set forth. This method consists essentially in the use as elements of the function-adjustment code in the multinumber single-digit adder system. The aggregate of the sets of adder function values is broken down into triads; each triad has three sets; the code distance between any of the sets of a triad is 2. The Gray code is employed to break the sets down into triads. It is shown that the use of this method simplifies the system and reduces the number of external poles in it. Tables - 2; illustrations - 1; bibliography - 5 titles.

UDC 519.832

SYMMETRICAL-LEXICOGRAPHICAL OPTIMIZATION PROBLEMS AND ANTAGONISTIC GAMES

[Abstract of article by Podinovskiy, V. V.]

[Text] This work is a study of decision-making problems involving a number of criteria $K_1,\ldots,K_m$, when for comparison of preferability strategies initially are compared the $\pi 1$ of the corresponding criteria values, the best strategy being considered the one for which this value is greater; if these values are equal, the $\pi 2$ values are compared in similar fashion etc. where $\pi = (\pi 1, \pi 2,\ldots, \pi m)$ is a permutation of set $\{1, 2,\ldots, m\}$. It is shown that discrete symmetrical-lexicographical optimization problems reduce to problems of maximizing a single numerical function. A number of specific characteristics and features of symmetrical-lexicographic antagonistic games are established. Among other things, it is shown that in a combined expansion of this game, the guaranteed average gain for one of the players may prove worse than the corresponding value for an initial game in pure strategies. Tables - 2; bibliography - 11 titles.

UDC 519.832

ADAPTIVE CHARACTERISTICS OF AUTOMATA WITH REGULAR TACTICS

[Abstract of article by Eydel'man, S. D. and Ezrokhi, A. I.]

[Text] The possible behavior of a broad category of stochastic multi-output automata with regular tactics in random steady-state environments is studied. It is shown that the probability characteristics of the behavior of a sequence of finite automata converge with those of the corresponding limited-infinite automaton (with a denumerable number of states). The work defines the conditions under which, regardless of their initial state, automata with a probability of 1 go into a stable optimum regime (the latter (the latter is adaptive). In conclusion the article discusses the possibility of employing this category of automata for adaptive control of computer-system servicing modes. Bibliography - 15 titles.

UDC 681.51:519.872

METHOD OF DETERMINING THE MEAN OPERATING INDICATOR OF A VARIABLE-MODE NETWORK FRAGMENT

[Abstract of article by Sklyarevich, A. N. and Sklyarevich, F. A.]

[Text] This work discusses a network fragment with two operating modes. Each mode has its own responses and its own system of first-order linear differential equations defining the laws governing the change in operating indicators. One-time mode change occurs at a constant rate. A system of first-order linear differential equations for mean efficiency indicators is found without the use of Kolmogorov-Fokker-Planck equations; the authors establish the validity of an algorithm for obtaining it directly by modifying system operating equations in each mode. The article presents an example of the application of this method involving calculation of the average throughput capacity of a variable-mode network fragment. Bibliography - 4 titles.

UDC 681.518.54

ESTABLISHING OPTIMUM DIAGNOSTIC CONTROL-SYSTEM PARAMETERS WITH DICHOTOMY

[Abstract of article by Ratushnyy, B. A.]

[Text] The problem of establishing optimum control-system parameters with differential diagnostics (dichotomy) is discussed. With normal distribution of control parameter x in regions of functioning D_1 and malfunctioning D_2 of the states of the object, with estimates of the mean value of $\tilde{m}_1$ and $\tilde{m}_2$ and of the mean quadratic deviation $\tilde{\sigma}_1$ and $\tilde{\sigma}_2$ obtained on the basis of statistical analysis of the results of measurements, and with satisfaction of the relationships $\frac{\overline{m}_1}{\tilde{\sigma}_1} \geq 3\sqrt{2}$, the author obtains a simple formula for the optimum value for parameter x $X_{opt} = \frac{m_1\sigma_2+m_2\tilde{\sigma}_1}{\tilde{\sigma}_1+\tilde{\sigma}_2}$, in the case of which the probabilities of correct diagnosis of D_1 and D_2 are equal as are, accordingly, the probabilities of errors in categorizing the states of the object. Illustrations - 1; bibliography - 3 titles.

UDC 621.317.341

USE OF DISCRETE METHODS FOR IDENTIFYING DIFFERENTIAL MODELS BY MEASURING SYSTEMS

[Abstract of article by Andriyanov, A. V. and Ponomarev, D. M.]

[Text] This work discusses a method of identifying the parameters of linear differential models of signals and systems. By breaking signals down in accordance with a system of orthogonal multiplicative base functions, the problem reduces to the identification of difference models. The authors propose an effective algorithm making it possible to determine the parameters of differential models and present the results of experimental studies on an automated pulse measuring system. Tables - 1; illustrations - 4; bibliography - 7 titles.

UDC 681.327:519.713

THE POSSIBILITY OF REALIZING AN ASYNCHRONOUS INTERFACE USING A SELF-SYNCHRONIZING CODE WITH AN IDENTIFIER

[Abstract of article by Varshavskiy, V. I., Marakhovskiy, V. B., Peschanskiy, V. A. and Rozenblyum, L. Ya.]

[Text] A method of establishing asynchronous interface not critical to the occurence of junction-bar delay distortion is demonstrated using the example of an interface for byte-by-byte data transmission. The interface is realized in a category of aperiodic systems, that is, systems whose behavior is invariant with respect to magnitudes of component delay. Tables - 1; illustrations - 1; bibliography - 4 titles.

UDC 681.324.012.001.63

STATISTICAL MODELING OF CONFLICT SITUATIONS IN MULTIPROCESSOR SYSTEMS

[Abstract of article by Koryachko, V. P. and Smolyarov, N. A.]

[Text] The authors discuss statistical modeling of conflict situations in multiprocessor systems. They propose an algorithm for modeling conflict situations and present the results of calculations for a specific example. Tables - 1; illustrations - 2; bibliography - 3 titles.

8963
CSO: 1863/35

ABSTRACTS OF ARTICLES IN 'ELECTRONIC MODELING', NOVEMBER-DECEMBER 1981

Kiev ELEKTRONNOYE MODELIROVANIYE in Russian No 6, Nov-Dec 81 pp 109-112

[Text] UDC 518:517.948

Sizikov, V. S., "Application of Similitude Principles to Simulation of Some Incorrectly Posed Problems."

New correlations are derived for the error in solving a first-order equation by Tikhonov's regularization method. Definitions of the estimate V and similar W examples (problems, equations) are introduced relative to a certain practical example (original) P. Refs: 11 titles.

UDC 681.3+519.2

Babordin, K. A., "A Method for Solving the Dirichlet Problem for a Poisson Equation by the Monte-Carlo Method Using a Hybrid Computer System."

A method is examined for organizing the calculations associated with solving a Direchlet problem for a Poisson equation using a probabilistic hybrid computer system consisting of an alphanumerical special processor and a digital computer. 10 figs. Refs: 10 titles.

UDC 681.322.06+681.3.323

Korneyev, V. V., and Monakhov, O. G., "Decentralized Task Allocation in Computer Systems With a Programmable Structure."

A method is suggested for isolating communicating subsystems intended to solve parallel problems. The method does not require complete information on the state of the computer system and of the problems introduced into the system. 5 tables. 1 fig. Refs: 9 titles.

UDC 681.325.5

Levina, A. I., "Organization of the Structure and Computation Process of a Specialized Computer for Analysis of Regular Nets by the Method of Fragmentary Simulation."

This paper examines a new approach to organizing a specialized computer intended for analysis of regular nets in fragments, based on multiple use of a reprogrammable fragment model. 5 tables. 10 figs. Refs: 4 titles.

UDC 681.306

Polyakov, A. K., and Lyashko, M. M., "Languages for Simulation of Computer System Structures."

This paper examines some specialized languages and simulation systems oriented on problems associated with analyzing the structure of computer systems and their software (with evaluating productivity, time delays, bottlenecks and queues; debugging control algorithms; analyzing interaction of program modules, etc.). 1 fig. Refs: 10 titles.

UDC 621.3.01

Demirchyan, K. S., and Butyrin, P. A., "Solution of the Problems of Parametric Synthesis by the Methods of Electric Circuit Analysis."

A relationship is established between the problems of parametric synthesis and electric circuit analysis. This relationship is used as the basis for proving a number of theorems making it possible to use, in solving problems of the first type, a more-profoundly developed and well tested apparatus for solving problems of the second type. 2 figs. Refs: 4 titles.

UDC 621.382.3

Korolev, Yu. V., and Yushchenko, I. A., "An Algebraic Method for Synthesis of Macromodels of Complex Electric Circuits."

A formalized method is presented for synthesis of macromodels of complex electronic circuits within the framwork of the algebraic systems provided by the theory of electric circuits. The process of constructing macromodels at different levels of complexity is examined with an analog-digital converter as an example. 7 figs. Refs: 4 titles.

UDC 621.39:681.3

Norenkov, I. P., and Zinov'yev, P. A., "Multilevel Optimization of Complex Technical Systems."

This paper examines the statement of problems associated with optimizing complex technical systems and the solution methods using, as the example, large integrated circuits subjected to descending design in automatic programmed design systems. The end result of optimization is the serviceability conditions for the element parameters. 4 tables. 2 figs. Refs: 5 titles.

UDC 681.5:621.372.5

Takhvanov, G. I., Belyanina, N. V., and Tupitsyn, D. D., "Structurally Compensated Smoothing Devices."

The basic premises pertaining to structurally compensated smoothing devices are established, and typical circuits are presented. It is demonstrated that the principle of structural compensation of systematic output errors extends to many other devices used to process noisy signals. 6 figs. Refs: 11 titles.

UDC 681.326.75

Khizhnyak, V. Ya., Serdyuk, G. B., and Bazutkin, V. V., "A Mathematical Model of Detection of Failures and Errors in Automatic Process Control System Transducers Using a General-Purpose Computer."

The authors propose a mathematical model intended for control, in real time, of a general-purpose computer's information channel (transducer--communication line--matching unit--communication line--unit converting transducer signals into computer code)--that is, controlling the readings of transducers at the input of the processor of the general-purpose computer. 1 fig. Refs: 11 titles.

UDC 621.316.71:621.3.013.8

Gorskiy, Yu. M., Popov, V. M., and Ushakov, V. A., "Approaches to Applying Adaptation Principles to Problems Associated With Controlling Synchronous Machine Excitations."

The principles of organizing adaptive strong-acting excitation regulators for synchronous machines are reviewed. The possibilities of building adaptive analytical and retrieval systems in excitation regulators are discussed. Examples of creating adaptive excitation regulators are presented. 6 figs. Refs: 13 titles.

UDC 621.107

Ignat'yev, M. B., and Maksimov, M. L., "Commutators in Construction of Microprogram Models."

Application of commutators to the construction of microprograms is examined in relation to program motion based on differential equations. Refs: 8 titles.

UDC 62-50

Batenko, A. P., "Use of Linear Models in Terminal Control Systems."

The law of terminal control is proposed as a means for accelerating, braking and stopping a vessel at a preset point. The control system contains an electronic model imparting the properties of a linear object to the nonlinear propulsion unit. 7 figs. Refs: 5 titles.

UDC 53.072.681.3

Teplov, N. L., Grishin, V. A., and Posokhov, V. P., "Investigation of the Interference Resistance of Binary and Multiposition Discrete Information Communication Systems by the Method of Statistical Simulation With a Digital Computer."

This paper presents the results of research conducted by the method of statistical computer simulation of the interference resistance of some suboptimal algorithms for processing complex signals on the background of nonstationary correlated noise. 2 figs. Refs: 5 titles.

UDC 51.001.57

Shevchenko, Yu. T., Korobetskiy, V. N., Yakubovich, Yu. V., Lyashchenko, V. K., and Bus'ko, Ye. S., "Some Problems in Simulating Effective Cutting of Blanks."

A procedure is suggested for planning the cutting of blanks of measured length, based on the methods of numerical solution of mathematical programming problems. A set of cutting optimization models and information on the developed software are presented. Refs: 11 titles.

UDC 681.325

Shcherbina, A. A., "Use of Redundant Numbering Systems to Accelerate Solution of Linear Algebraic Equation Systems."

Application of redundant homogenous numbering systems with integral, rational and irrational bases to accelerate solution of linear algebraic equation systems by a modified simple iteration method is examined. Refs: 2 titles.

UDC 681.325.6

Kirsanov, E. Yu., "Selection of the Structure of One Class of Threshold Element Memories."

Superoperational memories employing grouped serial recordings are interpreted as systems consisting of N^* digit recognition systems. Some characteristics of the structural organization of superoperational memories based on threshold elements are examined, and their design features are explained. A block diagram of such a superoperational memory is presented. 2 figs. Refs: 3 titles.

UDC 621.376.56+612+577.3

Dets', G. D., "Delta-Modulator Model of Reception."

The possibility of simulating a biological sensor by a known technical device--a delta-modulator--is demonstrated. 3 figs. Refs: 4 titles.

UDC 621.372.54

Gurenko, V. N., "Estimation of the Extreme Values of Approximation Parameters in the Design of Some Classes of Frequency-Range Filters."

A procedure is described for preliminary estimation of approximation parameters, obtained as a result of calculating the extreme values, for three basic classes of filters (Butterwort's, Chebyshev's and elliptic) permitting design of the optimum filter of the given class, and an example of the calculations is presented. 1 fig. Refs: 7 titles.

UDC 681.325.5

Simak, L. A., "Construction of Digital-Analog Cathode-Ray Displays."

The method and circuit engineering are shown for display of digital-analog information, obtained by electronic simulation, on the screen of a cathode-ray tube. 1 fig. Refs: 2 titles.

UDC 681.142-523.8

Gumen, N. B., "A Modification Method for Solution of Piecewise-Linear Equations."

A new method is examined for calculating the solutions of piecewise-linear equations based on solution correction and calculated at previous iterations. The effectiveness of the method is evaluated, and it is compared with other approaches oriented at solving problems of this type. 2 tables. 1 fig. Refs: 6 titles.

11004
CSO: 1863/49

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