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13 May 1982

USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 9/82)

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EXCERPTS FROM 'COMPUTER ENGINEERING'

CONTENTS

UDC 681.3(075)

COMPUTER ENGINEERING

Moscow VYCHISLITEL'NAYA TEKHNIKA in Russian 1981 (signed to press 27 Feb 81) pp 1-343

[Annotation, introduction and selected passages from the book "Computer Engineering" by Nikolay Aleksandrovich Mitreykin, Valeriy Pavlovich Feoktistov and Vladimir Il'ich Zelenkov, published under auspices of USSR Ministry of Higher and Secondary Specialized Education for use as a textbook in the technical high schools, Izdatel'stvo "Transport", 18,000 copies, 344 pages]

[Excerpts] A study is made of the arithmetic and logical principles of the computers in the unified system, the element base, the primary functional and structural diagrams of the assemblies and circuits of the unified system of computers and their operation, data and instruction formats, the structural principles of the data input-output system and the computer system interface. The structural design and operating principles of the peripheral devices of the unified computer system are described, and information is given on the monitoring and preventive work during operation and maintenance. The fundamentals of technical maintenance and repair of the unified system of computers at the computer centers are investigated separately.

The textbook is designed for students of technical high schools, and it can also be useful for specialists working on computers.

There are 226 illustrations, 25 tables and 17 references.

The book was written by N. A. Mitreykin, Chapters 4 to 14; V. P. Feoktistov, Chapters 15 to 20; and V. I. Zelenkov, the introduction and Chapters 1 through 3.

The reviewers were V. M. Fokin and G. V. Zubareva.

INTRODUCTION

The third generation computers in operation in the USSR and in other socialist countries are built by the united efforts of eight member countries of the CEMA (the Hungarian People's Republic, the German Democratic Republic, Cuba, the People's Republic of Bulgaria, the Polish People's Republic, Romania, the USSR and Czechoslovakia). Six models of the first series of computers making up the unified computer system (YeS EVM) were developed in a short period of time under the supervision of the Intergovernmental Committee on Computer Engineering formed in 1969: YeS-1010 (Hungarian People's Republic), YeS-1020 (People's Republic of Bulgaria, USSR), YeS-1021 (Czechoslovakia), YeS-1030 (Polish People's Republic, USSR), YeS-1040 (German Democratic Republic), YeS-1050 (USSR). The industrial production of the indicated models of the unified system of computers was started in 1972. The YeS-1022 and YeS-1033 computers were developed somewhat later in the USSR. In parallel with the creation of models of the unified system of computers in the new series (series 2) reflecting the next phase of development of microelectronics, the countries of socialist cooperation began work in 1974 on the minicomputer system (SM EVM) program.

Models of the second series are the YeS-1011, YeS-1015 (Hungarian People's Republic), YeS-1025 (Czechoslovakia), YeS-1035 (People's Republic of Bulgaria), YeS-1045 (USSR), YeS-1055 (German Democratic Republic), the SM EVM [minicomputer system], SM 1, SM 2, SM 3, SM 4 (USSR), SM 52/10 (Hungarian People's Republic). The models of the SM EVM constitute a new family of modular computer engineering means designed for operation in control systems. They are constructed on a modern element base, they have higher speed (240,000 to 300,000 operations per second) and greater on-line memory capacity, broader possibilities with respect to connecting peripheral devices compared to the M-6000 and M-7000 minicomputers produced at the present time.

The fourth generation of computers is being created on the basis of large-scale integrated circuits (LSI). The "Nairi-4" computer built on the basis of the LSI has already been put into series production, the production of fourth-generation universal multiprocessor complexes with a total output capacity of more than 100 million operations per second has been started. For the first time in the USSR, a single crystal microcomputer, the "Elektronika NTs 80," was built in 1979. This computer contains 300,000 crystal elements 6×6 mm in size. It works with 16-bit numbers at a speed of up to 550,000 operations per second. In the future, it is proposed that a 64-bit single-crystal microcomputer be built which will contain up to 1 million elements. In parallel with further improvement of

the element base and the structure of the fourth-generation computers based on LSI, a laser-based computer is being developed which makes use of glass fibers for data transmission.

Computer engineering is used broadly on railroad transportation. At the present time computer centers have been built at the road administrations, at a number of plants, several shunting yards and in the Ministry of Railways. More than 70 different types of planning, accounting, monitoring and analysis problems are solved at these computer centers. The automated "Ekspress" system is operating successfully in the Moscow Railroad Network for reserving and selling railroad tickets. A transition is being made from solution of individual problems on computers to integrated processing of information obtained from transport documents especially adapted for this purpose.

Since 1971 railroad transportation has been working on the creation and introduction of a branch automated control system (ASUZhT) which must provide for automated gathering and processing of the information needed to optimize the control of the railroads and enterprises of the Ministry of Railways. The ASUZhT [automated railroad transportation control system] is a subsystem in the national automated data gathering and processing system for accounting, planning and control of the national economy of the USSR (OGAS).

The development and introduction of the ASUZhT is divided into three phases. The first phase was introduced on the railroads in 1975. It was based on the second-generation computers and subscriber telegraph network operating at a transition speed of 50 bits/sec. In the first phase the ASUZhT includes about 30 standard medium range and operative planning problems and the control of freight shipments, some problems of statistical and bookkeeping accounting, the administration of the operations of the Ministry of Railroads, and so on.

The second phase (1980-1985) presupposes the creation of up to 30 junction computer centers (UVTs) in addition to the road computer centers and the main computer center of the Ministry. The number of solved problems will increase to approximately 150 in 1980 and 300 in 1985. During construction of the second phase, information banks must be created, including a dynamic data file on the location and condition of each unit of rolling stock (cars, locomotives, trains). During introduction of the second phase of the ASUZhT the plan calls for beginning the application of automated reading of information from moving rolling stock.

The third phase of the ASUZhT requires still higher output new-generation computers and data transmission means. It will be characterized by further expansion of the number of solved problems (to approximately 500) and interpretation of them, introduction of automated information reading from the rolling stock and other means of automatic primary data gathering. During this period, message switching centers have been developed which permit more flexible and efficient use of the unified data transmission network. The creation of the UVTs and VTs [computer centers] at the large plants and the group collective-use computer centers for servicing a group of enterprises will be completed. The "brain" terminals (data transmission systems equipped with a minicomputer) are being developed. The YeS-1010, YeS-1011, YeS-1020, YeS-1022, YeS-1030 and YeS-1033 and also individual models of the modular computer hardware (ASVT-M and SM EVM) are used as basic data processing and control devices on the railroad.

CHAPTER 3. ELEMENT SYSTEM OF THE UNIFIED SYSTEM OF COMPUTERS

In the lower-end models of the unified system of computers (YeS-1022 to YeS-1040) and in the majority of peripheral devices, integrated transistor-transistor logical circuits (TTL) series 155 are used. The control units for the input-output devices and the storage elements of all models are created on the basis of the series 155 TTL-circuits.

In the more powerful models of the YeS-1050 and YeS-1060 in the processors and channels, series 137 and 187 logical circuits based on current switches with combined emitters (emitter-coupling transistorized logical circuits -- ESTL-circuits) -- are used. The emitter-connected logic is the systems engineering type bipolar unsaturated integrated logical circuit in which the emitters of the input logical transistors are connected to the emitter of a reference transistor. Both the TTL-circuits and the ESTL-circuits are built from silicon plates by planar-epitaxial technology. Silicon plates with microcircuits are placed in sealed plastic rectangular housings with 14 pin leads. The housing dimensions are 20×7×4 mm.

The first structural level of the computer -- the standard replacement element or card (TEZ) (Figure 3.3) -- is based on integrated circuits. The TEZ is a functional unit of the computer, its basic module. Two types of TEZ have been developed. One of them contains 24 integrated circuits based on the two-way printed circuit board. Another -- designed for computers with higher output capacity -- is built from a multilayered printed circuit board on which it is possible to locate 72 integrated circuits.

The next structural level is the panel with 40 first or second type TEZ. The panels (usually six of them) are placed on a frame. The last structural level is the rack on which three frames are mounted, the middle frame stationary and the ones on the edges on hinges, which insures easy access to the wiring elements.

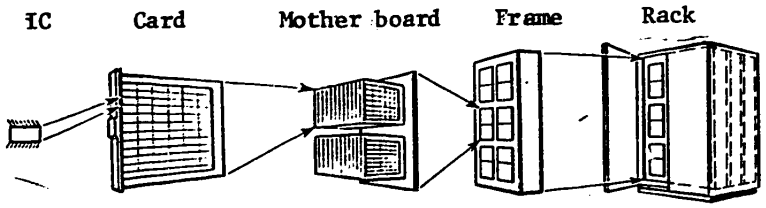

Figure 3.3. Standardized structural elements of the unified system of computers

3.2. Integrated Circuits Used in the Unified System of Computers

Transistor-Transistor Logical Circuits. The base element of integrated circuits TTL is the AND-NOT type logical element (Figure 3.4, a and b). It includes a two-emitter transistor T1 forming the AND circuit with two inputs and a complex inverter created from the transistors T2 to T4, the diode D and resistors R2 to R4. For a feed voltage E_k of +5 volts, the high input voltage level $U_1 \geq +2.4$ volts (corresponds to code 1), and the low input voltage level $U_0 \leq +0.4$ volts (corresponds to code 0). The voltages U_a and U_b fed to the inputs of the element vary within the same limits. There are different versions of base elements in which the input transistor T1 contains 3, 5 or 8 emitters, on the basis of which the input coincidence circuit has the corresponding number of inputs.

If voltage levels U_1 corresponding to 1 are fed to all the emitters of the transistor T1 (see Figure 3.4, a), then the base-emitter junction is shifted in the return direction and closed, and the base-collector junction is shifted in the forward direction and opened. The forward current of the base of the T2 transistor flows through the resistor R1 and the open base-collector junction. The transistor T2 is opened by this current, and it goes into the saturation mode. Simultaneously the transistor T4 from which the output inverter is executed opens completely. The low output voltage level U_0 (code 0) is picked up from the collector of transistor T4.

In this case transistor T3 is in the closed state. This state is insured by a low voltage level set up on the collector of the transistor T2. The diode D1 is used for reliable blocking of T3.

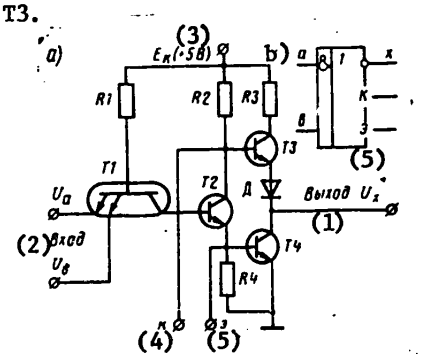

Figure 3.4. AND-NOT element: a -- circuit diagram; b -- legend
Key: 1. output U_x; 2. input U_B; 3. E_k (+5 volts); 4. k=collector; 5. E=emitter

With transistor T4 open, a voltage is set up on its collector which corresponds to the level 0 (0.1 to 0.4 volts), and on the collector of the open transistor T2, the voltage $U_{kT2}=U_{b.eT4}+U_{k.eT2}=$(0.8 to 1.1) volts. The difference between the collector voltages of transistors T2 and T4 is less than 0.7 volts. This voltage drop is insufficient to block the base-emitter junction of transistor T3 and the diode D inasmuch as the response threshold of each of them is about 0.7 to 0.8 volts.

The circuit is switched to the state in which the high voltage level U_1 (code 1) is set up at the output if at least one of the emitters of the transistor T1 is fed a low level voltage U_0. Here the corresponding base-emitter junction of transistor T1 is shifted in the forward direction, its base current is switched to the emitter circuit, and the transistor T1 goes into saturation. The resistance of the collector-emitter junction of the transistor T1 drops sharply, which blocks the transistor T2. Consequently, transistor T4 is also blocked. Transistor T3 is opened, for the collector voltage of the closed transistor T2 approaches the feed voltage E_k. With open transistor T3 the output voltage U_{out} becomes equal to U_1 (code 1). Thus, the circuit realizes the AND-NOT logical function: $x = \overline{a \wedge b}$, where the logical variables a, b, x correspond to the values of the input and output voltages U_a, U_b, U_x. Additional inputs k (collector output) and e (emitter output) permit the construction of the AND-OR-NOT logical circuits expanded with respect to the OR input (Figure 3.5) (the LR logical elements). The same outputs of the logically connected circuits (LP) (expanders with respect to the OR inputs) are connected to the logical elements LR. As a result of parallel inclusion of the transistors T2, the LR and LP elements, a circuit is obtained which realizes the logical function $x = \overline{ab \vee cd}$.

Using the jointly expanded and connected circuits with different combining coefficients m and l, respectively, with respect to the AND and OR inputs, it is possible to realize functions expressed in the form of a disjunction.

The set of series 155 integrated circuits includes a significant number of versions characterized by different technical and electrical parameters.

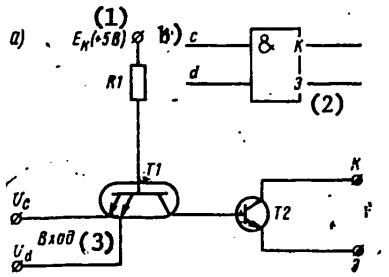

Figure 3.5. Input logic expander of the TTL element:
a -- circuit diagram; b -- legend

Key:
1. (+5 volts)
2. E
3. input

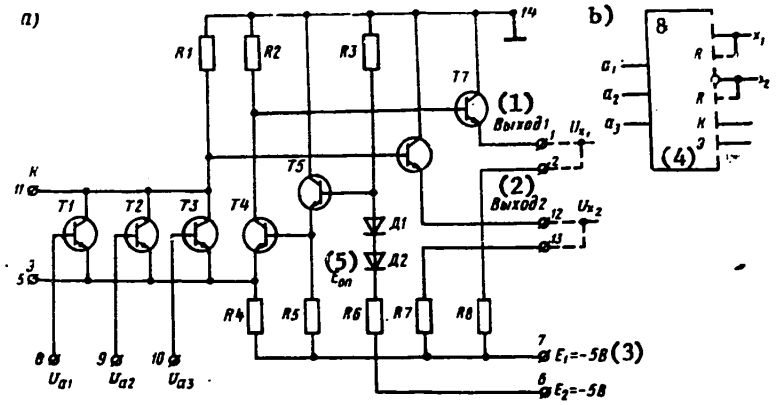

Figure 3.6. Three-input ESTL element:
a -- circuit diagram; b -- legend

Key:
1. Output 1
2. Output 2
3. -5 volts
4. E
5. E_{ref}

Emitter-Connected Transistorized Logical Circuits (ESTL). The functional base of the logical circuits based on current switches is the AND and AND-NOT type elements with paraphase outputs (Figure 3.6, a and b). The input half of the current switch of the element is executed from T1-T3 transistors, and the other half, from the T4 transistor. The source of the reference voltage E_{ref} consists of the transistor T5, the diodes D1, D2 and resistors R3, R5, R6. The output signals are put out through the emitter repeaters executed from the transistors T6, T7 and resistors R7 and R8. With feed voltages $E_1=E_2=-5$ volts, the circuit is switched by signals coming to the input, and it outputs output signals which vary from $U_0=-(0.7$ to $0.95)$ volts to $U_1=-(1.45$ to $1.9)$ volts.

The circuit is switched by input signals with amplitude $+(0.25$ to $0.4)$ volts and $-(0.25$ to $0.7)$ volts which are symmetric with respect to the reference voltage level $E_{ref}=-1.2$ volts.

For low voltage level at all inputs 8, 9 and 10 (see Figure 3.6, a) the transistors T1, T2, T3 are closed, and the transistor T4 is opened. This state is sustained until the high level signal U_0 reaches the base of any of the transistors T1, T2 or T3. In this case the transistor, to the input of which the high level signal has come, opens, and the transistor T4 is blocked, and the current flowing through it flows through the open input transistor.

In silicon transistors the voltage drop at the base-emitter junction is (0.7 to 0.8) volts. For a voltage drop of 0.7 volts and input signal $U_0=-0.95$ volts on the emitters of the transistors T1 to T4, the voltage will be $U_0-U_{b.e}=-0.95$ to $0.7=1.65$ volts. In this case the difference between the reference voltage and the voltage on the emitters of the transistors T1 to T4, $E_{ref}-(U_0-U_{b.e})=-1.2+1.65=0.45$ volts is insufficient to block transistor T4, for its response threshold

is 0.7 to 0.8 volts. If the transistor T4 is open, the voltage difference $E_{ref}-U_{b.e}=-1.2-0.7=-1.9$ volts is present on the joined emitters. The obtained result will occur when signals of the levels $U_1=-1.45$ volts are fed to all the inputs. The obtained potential difference will in this case be insufficient to block the transistors T1, T2, T3, for $U_1-(E_{ref}-U_{b.e})=-1.45+1.9=0.45$ volts. In the investigated circuits the transistors operate in the unsaturated mode; therefore the ESTL have high speed by comparison with other types of digital elements.

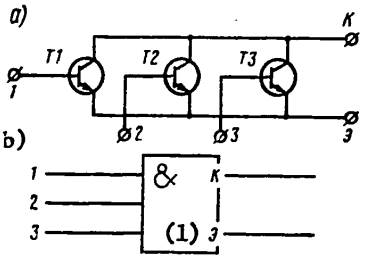

Figure 3.7. Input logic expander of the ESTL element:
a -- circuit diagram; b -- legend
Key:
1. E=emitter

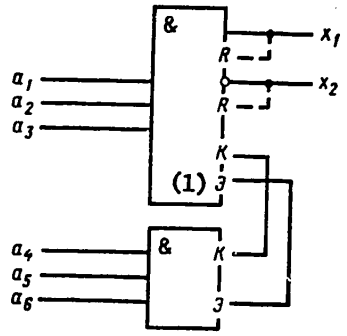

Figure 3.8. Circuit diagram of the input logic expander
Key:
1. E

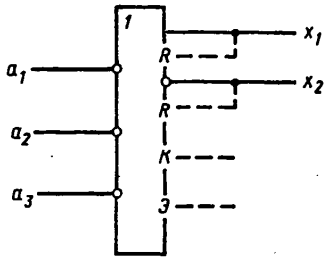

Figure 3.9. Provisional representation of OR, OR-NOT elements

The output emitter repeaters that shape the output signals and insure high load capacity of the elements ($K_{dec}<15$) are used for decoupling between the current switches and the load and also insure symmetry of the output signals with respect to the reference voltage level. Taking low potential levels U_1 corresponding to code 1 and high potential levels U_0 corresponding to code 0, we obtain the logical coupling of the first output circuit (terminals 1, 2) to the inputs by means of the relation $x_1=a_1a_2a_3$, and the second output (terminals 12, 13) to the inputs by means of the relation $x_2=a_1a_2a_3$, where a_1, a_2, a_3, ... correspond to U_{a1}, U_{a2}, U_{a3}; x_1, x_2, ... correspond to U_{x1}, U_{x2}, ... From the presented relations it follows that $x_2=x_1$.

The number of inputs can be increased as a result of the expanders. Figure 3.7 shows the diagram of a three-input expander. In order to increase the number of inputs on the AND, AND-NOT type circuit, one or two three-input expanders with k and e terminals on each are connected to the same terminals of the current switch (Figure 3.8). The maximum number of inputs for elements of both types can reach 9 in this case.

The elements assembled from current switches can also correspond to the logical circuits OR, OR-NOT if code 1 is placed in correspondence to the high potential level, and code 0, the low potential level. In this case the inputs are depicted as the inverse (Figure 3.9). The output variables x_1 and x_2 shown in Figure 3.9 will be related to the input variables a_1, a_2, a_3 by logical expressions

$x_1 = \bar{a}_1 \vee \bar{a}_2 \vee \bar{a}_3$ and $x_2 = \overline{\bar{a}_1 \vee \bar{a}_2 \vee \bar{a}_3}$. From these relations it follows that $x_2 = \bar{x}_1$.

CHAPTER 4. UNIFIED COMPUTER SYSTEM ASSEMBLIES

The assemblies of the YeS-1010, YeS-1020, YeS-1022, YeS-1030, YeS-1040 computers of the unified system are executed from TTL elements. They contain AND-NOT, AND-OR-NOT cells, OR expanders, RS, D, JK type flip-flops, and so on. The application of two-step AND-OR-NOT logic promotes increased speed of the computer by reducing the equipment and the connections.

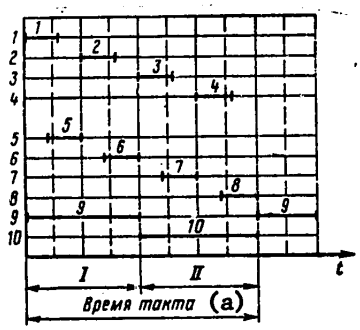

Figure 4.1. Time diagram for the shaping of clock pulses:
1 -- S1, TI1; 2 -- S2, TI2; 3 -- S3, TI3; 4 -- S4, TI4;
5 -- Si2, TI12, 6 -- S23, TI23; 7 -- S31, TI31; 8 -- S41, TI41;
9 -- halfcycle pulses I; 10 -- halfcycle pulses II

Key:
a. cycle time

Each microoperation is executed using a special signal generated by the computer control unit and sent at the required time to the corresponding control bus. Acting on the electronic circuit connected to this bus, the control signal (US) actuates the circuit, as a result of which the given microoperation is performed. The time spent on performing one or several microoperations simultaneously is called a cycle. A computer cycle usually consists of a series of US providing for the required operating sequence of individual functional assemblies during execution of the microoperations.

In the computers of the unified system the cycle is determined by the ROM [read only memory] cycle time (the ROM is one of the storages of the computer where micro-instructions for the execution of microoperations are stored). For example, in the YeS-1022 computer, a cycle is equal to 600 nanoseconds (Figure 4.1), and it contains two series of basic (S1, S2, S3, S4 and TI1, TI2, TI3, TI4) and delayed (S12, S23,

S34, S41 and TI12, TI23, TI34, TI41) sync pulses following each other after 125 nanoseconds. The pulses are generated by a special assembly of the computer -- the synchronizer or timing unit. The basic and delayed series S pulses are generated constantly, and the TI series pulses can be started as needed or stopped by a special start-stop circuit. In addition, the timing unit generates potentials: halfcycle I, halfcycle II. All of the enumerated pulses are designed for starting and synchronizing the operation of the computer assemblies and units.

4.7. Code Comparison Assemblies

Several versions of the code comparison operation are used in computers: comparison with respect to modulus, comparison with consideration of the signs of the numbers, comparison of the orders of the numbers. The most complete is the comparison operation in which the fact of satisfaction of one of the following conditions is established:

$$X = Y,\ X > Y,\ X < Y.$$

Two methods of executing comparison operations have become the most widespread. The first method consists in the fact that one number is subtracted from the other, and the sign of the remainder is used to determine whether the last two indicated conditions are satisfied. In the second method the subtraction operation is performed by an adder with a circuit for holding the zero code of the remainder which is obtained when X = Y. This procedure is inexpedient from the point of view of additional load on the computer adder. Therefore in the unified system of computers special combination coincidence circuits are used. These circuits can be used to perform three, two or one of the following three functions:

$$F_1(X,Y)=\begin{cases}1 & \text{for } X=Y,\\ 0 & \text{for } X\neq Y,\end{cases}$$

$$F_2(X,Y)=\begin{cases}1 & \text{for } X>Y,\\ 0 & \text{for } X\leqslant Y,\end{cases}$$

$$F_3(X,Y)=\begin{cases}1 & \text{for } X<Y,\\ 0 & \text{for } X\geqslant Y.\end{cases}$$

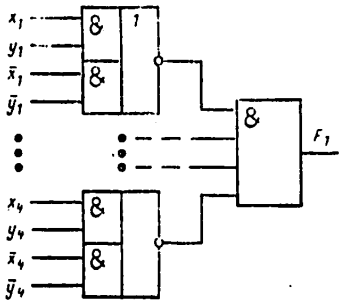

Figure 4.22. Code equality circuit of the YeS-1022 computer

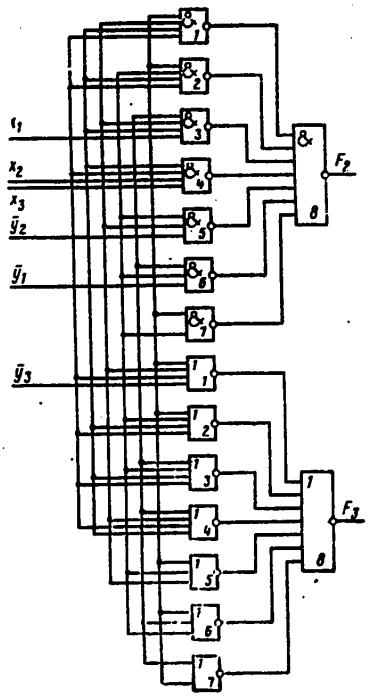

Figure 4.23. Circuit for performing the function of comparing F_2 and F_3

In practice it is frequently required that only one of the functions be performed. The circuit performing the function F_1 is called the code equality circuit. The code equality circuit illustrated in Figure 4.22 is used in the memory protection module of the YeS-1022 computer.

The operation of the circuit executing comparison functions F_2 and F3 is easily followed by sending the bits of the two compared three-bit binary codes to its corresponding inputs (Figure 4.23).

CHAPTER 6. ON-LINE AND READ ONLY MEMORIES OF THE UNIFIED SYSTEM OF COMPUTERS

The on-line storage is distinguished by high speed (access time 0.3 to 10 microseconds), relatively small capacity (10^5 to 10^7 bits) and complexity of electronic equipment. Ferrite cores and thin magnetic films are used as the memory element in the on-line storage of the computers of the united system. The speed of the on-line memory must correspond to the operating speed of the central processor.

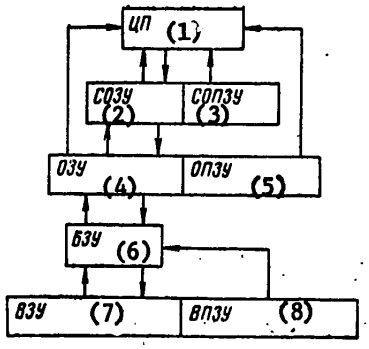

Figure 6.1. Memory structure of modern computers

Key:

1. TsP = central processor
2. SOZU = rapid-access storage
3. SOPZU = rapid-access ROM
4. OZU = on-line memory
5. OPZU = on-line ROM
6. BZU = buffer memory
7. VZU = external memory
8. VPZU = external ROM

Rapid-Access Memory (SOZU). The high speed of the logical elements permits the creation of arithmetic-logic units (ALU) that perform operations in fractions of a microsecond. The speed of the OZU (on-line memory) in this case limits the speed of performance of the operations in the computer. This limitation can be removed by introducing the SOZU. The access time of the SOZU is 20 to 500 nanoseconds, and it differs little from the ALU speed. The SOZU stores intermediate calculation results and information used repeatedly in the current phase of the calculations, which it is inexpedient to send to the OZU. The SOZU is included between the ALU and OZU. The SOZU has small capacity -- 10^2 to 10^4 bits. The SOZU is constructed from integrated circuits, semiconductor devices and thin magnetic films.

Buffer Memory (BZU). A medium-size (10^7 to 10^8 bits) and medium-speed (t_{access} from 0.1 to 10 microseconds) BZU is used to match the operating speeds of the slow VZU [external memory] and fast OZU [on-line memory] in the computer. Usually memories made of ferrite cores or magnetic drums are used as the BZU.

6.6. Thin Magnetic Film Memories

A layer of magnetic material, the thickness of which does not exceed the domain dimensions is called a thin magnetic film (TMP). The primary characteristic of the TMP is short remagnetization time, which permits construction of a high-speed memory with access time to several tens of nanoseconds. Films 0.05 to 0.15 micron thick have found practical application in computer engineering. As a result of their small thickness, the magnetization vector is in the plane of the film. The TMP used in memories are divided into plane and cylindrical.

Plane TMP Memories. Memory elements based on plane TMP are segments of magnetic film rectangular in shape with a system of control wires. The plane magnetic films are made by electrolytic deposition of magnetic metal vapor in a vacuum on heated glass or metal nonmagnetic plates (substrates). Iron and nickel films (Fe≈20%; Ni≈80%) have found the greatest application. The process of applying a magnetic film is carried out in a strong magnetic field. The effect of the magnetic field and the elongated shape of the film lead to the fact that the magnetic properties of TMP in different directions turn out to be different, that is, the film is anisotropic.

6.7. Read-Only Memory

Structural and Operating Principle. In young and middle generation models of the unified system of computers, read-only memories (ROM) are used to store the processor control microprograms. The ROM is used only to store and output information; therefore it is significantly simpler, cheaper and more reliable than the on-line memory, for it has no write circuit, and simpler and cheaper memory elements are used to store the information. The ROM is constructed by the 2D structure on diode matrices, MDS-transistors and ferromagnetic elements.

Let us consider the structural and operating principles of the transformer type ROM. Ferrite cores with nonrectangular hysteresis roots operating as line transformers are used as memory elements in this ROM. A number scale serves as the base for constructing the transformer type ROM. Figure 6.11, a shows the number scale made of four transformers. It is designed to store three four-bit binary numbers. Here each ferromagnetic core (FS) is used to store like bits of all storing numbers. The role of the primary (input) winding of the transformers of the number scales is played by a coordinate bus. The wires are woven through the cores in accordance with the information content of the stored numbers. If code 1 must be stored in a given bit of the stored number, then the wire passes through the core; if 0 is to be stored in the given bit, the wire goes around the core. For reading information each core has an output (secondary) winding. The number is read by sending an interrogation current pulse to the selected input bus. An emf is induced in the output windings of the cores through which this bus is woven, and there is no signal in the output windings in which the bus is not woven.

On the circuit diagrams the number scales are depicted simply (Figure 6.11, b). The intersection of the buses and the core is indicated by a short sloping line. If the bus bends around the core, the sloping line is absent.

In the transformer ROM, U or W type cores of split design are used, which permits automation of the process of making the number scales. The following advantages are promoting widespread use of transformer ROM: simplicity of the structural execution of the memory module; high write density permitting construction of large-size ROM (from several hundreds to several tens of thousands of words); high efficiency caused by low losses in the transformers; high read signal level; relatively high speed (the access time can be several tenths of a microsecond) and reliability. The deficiencies of the transformer ROM include difficulty of making them by the methods of integrated technology and the necessity for applying special (nonstandard) control circuits.

Structure. The basic component parts of the ROM, for example, the YeS-1020 (Figure 6.12) are the memory module (BP), address register (RAPP), address decoder (DShA), read amplifier assembly (US), microinstruction register (RMK), check station (UK) and local control module (BMU).

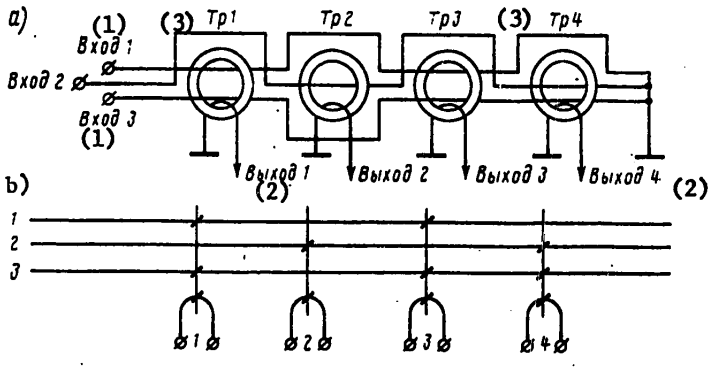

Figure 6.11. Number scale:
a -- structural principle; b -- simplified representation

Key:
1. Input ...
2. Output ...
3. Transformer

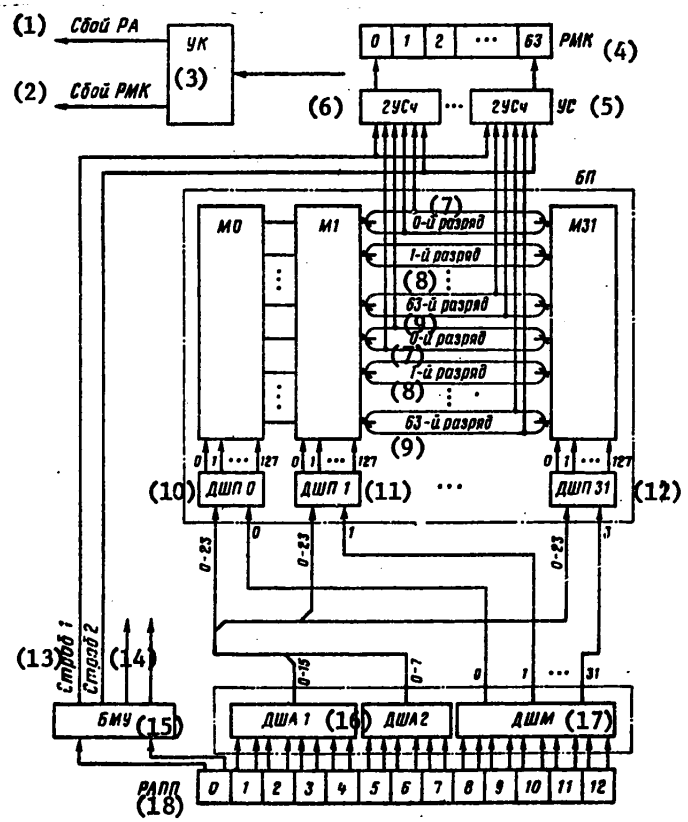

Figure 6.12. Structural diagram of ROM

Key:

1. Address register error
2. Microinstruction register error
3. UK = check station
4. RMK = microinstruction register
5. US = read amplifier assembly
6. 2 read amplifiers
7. 0 bit
8. 1st bit
9. 63d bit
10. DShP = wire decoder No 0
11. Wire decoder No 1
12. Wire decoder No 31
13. Gate 1
14. Gate 2
15. BMU = local control module
16. DShA = address decoder
17. DShM = memory module decoder
18. RAPP = address register

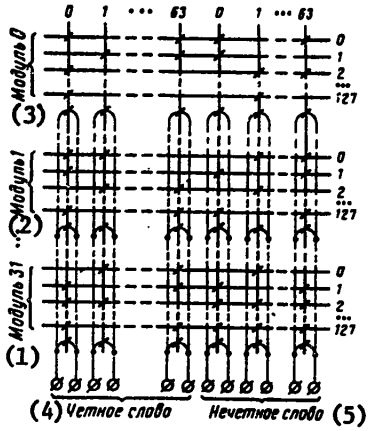

Figure 6.13. Memory module

Key:

1. Module 31
2. Module 1
3. Module 0
4. Even word
5. Odd word

The BP [memory module] (Figure 6.13) consists of 32 number scales, called memory modules. One module is designed to store 128 words 128 bits long each, and it contains 128 FS [ferromagnetic cores] woven by 128 input buses in accordance with the information content of the stored numbers. Each FS stores 1 bit of all 128 words and is equipped with a separate read winding. The read windings of like bits of all memory modules are connected in parallel. On referencing the ROM, a 128-bit word is read from a selected module. The 128-bit word is transmitted to other units of the computer in 64-bit words; therefore the read word is broken down into two machine words -- even and odd. The capacity of the investigated BP is 128×32=4096 words.

The RAPP is a 13-bit flip-flop address register designed to receive, store and output the addresses of the even and odd words.

The DShA realizes preliminary decoding of the address of the read number (it determines the wire decoder number -- DShP). It consists of the decoders DShA1 and DShA2 and the memory module decoder DShM. The decoders are controlled by signals coming from the first to the fourth, fifth to the seventh and eighth to the 12th bits of the RAPP, respectively. The DShM determines the number of the selected memory module (the decoder DShP) and has 32 outputs (with respect to number of ROM modules). The DShA1 and DShA2 decoders provide for selection of the input winding in the selected mode. The DShA1 has 16 outputs (from 0 to 15), and the DShA2 has 8 (from 0 to 7).

The DShP0, DShP1,..., DShP31 form the second decoding stage and are designed for shaping the interrogation current pulse in the selected input winding of the selected module. Each DShP has 128 outputs.

The US [read amplifier assembly] is designed for separating even and odd words, amplifying and shaping the code pulses. The US consists of 64 like channels, each of which has two independent read amplifiers (USch). One of them receives a bit of an even word, and the other, an odd word. The decision to transmit an even word is realized by a "gate 1" pulse, and an odd word, a "gate 2" pulse.

The RMK is the microinstruction register for receiving microinstructions from the BP, storing them and outputting them to the processor units. It has 64 bits, of which 62 (from the 0 to the 61st bit inclusively) are information bits, and two bits (the 62d and 63d) are check bits.

The UK is the check station which checks for odd parity of the RAPP and RMK registers. On detecting an error the UK shapes and outputs the RA error or RMK error signal to the processor check station.

The BMU is the local control module designed to shape and feed control pulses to the ROM assemblies and modules at required points in time.

The ROM of the YeS-1022 computer has the same structure, but the BP contains 24 modules.

CHAPTER 7. PROCESSOR

Mixed control is a compromise solution using the positive qualities of synchronous and asynchronous processors. The practical implementation of this principle has been achieved on the "Minsk-34," YeS-1050 and YeS-1060 computers. All of the operations performed in the processor are broken down into several groups with respect to complexity and duration. The execution of the simplest operations included in one group is realized in the synchronous mode. The most complex operations, for example, division and multiplication, are realized in the asynchronous mode. Thus, computers with mixed circuit control operate in the synchronous-asynchronous mode and are economical and the most widespread.

Microprogramming is receiving broad application and is used, for example, in the "Mir," "Nairi," YeS-1010, YeS-1020, YeS-1022, YeS-1030, YeS-1033 and YeS-1040 computers.

7.2. Structure of a Processor with Microprogram Control

A standard processor structure has been developed for all computers of the unified system. The distinguishing feature of processors of different computers is that in center models of the unified system the basic core storage (OOP) and the input-output channels are a part of the processor, and in others, they are in separate units. The processors are also distinguished by the method of organizing the computation process.

Figure 7.2 shows the generalized structure of a processor using the microprogram method of controlling the commutation process. The processor includes the following: the OOP -- basic core storage; ALU -- arithmetic-logic unit; TsUU -- central control unit; BR -- register module; SVV -- input-output system.

The OOP [basic core storage] is an ordered series of numbered bytes. In one access to the OOP in different models of the unified system of computers, a different number of bytes is selected simultaneously, called the access width. The access width of the YeS-1040 computer is 1 byte, the access width of YeS-1022 and YeS-1033 is 4 bytes, and for the YeS-1050 and YeS-1060, 8 bytes. The access time to the OOP fluctuates from 0.8 (for the YeS-1033) to 2.4 (for the YeS-1022) microseconds.

A characteristic feature of the logical organization of the OOP of the models of unified system of computers is use of dynamic memory distribution in which the segregation of the memory cells for the information files is not done in advance, but during the problem solution process. The dynamic principle is based on

page organization of memory by which physical blocks (pages) of fixed size (usually 2048 bytes each) are isolated. In addition, segmentation of the memory is provided for consisting in dividing all the pages into groups (segments) with independent addressing of the words within each group. Therefore the address of any word must contain three component parts: the segment number, page number and the address within the page.

The OOP can be segmented beginning with the purpose of its different regions. For example, the OOP of the YeS-1022 computer is divided into three logically independent types of memory: basic (OP), multiplex (MP) and local (LP) (see Figure 7.2).

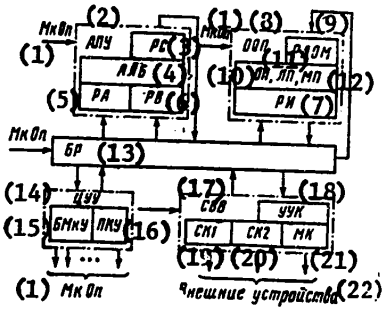

Figure 7.2. Structure of processors with microprogram control

Key:

1. MkOp = microoperator
2. ALU = arithmetic-logic unit
3. RS = output register
4. ALB = arithmetic-logic module
5. RA = input register
6. RB = input register
7. RI = information register
8. OOP = basic core storage
9. RAOM = common address register
10. OP = basic memory
11. LP = local memory
12. MP = multiplex memory
13. BR = register module
14. TsUU = central control unit
15. BMkU = microprogram control module
16. PKU = monitoring and control panel
17. SVV = input-output system
18. UUK = channel control unit
19. SK1 = selector channel 1
20. SK2 = selector channel 2
21. MK = multiplex channel
22. Peripheral devices

The OP is used for storing the working programs and operands. It is constructed from small FS according to the structure of 2.5D. A study is made of three versions of memory size: 128, 256 and 512 k/bytes. The memory cycle is divided -- read and write (regeneration) 1.2 microseconds each. The control information of the multiplex channel is put in the MP. The memory size is 2048 bytes (for all three versions of OP). The OP and MP are physically made as a single memory.

The LP is a rapid-access memory (SOZU). In the YeS-1022 computer, it is made from integrated circuits in the form of a separate module. It is called the working bank of the central processor which is used to store operands used in the given operation, immediate results, program state words (SSP), under the control of which the current program is executed, and so on.

The capacity of the LP is 256 20-bit words (2 working bytes, 2 reserve bits). The speed is twice the speed of the central processor. The presence of this memory has made it possible to increase the speed of the processor.

The OP and the MP are accessed through a common address register RA0M. Information exchange between the OOP and other units of the computer is realized through the information register RI. In the YeS-1022 computer, the local memory LP is assigned its own registers. The word length of the registers is determined by the access width.

The ALU of the processors execute all the arithmetic and logical operations, the set of which is determined by the instruction system of the unified system of computers. All models of the computers of the unified system are designed to perform a unique set of operations, including operations on the operands with fixed point and floating point, on fields of variable length and on decimal numbers. The basic units of the ALU (see Figure 7.2) are as follows: RA and RV -- input registers; RS -- output register; ALB -- arithmetic logic unit. Basic characteristics of the ALU: speed and combination of possible operations performed by the ALU.

The BR stores and outputs various information participating in the program execution process. The BR includes address registers, the common use registers and special purpose registers. The address registers store the addresses of the instructions in the operands and also any other information. The common use registers store information participating in the execution of the microprograms. The special (service) purpose registers store information reflecting the state of the units and assemblies of the computer when executing the programs.

The TsUU is designed for automatic control of the computation process. It provides coordination of the operation of all units of the computer with the help of synchronizing and controlling signals generated during the process of executing the program. The TsUU performs the following basic functions: it organizes automatic input of the initial data and the program, output of the results of solving the problem and any other information; it selects program instructions from the OOP in the required sequence and provides for execution of them; it selects the required information from the OOP and transmits it from certain types of memory to others; it monitors the functioning of the computer units. The TsUU includes the microprogram control module BMkU, the check stations, the monitoring and control panel PKU. The BMkU is designed to organize the computation process in the computer. The LKU is used to identify the state, monitor and assign the operating conditions of the central processor. The computer is started, the course of the computations are monitored, operator intervention in the computation process and program checkout are all realized from the PKU.

The SVV provides communications with the peripheral devices of the computer and contains the channel control unit UUK, two selector channels (SK1 and SK2), and one multiplex channel (MK) and the input-output interface.

7.3. Microprogram Control Module

The BMkU [microprogram control module] includes the following (Figure 7.3): read-only memory (ROM), address register (RAPP) and microinstruction register (RMK), address decoders (DShA) and microinstruction decoders (DShMK), the assembly for forming the address of the next microinstruction (UFAMK) and the assembly for entering the codes in the address register of the ROM (UZAN RAPP).

The microprogram control principle consists in successive reading of the microinstructions of the given microprogram from the ROM and converting them by means of the DShMK to control signals (microoperations -- MkOp). Horizontal and vertical microprogramming are distinguished by the method of forming the control signals (US). In the case of horizontal programming, the microprogram can be represented in the form of a matrix (Figure 7.4), in which each row corresponds to one microinstruction, and a column corresponds to one microoperation (1 US). Code 1 at the intersection of a row and a column corresponds to sending a US in the given microinstruction, and code 0, absence of US.

The advantages of horizontal microprogramming are the possibility of simultaneous execution of several microoperations (if ones are placed in several bits of the microinstruction) and simplicity of forming the US (without decoding). A disadvantage of horizontal microprogramming is long microinstruction length, for the number of US in the processor of the unified system of computers can reach several hundreds. In order to store such microinstructions memory with long word length YaP is required, which is economically disadvantageous.

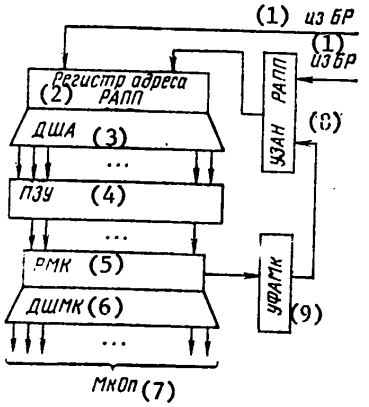

Figure 7.3. Microprogram control module
Key:
1. From the BR
2. Address register RAPP
3. DShA
4. PZU
5. RMK
6. DShMK
7. microoperation
8. UZAN RAPP
9. UFAMK

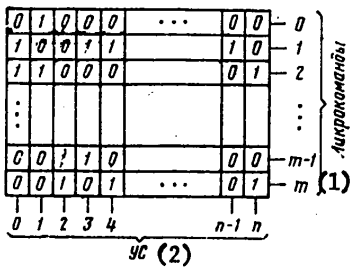

Figure 7.4. Microprogram for horicontal programming
Key:
1. Microinstructions
2. US = control signals

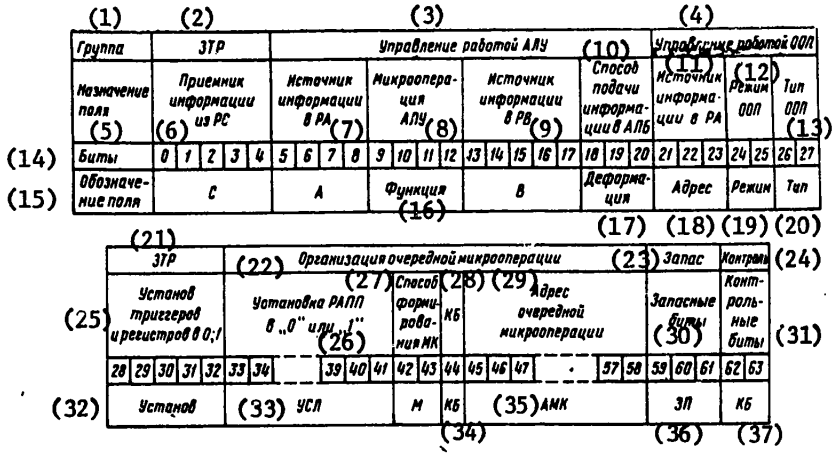

Figure 7.5. Structure of a microinstruction

Key:

1. Group
2. ZTR*
3. ALU operation control
4. OOP operation control
5. Purpose of bank
6. Reception of information from RC
7. Information source in the RA
8. Microoperation of the ALU
9. Information source in the RB
10. Method of sending information to the ALB
11. Information source in the RA
12. OOP mode
13. Type of OOP
14. Bits
15. Bank designation
16. Function
17. Deformation
18. Address
19. Mode
20. Type
21. ZTR
22. Organization of next microoperation
23. Reserve
24. Check
25. Setting flip-flops and registers to 0, 1
26. Setting RAPP to 0 or 1
27. Method of forming the MK
28. KB
29. Address of next microinstruction
30. Reserve bits
31. Check bits
32. Setting
33. USL
34. KB
35. AMK
36. ZL
37. KB

*[entering in the flip-flops and registers]

During vertical microprogramming, each microoperation is defined by a binary code. The format of the vertical microinstruction is similar to the instruction format. It contains the microoperation code and address part determining the source of the operands participating in the microoperation and the destination of the result. The different consists in the fact that a microoperation and not the operation is performed by the microinstruction, and the address part in the majority of cases defines not the memory cell, but the central processor register. In the case of parallel microprogramming the formation of the address and reading of the next instruction are carried out simultaneously with execution of the current microinstruction.

In the unified system of computers, vertical microprogramming is used. A microinstruction (Figure 7.5) is a 64-bit binary word containing fields of a defined length. Each field is assigned its independent decoder DShMK organizing up to 2^m microoperations (m is the number of bits in the microinstruction field). The fields by which the US are formed have no more than 5 bits; therefore each field defines up to 32 different microoperations. The microinstruction fields can be divided into the following six groups: control of the ALU operation (bits 5-20) -- field A, function, B, DEFORMATION; control of the operation of the basic core storage (bits 21-27) -- Address, Mode, Type fields; entry in the flip-flops and registers (bits 0-4 and 28-32) -- fields C, SETUP; organization of the address of the next microoperation (bits 33-58) -- fields USL, M, KB, AMK; check (bits 44, 62 and 63) -- field KB; reserve (bits 59-61) -- field ZP.

ALU Operation Control. The four-bit field A determines the source of information -- the process register -- from which information is fed to the input register RA of the ALU. For example, in the YeS-1020 with a code value of 0001 of this field, the information source will be the OOP [basic core storage] register RN, 0010 -- RZ, 0000 -- information in the RA remains unchanged, 1111 -- zeroes are entered in the RA and so on.

The four-bit field FUNCTION defines the microoperation which the ALU will perform. For all values of the codes of this field, except 0001, one of 15 possible microoperations is performed in the ALU. For example, for the code 0000, the microoperation $A\bar{\vee}B$ is executed, for code 0101, $A\wedge B$ 1100 is a right shift.

The five-bit field B defines the information source for the input register of the ALU. For example, for a 00001 code of this field the information source will be the output register RN of the OOP, and for the code 00010, RZ. For the code 00000 the information in the RB remains unchanged, and for the code 11010 zeroes are entered in the RB.

The three-bit field DEFORMATION defines the methods of feeding the information from the RB to the ALB. For example, for the code 001 ("Cross"), the high order tetrad is transmitted to the low-order position, and the low-order tetrad to the high-order position. For the code 011 ("high-order directly") zeroes are fed to the location of the low-order tetrad, and the high-order tetrad is transmitted without changes.

OOP Operation Control. The fields of this group control the operation of the OOP. The three-bit field "address field" defines the information source for the address register RA of the OOP. The two-bit field "mode" defines the operating mode of the OOP: 01 -- ChT (read); 10 -- ZP, RG (write, regeneration); 11 -- ST (erase); 00 -- no access to the OOP. The two-bit TYPE field defines the type of memory which will be accessed: 00 -- Z (protection module memory); 01 -- OP [core storage]; 10 -- LP; 11 -- MP.

Entering in the Flip-Flops and Registers (ZTR). The five-bit field SETUP includes the microoperations which set the registers and control flip-flops to 0 or 1, and it also executes special microoperations. The five-bit field C defines the information receiver from the RC of the ALU.

For example, for code 00010, the information receiver from the RC will be the register RZ of the OOP; for the code 10001, the register BR of the central processor.

Organization of the Address of the Next Microoperation. The fields of this group are used to form the address of the following microoperation. The nine-bit field USL defines the setting of the RAPP to 0 or 1. The two-bit field M defines the method of forming the address of the next microinstruction (the microinstruction forming procedure). The 18-bit field AMK directly forms the next microinstruction which is transmitted to the RAPP and certain other registers.

Check. The KB fields of this group contain the check bits 44, 62, 63. The bits 44 and 63 are check bits for the RMK; 62 is the check bit for the RAPP.

Reserve. Bits 59-61 are reserve bits (ZP).

Let us consider the purpose of the individual parts of the BMkU and its operating principle. The ROM is designed to store microprograms that execute the program instructions in the OOP, the manual operations, diagnostic tests, and so on. The decoders of the microinstruction fields are used for direct conversion of the corresponding parts of the microinstructions to US. In the UZAN RAPP, the address of the next microinstruction is formed, and the control of the formation is realized by the UFAMK.

The operation of the microprogram control module takes place in the following sequence. The formed address of the microinstruction is transmitted from the UZAN RAPP to the RAPP. The microinstruction selected from the ROM by this address is entered in the RMK. The fields of the microinstruction in the RMK are decoded by the DShMK decoder, at the outputs of which the set of US exciting the assemblies and modules required to execute the given microinstruction is formed. Simultaneously with decoding the microinstruction fields in the RMK, the address of the next microinstruction is formed, and the USL, M and AMK fields of the current microinstruction, ALB, and so on, participate in the formation of this address.

The microprogramming facilities, in addition to other things, the construction of the processors with a broad set of performed instructions for introduction of additional instructions requires only an increase in size of the ROM. In the processors with "hard" logic, the introduction of new instructions increases the expenditures on redoing them.

Memory Protection. In connection with the fact that the unified system of computers operates in the multiprogram mode, the OOP can have several PP [problem programs -- the programs by means of which the computer solves applied problems]. In order to avoid erroneous sending of the data of one PP to the memory zone occupied by another PP, protection is provided. For this purpose, each problem is equipped with a "pass," that is, it has its own code, and the OOP is divided into "pages" of 2048 bytes each. Each page is assigned an order number -- the protection key. The protection keys are stored in the memory key storage (ZUKP). When executing the current program in one of the registers of the central processor, the SSP and the protection key are entered corresponding to the region of the OOP

where the executed program is located. On each access to the OOP, the keys in the SSP and the ZUKP are compared. Access to the OOP is permitted only on comparison of the SSP and the memory protection key or when the SSP is equal to zero. In the YeS-1022 computer, for example, two methods of memory protection have been provided: on "read" and on "write." In order to assign the page protection method in each protection key there is an additional fifth bit in which the code 1 is entered if "read" protection is proposed or 0 if "write" protection is proposed. If the protection keys in the SSP and the ZUKP do not compare, a program interrupt signal is generated.

The sixth bit in the protection key is the check bit. The OOP protection means are implemented by a special protection module.

7.5. Characteristics of Processor ALU of Different Models of the Unified System of Computers

In order to insure program compatibility, all the models of the unified system of computers are designed to execute a united universal set of operations. Therefore the ALU of the processors of different models differ little from each other. The structural diagram of the ALU (Figure 7.7) of the processors of all models of the unified system of computers has four main parts: the registers RA and RB serving to receive and store operands and RC, for reception and storage of the operation results; the arithmetic-logic module ALB performing transformations of the operands according to the algorithms of the arithmetic, logical and other operations, for the execution of which the ALU is designed; the local control module BMU coordinating the interaction of all the ALU modules with each other and other processor units; the check system (K) providing for continuous checking of the operation of the ALU.

Flexible control of the execution of the operations is realized in the ALU of all models. The operating sequence of the ALU modules is determined by a specific operation and the peculiarities of the operands, intermediate and final results. Here, in different steps of execution of the ALB operations, an analysis of the converted information is made. The results of the analysis in the form of response attribute signals SP go to the BMU. On the basis of these signals the BMU shapes the result attribute PR which in the form of a two-bit condition code is entered in the SSP. The BMU analyzes this code and generates the next US for the ALU. After execution of the operation the ALU forms the end of operation signal SKO, on which the BMU generates the beginning of next operation signal SNO. The operands in the RA and RB registers are selected from the BR register (see Fig 7.2), where they are first entered from the OOP. The results of operations are sent from the RC to the BR, and then to the OOP (if they are not needed to execute the next operation).

The number of registers in the ALU and their word length are different in different models of the unified system of computers. The ALB of the ALU of the different models also differ with respect to composition and structure. For example, the ALB of the model YeS-1022 (Figure 7.8, a) is a universal arithmetic-logic module (ALB). A peculiarity of it is that it does not have an explicitly expressed adder. All of the arithmetic and logical operations in the ALB are executed using a set of elementary operations: binary and decimal addition and subtraction, shift by one bit right and left, bit by bit operations of logical addition, multiplication and mod2 addition and also the operations of through transmission of operands through the module.

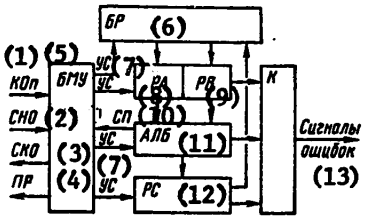

Figure 7.7. Generalized structural diagram of an ALU

Key:

1. KOp
2. SNO
3. SKO
4. PR
5. BMU
6. BR
7. US
8. RA
9. RB
10. SP
11. ALB
12. RC
13. Error signals

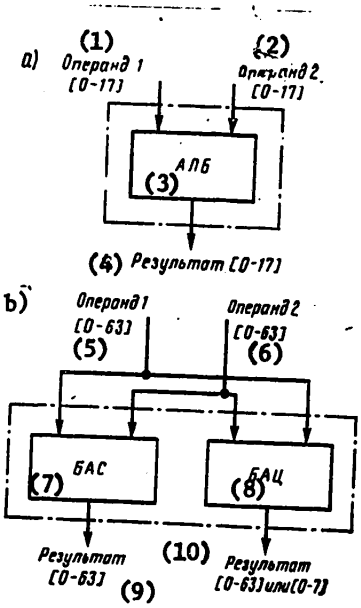

Figure 7.8. Operation parts of the processors of the unified system of computers

Key:

1. Operand 1 [0-17]
2. Operand 2 [0-17]
3. ALB
4. Result [0-17]
5. Operand 1 [0-63]
6. Operand 2 [0-63]
7. BAS
8. BATs
9. Result [0-63]
10. Result [0-63] or [0-7]

In the model YeS-1050, the ALB consists of two modules (Figure 7.8, b); the BAS is the arithmetic adder module, and the BATs is the digital decimal arithmetic module with explicitly expressed adders. In the BAS, arithmetic and logical operations are performed on the fixed-length operands. The basis for it is the 64-bit binary parallel-action adder. In the BATs, only the byte by byte processing of the operands is carried out. The basis for it is the 8-bit decimal adder and logical commutator (the latter is designed for execution of logical operations). The registers RA, RB and RC are 64-bit registers. The result of the operations can be output byte by byte from the RC or all 64 bits simultaneously.

The differences in composition and operation principle of the ALU were the result of different requirements on the output capacity of the models of the integrated system of computers and the desired volume of their equipment imposed by the developer during their design. Characteristic features of the decisions made gave rise to different structural principles of the ALU and different algorithms for executing individual operations.

7.6. Performance of Arithmetic Operations on Fixed-Point Binary Numbers

Addition and Subtraction. When performing these operations, the operands with respect to addresses indicated in the instruction are caused from the OOP and are transmitted to the registers RA and RB. In the OOP, the fixed-point binary numbers are represented in two formats: in the form of a 32-bit word or 16-bit halfword. The operations are performed on numbers which are smoothed with respect to the high-order bits. In positive numbers the missing bits are filled with zeroes to the halfword or word, and for negative numbers, ones. For example, a positive number +11001101 in the halfword format has the form 0.0000000 11001101, and the negative number -101 101 101 is written 1.111 111 101 101 101. In the different models of the unified system of computers, the operand codes are sent differently for addition and subtraction. For example, in the YeS-1022 computer the operands are made up of halfwords, and in the YeS-1030 and YeS-1050 which have 32 and 64-bit adders, respectively, they are made up of words and double words. When executing the subtraction operation in the unified system of computers, a complementary code is used. In order to obtain the complementary code, the subtrahend of the second operand going to the ALU, bit by bit (including the sign bit) inversion takes place with subsequent addition of one to the low-order bit. On completion of the summation process the BMU analyzes the result (equal to, less than or greater than 0 result and whether an overflow has occurred). By the result of the analysis, the result tag (PR) is generated which is a two-bit binary code. If the result of the operation is zero, then the code 00 is generated; if it is less than 0, the code 01; if greater than 0, the code 10; if overflow has occurred, the code 11.

Accelerated multiplication circuits are used to reduce the multiplication time in the computers of the unified system. For example, in the YeS-1030 model, multiplication takes place by two bits of the multiplier simultaneously, and in the YeS-1050, by four bits simultaneously.

In the unified system of computers, the divisor, remainder and quotient with the sign have 32-bit formats.

7.8. Monitoring and Control Panel

The monitoring and control panel PKU is designed to monitor the operation of the computer units, manual control and operative intervention in the operation of the computer. The PKU of any of the unified system of computers (Figure 7.11) contains a control panel PU, a display planel PI and electronic circuits -- control circuits and registers -- by means of which the panel operations are performed.

The control board has: "operating mode," "check," "address comparison," "type of memory" switches designed to assign the operating mode of the computer and the panel operations; the control buttons with light (the display buttons) "power on," "power off," "clear," "memory address" and others designed for panel operations. In addition, the control panel has the display lights "system state" (LOADING, WAITING, CHECK, MANUAL OPERATION, SYSTEM).

The display panel has lights to indicate the contents of certain registers of the computer and the state of individual control flip-flops.

Processor Start-Stop. The processor is switched on and off by the "power on," "power off" buttons, respectively. After pressing the "start" button, the processor performs operations in the mode selected by the "operating mode" switch (AUTOMATIC, INSTRUCTION, MICROINSTRUCTION positions). The transition of the processor to the "halt" state is realized either by the operator (by pressing on the "halt" button) or automatically. An automatic halt of the processor takes place when the execution of the current instruction has been completed and there are no interrupt requests or when an error is detected in the processor and the execution of the current instruction or service microprogram is impossible.

Processor Operation Check. The operating mode of the check circuits is given by the "check" switch (AUTOMATIC, HALT, BLOCKING positions). If the "check" switch is set to the AUTOMATIC position, then when an error occurs the processor processes it, finds and eliminates the cause of its occurrence. In the HALT position, machine errors are not processed, the generator GSI is switched off, the error is recorded in the error register RO, and the computer halts. If the "check" switch is set to the BLOCKING position, the processor continues to operate without reacting to the error. The clearing of an error is produced in all cases by the "clear error" button. In this case the RO is initialized and further operation of the processor can be continued.

Checking the Operation of Memory Cells. The "type of memory" switch (OP, MP, LP, process registers, registers KS0, KS1, KS2) selects the type of memory which is accessed from the PU. When assigning the memory address by the "memory address" buttons (gives the OOP cell address, the processor register or input-output channel address) and the "instruction address" (gives the address of the current instruction, the ROM address, the address of the peripheral device on input of the initial program), the contents of the checked memory cell light up on the display panel. The contents of the memory cell and the processor registers are changed by the address selected by the "memory address" buttons by pressing on the "write" button. The entered information is in this case given by the buttons "instruction address."

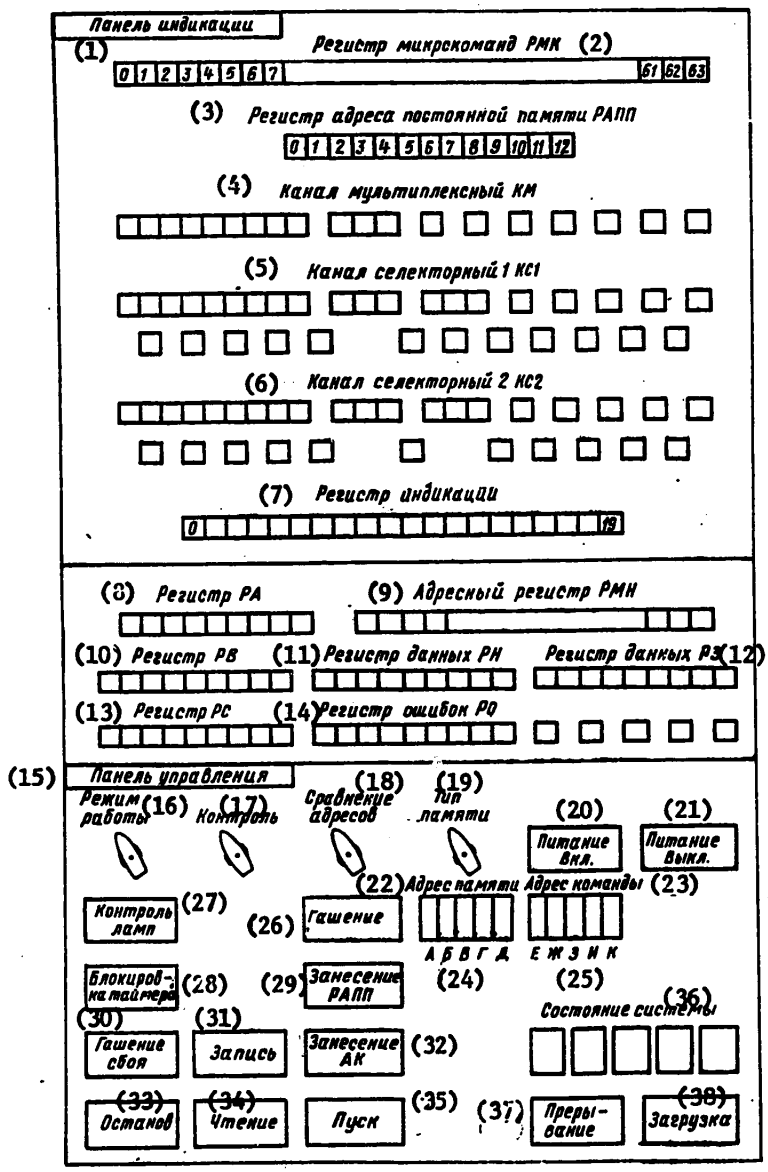

Figure 7.11. Computer monitoring and control panel

Key:

1 -- Display panel; 2 -- microinstruction register RMK; 3 -- read-only memory address register RAPP; 4 -- multiplex channel KM; 5 -- selector channel 1 KS1; 6 -- selector channel 2 KS2; 7 -- display register; 8 -- register RA; 9 -- address register of the RMN; 10 -- register RB; 11 -- RN data register; 12 -- RZ data register; 13 -- register RC; 14 -- error register RO; 15 -- control panel; 16 -- operating mode; 17 -- check; 18 -- address comparison; 19 -- type of memory; [continued]

[Key to Fig 7.11, continued]

20 -- power on; 21 -- power off; 22 -- memory address; 23 -- instruction address; 24 -- A B C D E; 25 -- F G H I J; 26 -- clear; 27 -- light check; 28 -- timer blocking; 29 -- entering in the RAPP; 30 -- error clear; 31 -- write; 32 -- entering the AK; 33 --halt; 34 -- read; 35 -- start; 36 -- system state; 37 -- interrupt; 38 -- loading

Initial Loading of the Program and Clearing of the System. The system is cleared by pressing the "clear" button. Here the master clock "GSI is shut off and the hardware clear signal is generated. This signal clears all the processor registers and nullifies all of the interrupt requests.

The "load" button is used for initial loading of the program (PZP). In order to perform this operation, the Z, I, and K instruction address buttons are used to set the channel number and the number of the peripheral device from the program must be loaded. All of the control switches except the "type of memory" switch are set to the AUTOMATIC position. After pressing on the "load" button, the system is cleared, and the PZP microprogram is executed, as a result of which the loader program realizing further program input in the automatic mode is read into the OOP from the peripheral device indicated on the control panel.

The indicated properties of the panel are sufficient to input the program and the initial data to the computer, force its operation in the automatic or single-mode, start the computer with any instruction in the OOP, print out codes from any of the OOP cells, operate the computer by loops and cycles when the computer must be checked out.

Before proceeding with the solving of a large problem, a preventive check is run on the modules and elements of the computer by a special test program. The test problems are selected so that on solution of them all elements of the computer will be encompassed. When solving the test problem it is possible to set feed voltages that are $\pm$(10-15%) different from the rated voltages from the panel. If under these conditions the computer continues to operate stably, it is certain that it is operating reliably.

Special "measurement from channel" lines (IZM-K), "measurement from subscriber" (IZM-A) and "state shift" (SMS-K) lines are used to control the time measurements and shift and states of the UVU.

The interface lines are made of high-frequency cable type IKM-2 with wave impedance of 82 to 110 ohms. The cable length from the MSK to the most remote UVU does not exceed 100 meters for the VBR-K and VBR-A lines and 65 meters for all the rest. All the lines were composed of two strands for the connection of which to the MSK or the UVU, rectangular combined 40-contact plugs of the "plug board" type are used.

The input-output interface of the unified system of computers provides for transition of information at a maximum speed of 1.3 megabytes/sec. New developments of the VU have required improvement of the interface characteristics. In the improved input-output interface, the carrying capacity has been increased by multiplexing the information in the buses and enlarging the information buses.

The possibility of repeating the output of an instruction by the channel in case of random error detection or temporary unreadiness of the UVU to execute the instruction and also selective clearing when necessary have been provided.

CHAPTER 9. GENERAL INFORMATION ABOUT INFORMATION STORAGE

The basic characteristics of magnetic recording when it is used to store information are the following: high recording density (60-80 bits/mm); unlimited information storage time without consuming electric power, comparatively high information write and read speed; the possibility of erasing previously written information and recording new information.

All of the existing storages can be divided into two groups with respect to information output and reception speed: fast and slow. The storage elements of the first group have a speed of (1 to 5)$\times 10^6$ bits/sec and access time of 10 to 20 milliseconds. They are executed on magnetic drums and discs. The slow ones have a speed of (1 to 5)$\times 10^5$ bits/sec and an access time from units of seconds to several minutes. They are executed on magnetic tapes and cards. As a rule, the amount of information required for large computers is so great that the VZU is made up of several fast storages and several tens of storages of the same group. During the operating process of the computer, in order to reduce the access time to the VZU, all of the information from the second group storage elements goes to a processor through the first group storage element.

The information written on a magnetic surface usually is not used directly in the computer process, but it is first transmitted to the OOP and only then goes to the ALU for processing. As a result of large volume of information which can be stored in a memory with magnetic recording they are called storage elements.

Magnetic Information Carriers. In modern computers broad use is made of magnetic tape, drum, disc and card storages. Powder and galvanic magnetic coatings applied to a nonmagnetic base are used as the storage medium in these devices.

Magnetic tapes and magnetic cards have, as a rule, powder magnetic coatings. As a nonmagnetic base for them, broad use is made of lavsan (polyethyleneterephthalate) 25 to 35 microns thick or acetylcellulose (triacetate) 50 to 120 microns thick. The magnetic coating -- ferrolac 2-20 microns thick -- is applied to the moving base. The ferrolac consists of fine powdered iron oxide Fe_2O_3 and nonmagnetic binder -- lacquer. The powder particles can be cubic (or spherical) and acicular in shape. Individual powder particles have dimensions on the order of 0.1 to 1.5 microns.

The magnetic coating must be distinguished by small surface roughness, uniformity of the magnetic parameters and high wear resistance. The values of the magnetic parameters of the coating, depending on the type of powder, are within the limits of H_c=1200 to 24000 amps/meter, B_r=0.08 to 0.15 tesla. The coercive force H_c is selected sufficiently large to exclude the possibility of erasing information as a result of the external magnetic fields.

Magnetic drums and discs are covered with ferrolac or metallic coatings based on nickel, cobalt and tungsten. The thickness of the metal coatings is 2 to 10 microns. They are applied galvanically. The advantage of the metal coatings is large wear resistance and the possibility of obtaining thin magnetic layers. The most frequently used metal coatings have the following magnetic parameters: nickel-cobalt H_c=16000 to 20000 amps/meter, B_r=0.4 to 0.6 tesla; cobalt-tungsten H_c=28000 to 40000 amps/meter; B_r=0.3 to 0.5 tesla; cobalt-nickel-phosphorus, H_c=55000 to 65000 amps/meter; B_r=0.3 to 0.5 tesla.

The drum is a carefully machined cylinder of brass, stainless steel or aluminum alloys. In order to decrease the mass, the discs are made of aluminum alloys. The magnetic coating is applied to a copper sublayer.

Magnetic Head. Writing of the information on the magnetic carrier 4 (Figure 9.1) and reading are carried out by the magnetic head MG. It is a miniature electromagnet. In order to reduce the losses from the eddy currents, the core 1 is assembled from thin (0.02 to 0.15 mm) cold-rolled plates of iron-nickel alloys having small coercive force H_c (1 to 4 amps/meter) and residual induction B_r, high saturation induction B_m (1-1.6 tesla) and initial magnetic permeability μ_{init} ($1 \cdot 10^4$ to $3 \cdot 10^4$). The core 1 has two gaps: working 3 and additional process 2. The modern magnetic heads have a working gap of up to 2 to 30 microns. The working gap is filled with nonmagnetic material, for which, for example, beryllium foil is used. The windings are included opposite to each other and have a common grounded point. As a result, there is no necessity for changing the direction of the current when writing a "zero" and "one." In order to increase the service life, the working surface of the head is carefully polished, and sometimes it is coated with a layer of rhodium or palladium.

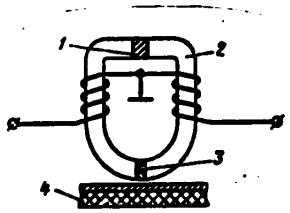

Figure 9.1. Magnetic head

At the present time the following NML [magnetic tape storages] are in operation: YeS-5003, YeS-5010, YeS-5014, YeS-5017, YeS-5021, YeS-5025 built in the USSR; YeS-5001, YeS-5019 built in Poland; YeS-5004, YeS-5015, YeS-5022 built in Czechoslovakia; YeS-5012 built in Bulgaria; and YeS-5016 built in the German Democratic Republic. The YeS-5017 storage is the base storage and corresponds to the All-Union State Standards and recommendations of the ISO (International Standards Organization).

A standard magnetic tape 12.7 mm wide, 750 meters long and 48 microns thick wound on a standard holder with external diameter 267 mm is used in all of the storage elements. The information is recorded during forward motion of the tape simultaneously on 9 tracks with densities of 63, 32 and 8 bits/mm (8 tracks are designed to record data and 1 is a check track), and read is in both forward and reverse. The magnetic heads have contact with the tape only in reading and writing information, and during rewind they are automatically retracted.

Two write methods are used in the storage elements of the unified system of computers: with respect to two levels with inversion by "1" (BVN-1) and with respect to two levels with phase modulation (FK-write). The YeS-5014, YeS-5015 and YeS-5025 units which make use of the FK-write produce a recording density of 32 and 63 bits/mm. In the remaining storage elements, except the YeS-5004, the BVN-1 write method is used. Data recording and reading are realized with densities of 8 and 32 bits/mm. In the YeS-5004, the BVN-1 and FK-write methods are used which insure a recording density of 8, 32 and 63 bits/mm. In the YeS-5016 and YeS-5021 units, the data is recorded only with a density of 32 bits/mm, but in them provision is made for the possibility of reading information having a recording density of 8 bits/mm.

The capacity of each magnetic tape storage, except the YeS-5004 and YeS-5025, is 25 megabytes. The capacity of the storage elements YeS-5004 and YeS-5025 is 50 megabytes. The data transmission speed for the various storage elements is different and fluctuates within the limits from 48 kbytes/sec (for example, for the YeS-5016) to 315 kbytes/sec (YeS-5003). The working speed of displacement of the magnetic tape of the storage elements YeS-5012 and YeS-5017 is 2 m/sec; YeS-5019 is 3 m/sec; YeS-5022 is 4 m/sec. The rewind speed of the tape is 5 m/sec for the majority of units.

In all of the storages, good ventilation of all of the units is insured, excess pressure is created which prevents penetration of dust into the work zone. For compatibility of the various types of NML, a number of structural and production requirements have been imposed -- the sizes of the magnetic tapes and the reels for them, methods of writing and locating information, recording density and methods of checking the data have been standardized. An international standard for the above-enumerated and other characteristics has been developed in connection with the important significance of compatibility of tapes.

10.2. Arrangement of Information on Magnetic Tape

Each module has 140 bytes, 44 bytes of which are in the key field, and 96 bytes, in the data field.

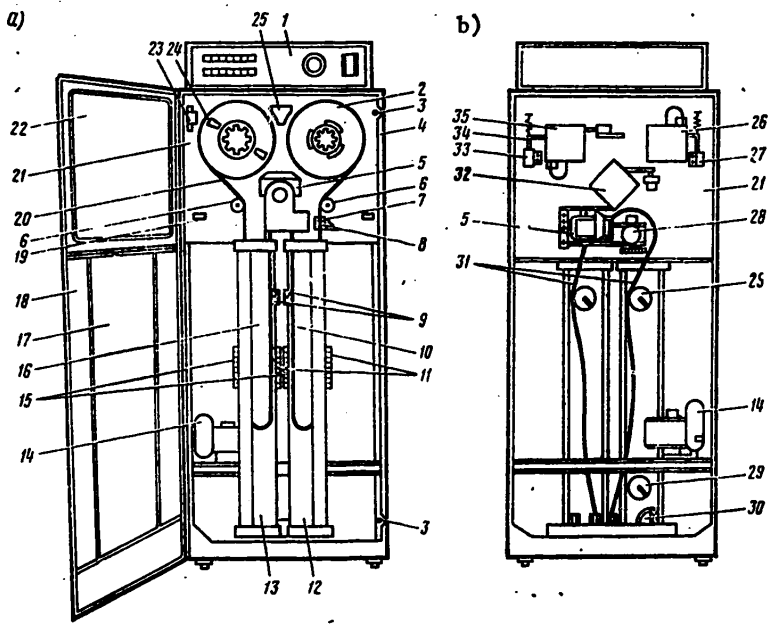

Figure 10.5. Magnetic tape storage:
a -- front view; b -- back view (without door); 1 -- control console; 2 -- feed reel; 3 -- bolts for fastening the rpm plate; 4 -- frame; 5 -- magnetic head module; 6 -- magnetic tape sensor; 7 -- tine for pressing the magnetic tape; 8 -- limiter; 9 -- vacuum column lock; 10 -- magnetic tape loop; 11 --photo pickups of the reel motor servosystem; 12 and 13 -- vacuum columns, right and left, respectively; 14 -- vacuum pump; 15 -- tubes for lighting the photo pickups of the reel motor servosystem; 16 -- column screen; 17 -- lower inspection hole; 18 -- front door; 19 -- blocking circuit; 20 -- magnetic tape; 21 -- mounting plate; 22 -- upper inspection hole; 23 -- photo sensor for diminished amount of tape; 24 -- take-up reel; 25 -- focusing system; 26 and 35 -- drive mechanisms, take-up and feed reels, respectively; 27 and 33 -- brake electromagnet; 28 -- mechanism for positioning the magnetic head module on or off the tape; 29 -- sensors for limiting the magnetic tape loop; 30 -- pneumatic sensor; 31 -- vacuum tubes; 32 -- magnetic tape drive mechanism; 34 -- brake shoe.

In order to insure the required vacuum in the columns there is a vacuum pump 14 which guarantees a pressure in them of 3.64 to 4.0 kPa. The vacuum in the columns is checked by the pneumatic sensor 30 which blocks switching the storage on at a pressure of 2.45 to 2.94 kPa and switches it off if a pressure of 1.47 to 2.06 kPa is recorded during operation. As a result of the pressure difference, the tape is pulled into the columns, forming a loop of defined dimensions. During the transient processes connected, for example, with starting and stopping the magnetic tape, the buffer and reel drive controlled by a photocurrent from the photo pickup prevent inadmissible increase or decrease in tape tension. The vacuum tubes 31 form part of the system for cleaning dust off the magnetic tape. The exhaust air from the vacuum pump is used to cool the drive motor.

In the YeS-5017, the MGS [magnetic erase head] operates on direct current of about 970 milliamps.

The material used to fill the working gap of the magnetic head must have a number of special properties, for the width of the gap frequently is only equal to a few fractions of a micron. Gaps 5 to 10 microns wide usually are filled with metal in the form of beryllium bronze or platinum foil. In order to obtain small gaps, silicon oxide is used, the filling of the gap with which is realized by spraying.

The BMG [magnetic head module] must be located strictly perpendicular to the moving tape. If the perpendicularity is violated, the signals read by different heads will be output at different time (misaligned). This can occur also when recording information. If the direction of the misalignment during recording and reading is different, then the mismatch will be doubled in time. The phenomenon of misalignment is impossible to eliminate completely by mechanical methods; therefore special electronic circuits that compensate for it are used in the NML.

BMG Lift Mechanism. The mechanism (Figure 10.10) is used for angular displacement of the BMG from the operating position to the nonoperating position: A=7°, B=42° and back by control instructions from the storage or manually. There are two cases when the BMG is withdrawn from the operating position: on performance of the REWIND operation, by 7°, and when performing the UNLOADED operation, by 42°.

Operating Principle of the Electric Drive Motor Control System. The electric drive motor control system provides for movement of magnetic tape with constant working speed forward and in reverse and accelerated rewind (on the feed reel) at a speed of 5 m/sec for the YeS-5014, YeS-5017, YeS-5019, YeS-5025 and 8.5 m/sec for the YeS-5015 and YeS-5022.

When the magnetic tape is moved at working speed, the DS pickup generates a signal with 50 millivolt amplitude and frequency of about 2 kilohertz. In the case of accelerated rewind of the tape the DS generates a signal with high amplitude and a frequency of about 5.5 kilohertz. This signal goes to the UFI where it is amplified and shaped into square pulses with steep front and cut, and it is differentiated. The differentiated pulses have a duration of 1 microsecond and frequency proportional to the shaft rpm of the electric motor. If the speed of the tape is equal to the rated speed, then the pulse repetition period is equal to 512 microseconds, and a defined number of pulses recording this speed are entered in the registers R. With a decrease or increase in the speed, a

different number of pulses is entered in the registers R of the UFI, and this number of pulses is compared with the standard. Depending on the difference obtained, a PWM [pulse-width modulated] signal is generated with defined duty factor -- for pulses with the largest repetition period, the PWM signal with maximum duty factor is generated, and for pulses with small repetition period, with minimal. The duty factor of the PWM signal is determined by the shaft rpm of the electric motor M. The PWM signal from the registers R goes to the control logic module BLU, which acts on the electric motor through a powerful amplifier UUVD.

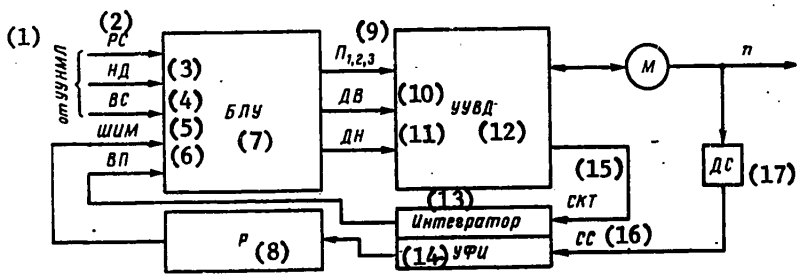

Figure 10.12. Drive electric motor control system

Key:

1. from the UUNML
2. RS
3. ND
4. VS
5. PWM
6. VP
7. BLU
8. R
9. $П_{1,2,3}$
10. DV
11. DN
12. UUVD
13. Integrator
14. UFI
15. SKT
16. SS
17. DS

Start, Movement of Magnetic Tape with Rated Speed and Halt. When starting the tape from the UU, RS (operating speed) and ND (direction of movement) signals are fed to the BLU. On the basis of these signals the BLU generates the signal DV (movement forward) or DN (move backward). In this case the total feed voltage is fed from the UUVD to the electric drive motor M in order to reach the required magnetic tape speed as fast as possible. When the electric motor has reached 90% of the rated speed, on instruction from the BLU, the UUVD organizes the pause $П_1$, that is, stops the feed voltage for a time of 0.12 milliseconds. The current through the electric motor during this pause decreases, and the electric motor picks up rated speed, upon which the PWM signal with defined frequency filling is fed to the BLU from the registers R.

If it is necessary to stop the magnetic tape, then the UU NML picks up the signal RS and the BLU issues the pause $П_2$ lasting about 0.5 milliseconds. The thyristors of the controlled rectifier (see Figure 10.11) opened before the pause $П_2$ are restored, after which the total feed voltage of opposite polarity is fed to the motor (through the corresponding pair of thyristors). When the electric motor reaches 10% of the rated speed the BLU generates the pause

Π_3 lasting about 0.9 milliseconds, during which the thyristors are restored, insuring a countercurrent. The instruction to generate the required pause is the VP signal (generate pause), which is formed as follows. The UUVD checks the shaft rpm of the electric motor M by the current flowing through it and constantly feeds the current check signal SKT to the integrator. When the electric motor M reaches a speed that is 10 or 90% of the rated speed the integrator generates the VP signal.

Start, Movement of the Magnetic Tape at High Speed and Halt. If the signal VS (high speed) reaches the BLU simultaneously with the signal RS, the tape acquires the requirement speed in 0.5 second in the YeS-5012 and 5 milliseconds in the YeS-5017 as a result of feeding the total feed voltage to the electric motor. After this, it is controlled by the corresponding PWM signal for this speed. If the signal VS is now picked up, then the electric motor rpm decreases independently to 2 m/sec in the time 0.5 second (or 5 milliseconds for the YeS-5017) without supplying additional power. When picking up the signal RS, the electric motor is stopped by the countercurrent. An automatic halt of the magnetic tape is realized in the following cases: in the automatic control mode on detection of the "beginning of tape" marker, in the autonomous control mode on detection of the markers of the beginning and end of tape; independently of the operating conditions of the storage, when the tape loop from the vacuum columns goes beyond the upper or lower emergency photo pickups, the tape breaks, the vacuum disappears in the vacuum columns, any of the phases of the primary network voltage drops, any of the feed potentials increases or decreases.

10.7. Electric Circuitry of the Tape Storage

The electric circuitry includes the following: the electronics module, the automation module, the power pack, the control console and the external connections panel (see Section 10.3). They are assembled from standard elements (see Chapter 3) and special-purpose elements. Let us consider the structure and the operating principle of some of the special elements and assemblies.

Reproduction Amplifier UV. The reproduction amplifier is designed for preliminary amplification of signals picked up from the MGV, the shape of which is close to sinusoidal. Basic characteristics of the amplifier: input signal amplitude from -15 to -20 millivolts; output signal sinusoidal, amplitude to -5 volts; amplifier gain about 100; frequency range 0.2 to 100 kilohertz; frequency distortions in the operating range no more than 3 dedibels. Nine identical UV are mounted in the TEZ. The basic UV is the operation amplifier U0.

Shaper Amplifier UF. Signals from the reproduction amplifier go to the UF, they are rectified and amplified by it.

The characteristics of the UF are as follows: input signal about 2.5 volts amplitude, sinusoidal shape with repetition period of 30 microseconds; output signal: high level +5 volts, low level 0 to 0.4 volts, repetition period 60 microseconds, leading and trailing edge durations no more than 0.15 microseconds.

Three functionally independent UF are mounted in the TEZ. Each of them (Fig 10.14) contains: differential amplifier executed from transistors T1 and T2, two-period rectifier based on diodes D1 and D2 and shaper based on transistors T3-T6.

In order to increase the noise immunity and reduce the distortions introduced by the shaper to a minimum, the first stage is assembled as a differential circuit.

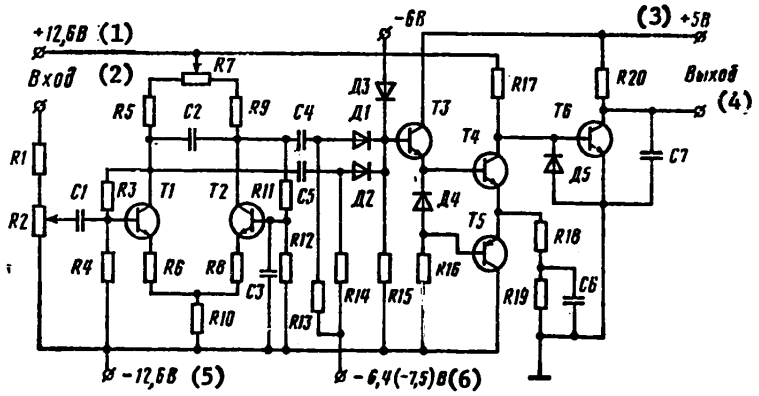

Figure 10.14. Shaper-amplifier

Key:
1. +12.6 volts
2. input
3. + 5 volts
4. output
5. -12.6 volts
6. -6.4 (-7.5) volts

10.8. Characteristic Failures of Magnetic Tape Storages, Their Detection and Elimination

The violation of normal operating conditions of the NML or failure of any assembly of it is signalled by the SK channel using the "sense state" instruction. The nature of the error is displayed on the display panel of the tape unit or the computer.

The storage is usually initially checked out in the autonomous mode, performing all manipulations proposed by the operating instructions. By the results of this test and on the basis of the operating logic of the storage, the cause and location of the error or failure are established.

Further search for a failure is made using the monitoring and measuring equipment which is available in the computer units. In particular, for the NML the following are used: the MKN -- a device for checking out storages, by means of

which it is possible to check the basic parameters of the NML; PKTE — a device for checking out standard elements for testing and adjusting their operating conditions; type S1-18 electronic oscillograph used to check electric parameters; ChZ-9 type digital frequency meter for measuring frequency and calculating errors, zones, rows; combined devices AVO-5M, Ts56 or Ts34, and so on for checking voltages and determining the magnitudes of the resistances; dc bridge with precision class no less than 0.5 to measure small resistances; stop watch, set of probes and long strands. The parameters are measured, the elements, assemblies and systems adjusted and tuned in accordance with the operating instructions and tables attached to them.

It is possible to estimate the fitness of the storage after eliminating a failure only after the storage has executed a special test program correctly.

The simplest, most frequently encountered failures can be determined without using special means of finding them. Let us consider some of these failures.

Power Not On. The cause of this can be absence of voltage in one of the phases of the primary feed network, an unreliable electrical contact in one of the plugs, burning out of the fuse in the power control unit (BUP) or in one of the power modules (BP).

The presence of phase voltages is checked by an ammeter-voltmeter. A burned-out fuse in the BUP can be caused by violation of normal operation of the power pack protection circuit; therefore it must be carefully checked. By a continuity test on the power on circuit, an unreliable contact is discovered in the plug or reliability is certified.

The storage does not react to the emergency position of the tape loop in the vacuum columns. This failure can be caused by failure of the photodiodes or having the vacuum sensor out of adjustment.

The magnetic tape loop goes outside the vacuum column or drops to its bottom. In this case it is necessary to check for a failure of the lighting tubes and the reliability of the circuit for switching on the electric reel motors.

In reverse the magnetic tape loop goes outside the working zone. This can be caused by failure of one or several photodiodes in the photo pickup that monitors the magnetic tape loop in the vacuum column or poor adjustment of the braking electromagnet of the reel.

The pressure in the vacuum system is below the required pressure. It is necessary to check the contact points of the air lines in the pressure branch of the system and vacuum pump.

The amount of rarefaction in the vacuum columns, pressure in the pneumatic system are below the required levels. The probable cause of this failure is weakening of the tension in the drive belt of the vacuum pump.

The "load" indicator is not on. It is necessary to check the bulb and the photodiode in the "beginning of tape" sensor.

If we analyze the investigated failures, it is possible to arrive at the conclusion of the possibility of preventing them by correct and timely preventive maintenance of the storage element. Fail-safe operation of the NML is determined primarily by skillful operation and good technical maintenance.

10.9. Preventive Control Operations

General Principles. Preventive control operations are intended to insure uninterrupted operation of the storage. They provide for periodic checking of the parameters of the elements and assemblies and maintenance of cleanness of the entire storage. The periodicity of the preventive monitoring operations for the storage is established considering the reliability of its mechanical assemblies and electronic circuits. All types of operations are performed strictly by the instructions for technical maintenance of the storage.

After every 4 hours of operation of the storage, the surfaces of the elements of the tape drive channel in contact with the magnetic tape are cleaned with a soft cotton cloth wet in alcohol. The working surface of the BMG is wiped with a chamois, and the surface of the drive roller and surface of the inspection holes, with a dry cotton cloth.

Once a day the same operations are performed as after every 4 hours of operation of the storage element. The entire storage is inspected externally and the attachment of the feed reel is checked also.

Once a week all of the above-enumerated operations are performed. In addition, the perpendicularity of the magnetic head module with respect to the magnetic tape is checked, and if necessary, adjusted. When adjusting the BMG it is necessary to be very careful to see that the operating surface is not scratched.

Once a month all the operations performed after 4 hours, diurnally and weekly are performed. In addition, the following operations are performed: cleaning of the fan air filter, adjustment of the magnetic heads with respect to azimuth, monitoring the level of the read signals and voltages in the circuits controlling the limitation level in the reproduction channel, checking the "SKYu" compensation during information read and write. The fan air filter is cleaned by mechanical vibration or a vacuum cleaner. All of the remaining parts are made strictly by the instructions.

Once or twice a month, in addition to the above-enumerated operations, the following are performed: the vacuum in the vacuum columns is checked and the operation of the pneumatic sensor is checked; the drive and reel electric motors are checked and cleaned; the pump power supplies, automation module, start and stop time of the magnetic tape and its speed are checked and adjusted, and the functioning of the photo pickups for short tape, beginning and end of magnetic tape is checked out.

Once every 6 months, in addition to all of the above-enumerated operations, the BMG and fans are lubricated, the write current buildup and quality of erasing information off the magnetic tape are checked.

Once a year all forms of operations performed after 4 hours, annually, weekly, once every 2 months and every 6 months are performed. In addition, all of the electric motors of the storage, the reduction gears and coil springs are cleaned and lubricated, the travel of the armatures of the brake electromagnets and the friction of the brake shoes are checked. The volume and periodicity of the preventive control operations will change in one direction or another depending on the load on the storage, the ambient conditions, and so on. Materials used when performing preventive work are as follows: distilled alcohol, benzine solvent, clock oil, US graphite lubricant, TsIATIM lubricant 201 or 221, turbine oil, cotton gauze, soft cotton cloth, technical chamois, fine emery paper No 400 and 600.

Procedure for Performing Certain Monitoring and Preventive Operations. The monitoring and cleaning of the drive and reel electric motors are carried out after 500 to 700 hours of operation of the storage. Here the degrees of wear, deformation and pollution of the collector brushes and contact surface, loosening of bolts, clamps and so on are determined. During operation the electric motors are checked for the presence of noncharacteristic knocks and noise and sparking of the contact brushes. On detection of inadmissible wear in the contact brushes, they are replaced by new ones. The new brushes must be fitted to the collector. For this purpose, a strip of emery paper 2 No 400 (Figure 10.17) is placed between the collector 3 and the contact brush 1. The width of this paper must be equal to the width of the contact surface of the collector. The emery paper is placed so that the abrasive side will be toward the contact brush. The brush is fitted by drawing the emery paper back and forth until the brush assumes the shape of the collector. After fitting, the collector is cleaned with a dry soft rag, it is blown with air under pressure or the dust is removed by a vacuum cleaner.

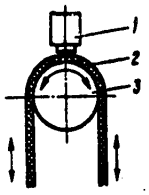

Figure 10.17. Fitting of collector brushes

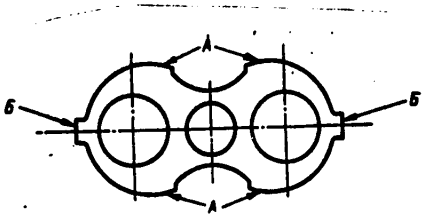

Figure 10.18. Vacuum pump impeller

The contact surface of the collector is cleaned with emery paper No 600, for which it is applied with the abrasive side to the contact surface of the collector, the shaft of the electric motor is clamped and turned manually. After cleaning, the surface of the copper bars of the collector must be clean and have metallic shine. On completion of grinding, the collector surface is cleaned of dust using a vacuum cleaner or it is blown with air.

When performing all of the operations it is necessary to remember that there is a powerful magnetic field in the electric motor. Therefore small metallic objects such as screws, springs, seals, and so on must not be placed close to it.

The friction of the brake shoes is checked with the electromagnetic brakes off, using a filled test reel and dynamometer.

After every 1000 hours of operation of the storage, preventive control operations are performed with a vacuum pump. First the belt tension and the alignment of the drive and driven pulleys are checked. When pushing on the belt with a force of 20 N, it should deflect 12±1 mm, and the misalignment of the pulleys relative to each other should be no more than 0.2 mm. Then the pump is switched on for 10 or 15 minutes and its heat is checked by feeling it. Strong local heating of the bearing covers to the point that one cannot hold one's hand on the cover (above 70°C) can occur as a result of absence of axial clearance or in the case of poor lubrication of the bearings. Strong heating of the housing and the presence of a dull metallic sound are the sign of the impellers hitting together.

When the pump is taken off it is first deenergized, then the belt is removed, the vacuum tubes are removed, and the bolts unscrewed that fasten it to the plate. The removed pump is inspected and checked for oil leaks and chips in the housing. The manual rotation of the pulley rotors must be smooth, without seizure or jerking, the cause of which can be increased play or wear of the bearings. The impeller surfaces are examined through openings in the pump housing. A characteristic metallic shine on the surfaces A (Figure 10.18) of the impeller indicates that the impellers are making contact when they turn, and scratches on the surfaces B indicate that the impellers are catching on the housing. A noncharacteristic metallic bumping heard against the general background when the pump is in operation, jerking when the impellers are turned without load and circular scratches on the inside surfaces of the housing all can be a sign of bearing wear. If the enumerated or other defects are detected when the pump is inspected, the pump must be dismantled, the worn parts replaced and the pump must be reassembled and adjusted. All the operations are performed in strict accordance with the technical maintenance instructions. If there are no defects, then we proceed with lubricating the pump, for which the pulley and bearing covers are removed together with the blocks of shims and the cover of the case. The old oil is drained out and all of the assemblies are washed in benzine solvent, and then they are carefully dried with a rag. The presence of lint and traces of dirt on the parts is not permitted.

After cleaning, all of the assemblies are carefully inspected and, if there are no defects in the pump assemblies, ease of running of the impellers when they are turned by hand is checked with the bearing covers removed and then with them installed. If the impellers are hard to turn when the covers are installed, then shims are added under the covers. The pump is lubricated in accordance with the instructions.

CHAPTER 11. MAGNETIC TAPE STORAGE CONTROLLER

11.1. Purpose and Technical Specifications

The magnetic tape storage controller (UU NML) is designed for connecting the magnetic tape storage to the input-output channels of the unified system of computers and also to control the operation of the storages. It provides for matched operation of high-speed circuits of the SK and MK channels with the slow storages. The UU NML is connected to the SK and MK channels through the input-output interface, and it operates only in the exclusive mode.

The UU NML provides for the following: selection of the given storage, reception and execution of central processor and channel commands, information transmission between the NML and the channel; checking the reliability of the information transmitted through the UU, control of the movement of the magnetic tape in the storage; shaping of the time delays required for proper execution of the information recording and reproduction; generation of information describing the state of the storages in detail; control of completion of a series of operations (rewinding the tape, unloading, and so on) without channel participation.

One UU provides for successive execution of all of the commands with each of the eight storages connected to it. The commands executed by the UU NML are divided into three groups: basic, auxiliary and control and mode setting commands.

The basic NML commands include the following: READ, REVERSE READ, WRITE, CHECK INPUT-OUTPUT, SENSE. On the READ command the magnetic tape in the selected storage moves forward to the required interzonal interval and halts. The information recorded on the tape is read and transmitted to the channel. The REVERSE READ command is executed just as the READ command, but the tape runs in the opposite direction. On execution of this command, the successively read bytes are arranged in the OOP in order of decreasing addresses. On the command WRITE, the data coming from the channel are written on a tape moving in the forward direction. This operation is completed by channel initiative. The commands CHECK INPUT-OUTPUT and SENSE are used to transmit information about the state of the unit to the OOP.

The control commands are used to move the magnetic tape to the required position. These include: REWIND, REWIND AND UNLOAD, FORWARD TO BLOCK, BACKWARD TO BLOCK, FORWARD TO FILE, BACKWARD TO FILE, ERASE INTERVAL, WRITE MARK. On the REWIND command the tape in the selected storage element is rewound to the "beginning of tape" marker, and on the REWIND AND UNLOAD command the tape is fully wound on the feed reel. On the command FORWARD TO BLOCK the tape is rewound in the forward

direction to the next interzonal interval, and on the command BACKWARD TO BLOCK, in the opposite direction to the next interzonal interval or to the "beginning of tape" marker.

The mode setting and auxiliary commands include the commands CORRECTION, DIAGNOSTICS, SET DENSITY (8, 32 or 63 bits/mm).

On execution of all commands except the REWIND, REWIND AND UNLOAD, the UU is occupied with execution of the operations for the entire time. On executing the REWIND, REWIND AND UNLOAD commands, the control unit is busy only to the beginning of movement of the tape in the storage. After beginning of movement, the UU is released and can perform any operation on another free storage.

At this time the UU NML YeS-5511, YeS-5512, YeS-5515, YeS-5517, YeS-5519, YeS-5521 and so on are in operation, which provide for connection of various types of NML. For example, the storages YeS-5010 and YeS-5012 can be connected to the UU NML YeS-5511. The structure of the YeS-5517 provides for joint operation with the YeS-5012, YeS-5017, YeS-5019 and YeS-5022 storages connected to the input-output channels of the YeS-1020, YeS-1022, YeS-1030, YeS-1033, YeS-1050, YeS-1060 model computers. The YeS-5525 unit permits joint operation with storages using the BVN-1 recording method and storages using two recording methods -- BVN-1 and FK-write. In addition, this unit can operate with the NML having different tape speeds.

The majority of UU NML provide for writing and reading information with a density of 8 and 32 bits/mm. The write and read density for each serviced storage is given by command from the channel. Information is written with the tape running forward, and it is read either moving forward or in reverse.

The data transmission speed between the UU NML and the channel is determined by the NML model, the recording density used and the type of UU NML. For example, for the YeS-5517, the data transmission rate for a density of 32 bits/mm will be as follows: for the models YeS-5012 and YeS-5017, 64 kbytes/sec; for the YeS-5019, 96 kbytes/sec; for the YeS-5022, 128 kbytes/sec. With a write density of 8 bits/mm,: for the YeS-5012 and YeS-5017 models, 16 kbytes/sec; for the YeS-5019,24 kbytes/sec; and for the YeS-5022, 32 kbytes/sec.

All of the UU NML operate in two modes -- autonomous and complex (jointly with the computer). The UU is switched from the autonomous mode to the complex one from its control panel.

Structurally all of the UU NML are executed in the form of an instrument bay, the frame of which is made of welded steel framing. The sides of the bay are covered with easily removable sheathings, front and rear have double doors. The right door of each double door has a lock for holding them in the closed position. Both doors have stops which do not permit them to be open more than 90°. In the lower part of the bay there is a dust filter. At the top the bay is closed with a grid and upper sheathings. The bay is installed strictly vertically using legs that adjust with height. Inside the bay are two frames, one sliding and the other stationary. Both frames are welded and made of aluminum section. All of the

equipment is placed on these frames: a control panel, the display panel, the switching panel, the TEZ modules, standardized feed units and feed control unit and fans. Plugs for connecting the inside and outside cable connections are fastened to special brackets on the sliding and stationary frames.

Synchronization Circuits. Different models of NML can be distinguished by at least two parameters: the tape speed and recording density. Taking this into account in the UU NML, synchronization means are provided which are designed for different combinations of values of these parameters. For synchronization of all of the operations performed by the storage, in the UU NML there are four synchronizing generators: the read synchronizing generator GSCh; the write synchronizing generator GSZ; the microsecond delay generator GMKZ; the millisecond delay generator GMLZ.

Figure 11.2 shows the interrelation of the synchronization circuits making up the UU NML. In these circuits three clocks are used, each of which has a fixed frequency. The read clock TGCh forms the clock pulses for synchronizing the circuits that operate when performing the read operation, and the write clock TGZ, for synchronizing the write circuits. The operating frequency of these clocks is given by the contents of the write density register RPZ and the model number register RNM. The pulses from the clock TGCh start the clock GSCh, and the pulses from the TGZ start the GSZ and GMKZ clocks.

The read synchronizing generator GSCh services the read synchronizer SS, the basis for which is a three-bit counter with scaling factor $K_{count}=8$. During operation of the read synchronizer, the counter counts from 0 to 7, inclusively, and then it begins to count from zero (cyclic mode).

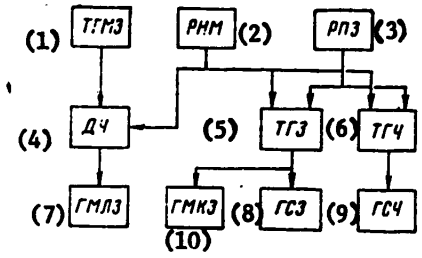

Figure 11.2. Synchronizing generator

Key:

1.	TGMZ	6.	TGCh
2.	RNM	7.	GMLZ
3.	RPZ	8.	GSZ
4.	DCh	9.	GSCh
5.	TGZ	10.	GMKZ

The write synchronizing generator GSZ services the write synchronizer SZ, the basis for which is a four-bit counter with scaling factor $K_{count}=16$. The write synchronizer also operates in the cyclic mode. A data byte is written on the tape in each operating cycle of the synchronizer.

The pulse repetition frequency of the GSCh and GSZ is selected in accordance with the model of the NML and the write density. For example, the model YeS-5017 with density of 32 bits/mm, the pulse repetition frequency is equal to 500 kilohertz, and with density of 8 bits/mm, it is 125 kilohertz.

The millisecond delay clock TGMZ has an operating frequency of 5 kilohertz which by the frequency divider DCh (see Figure 11.2) can be decreased by twofold or fourfold depending on what type of NML the UU NML is working with. The TGMZ pulses control the GMLZ generator. Each synchronizing generator has a controlled input, as a result of which the generators form pulses only when this is necessary for the UU NML.

The GMLZ and GMKZ generators service the control assembly of the write and read circuits. The GMLZ generator is used to generate a delay for the tape start and stop time, for the interval erase time and also when writing zones in the autonomous mode. The GMKZ generator is designed for generating pulses used by the control assembly of the write and read circuits to measure the intervals between rows on the tape when writing and reading the STsK and SPK check rows and also when processing the end of operation. The basis for the write and read circuit control assembly is a 9-bit delay counter with scaling factor K_{count}=255. In the microsecond mode the delay counter is started by the GMKZ generator, the frequency of which is selected as a function of the NML model and the recording density. For the YeS-5017 with a density of 32 bits/mm, it is 512 kilohertz, and for a density of 8 bits/mm it is 128 kilohertz. In the multisecond mode, the delay counter operates on one of three frequencies: 2.5 kilohertz when working with the YeS-5012 and YeS-5017; 3.75 kilohertz for the YeS-5019 and 5 kilohertz for the YeS-5022.

11.4. Electric Power Supply for the Controller

The electric power supply system for the UU NML magnetic tape controller YeS-5517 (Figure 11.6) includes the following: the feed control unit BUP; the power pack BP1 (YeS-0904) providing stabilize voltage of +5 volts (admissible load current 18 amps); the BP2 and BP3 power packs (both YeS-0905) giving stabilized voltage of +5 and -5 volts, respectively (admissible load current 3.6 amps). In addition, the electric power supply generates a three-phase ac voltage of 380/220 volts for powering the NML.

The feed voltage to the network filter SF of the electric power supply and the NML is fed from the ac, 380/220 volt network with 50 hertz frequency. The admissible voltage deviations from the rated value lie within the limits from +10 to -15%. The network filters are designed to lower the level of pulse and high-frequency interference of the feed network and the interference generated by other units. From the network filters the three-phase voltage of the primary network is fed to the BUp which distributes it to the power packs BP1, BP2, BP3 and the fans V1, V2 and V3.

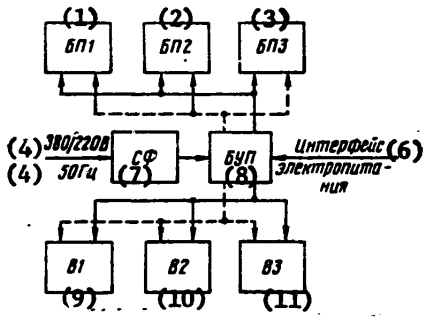

Figure 11.6. Structural diagram of the power supply for the YeS-5517 controller

Key:

1. BP1
2. BP2
3. BP3
4. 380/220 volts
5. 50 hertz
6. Electric power supply interface
7. SF
8. BUP
9. V1
10. V2
11. V3

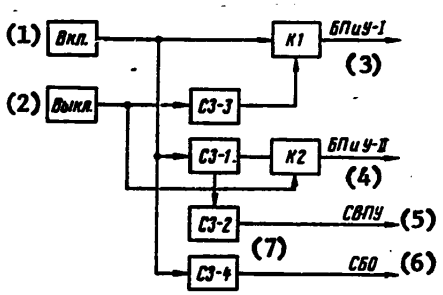

Figure 11.7. Structural diagram of the feed control unit

Key:

1. on
2. off
3. BPiU-I = power packs and first stage assemblies
4. BPiU-II = power packs and second stage assemblies
5. SVPU
6. SBO
7. SZ ...

The control of the electric power supply, warning and protection are realized by the power supply interface. Three control modes are possible: local from the display panel of the YeS-5517, local from the BUP and remote from the power supply control panel of the computer.

When the BUP is on, the feed voltage is fed to the BP1, BP2 and BP3 and the fans in three stages: fans are connected to the first stage, then the service ac voltage of 20 volts is fed, and the primary network voltage is fed after 20 to 30 milliseconds. When the BUP to the first stage is off, the primary network voltage is off, the service voltage is disconnected after 20 to 30 milliseconds, and then the fans are switched off. In addition, the BUP outputs a dc voltage of 24 ± 0.3 volts. The BUP includes three transformers, electrifier, stabilizer and control circuit.

The BUP control circuit (Figure 11.7) contains the following basic elements: the power on button Vk1 and the power off button Vylk. Switches K1 and K2 for the primary network and service voltage; delay circuits SZ-1 ... SZ-4.

When pressing on the power on button, the switch K1 is switched on, sending the ac service voltage of 20 volts to the power packs and the first stage assemblies (BPiU-I) and then the three-phase 380/220-volt voltage. Simultaneously, the delay circuits SZ-1 and SZ-4 are started. After 200 to 300 milliseconds the signal from the output of the SZ-1 starts the SZ-2 and switches the switch K2 on. The latter sends the ac service voltage and then the primary network voltage to the power packs and the second stage assemblies (BPiU-II). After 200 to 300 milliseconds, the signal to switch on the power supply (SVPU) arrives at the

output of the SZ-2, and after 2-3 seconds, the blocking signal of one of the emergency disconnect channels (SBO) arrives from the output of the SZ-4. When pressing on the power off button, the switch K2 is disconnected, and the delay circuit SZ-3 is started. After 200-300 milliseconds, a signal that disconnects the switch K1 appears at its output.

In the electric power supply of the YeS-5517 provision is made for protection from disappearance and overage of the stabilized voltages, from overloads and short circuits with respect to output voltages and disappearance of a phase of the primary network. In these cases a failure signal is generated which breaks the emergency signal circuit, which leads to impossibility of reclosure of the UU NML. There is also blocking that excludes the possibility of switching on the electric power supply in case of improper installation of it with respect to location and in the absence of any module, fan or failure to connect critical parts of the plug. On the face panel of the BUP and the display panel there is a light display for the presence of the ac feed voltage of the primary network, switching the unit on and off, emergency conditions and preventive control. In addition, the emergency and preventive control signals are coupled out to the electric power supply control panel of the computer.

11.5. Checking the Fitness of the UU NML Tape Controller Equipment and Possible Failures

The fitness and proper operation of the UU NML are checked during its operation under complex and autonomous conditions using circuits specially provided in the unit for this purpose and also using monitoring and measuring equipment.

Checking Out the Controller Equipment Operating Under Complex Conditions. The fitness and correctness of the operation of the basic assemblies and modules of the UU NML tape controller are checked under these conditions by special circuitry of the device. For example, these include the state and sense byte modules, the sequence of performed operations display, various check circuits and error forming assemblies.

The basic state byte module is designed for shaping the basic state byte code which is transmitted to the channel at the end of the initial access and on completion of the executed instruction. The module includes the basic state flip-flops which establish the end of operation of the channel, including the presence of an error in the UU NML and in any NML.

The sense byte module is used to gather and output detailed information to the channel about the state of the UU NML and the storages, about a failure or error appearing in the execution of the preceding input-output operation. The sense byte is output to the channel on the "sense" instruction. In the YeS-5517 there are six sense bytes, in the bits of which the state of the controller and the magnetic tape storage is depicted. For example, in byte 0 the second bit informs of an error in the channel buses, the third bit, an error in equipment; in byte 3 the second bit communicates an extraordinary misalignment during check reading, the third bit, an error in the RTsK register; in byte 4 the 0 bit informs that none of the write flip-flops is operating in the NML, and the second bit, an error in the read synchronizer SS, the third bit indicates an error in the write synchronizer SZ.

The sequence displays are designed to check the sequence of the performance of the operations causing movement of the magnetic tape in the NML. The sequence display is a three-bit counter. During the execution of each operation it goes through various steps. The counter is switched at the end of each proper execution of a step of the operation. On proper execution of the operation the countery can reach the maximum and be cleared. One or several counters not cleared indicates improper operation of the UU [controller] or the NML [magnetic tape storage]. Since each step of the operation corresponds to a defined state of the counter, it is possible to use the state of the counters to determine the cause of an error in the UU or the NML.

The information check circuits are designed to check the transmission of data through the UU NML. These circuits include the following: the parity check circuits in the RZS, RPK, RP and RTsK registers, the skew check circuit; interference detection circuit in the intervals when performing the write, read and other operations.

The equipment check circuits control the operation of defined circuits of the UU NML. They include the following: the SZ and SS check circuits; the echo error check circuit; the delay counter check circuit. On detecting an error each of the check circuits sets the "error in the unit," "error in information," or "error in equipment" display.

The error formation assemblies consist of a number of circuits designed for shaping and recording errors discovered during operation of the UU and NML.

Checking the UU Equipment in the Autonomous Mode. During checks, repair and adjustment of the UU and the NML in the autonomous mode, their operation is controlled from the control panel of the UU. Using the panel, jointly with special autonomous control circuits, it is possible to check the majority of the systems and circuits of the UU and the NML. Visual checking of the operation of the unit is realized in this case by means of the display tubes located on the display panel (the interface signal display, the UU and NML states; the write and read synchronizers and the delay counter; errors determined by the UU systems; information contained in the UU registers).

The following manipulations can be performed from the control panel of the UU NML: checking information contained in one of six registers of the UU (RK, RZS, RTsK, RPK, RP, RO); setting up the input-output instruction and address codes of the UU; setting up and recording zones of 1, 8, 16 and 128 bytes or of arbitrary length; simulation of parity errors in the write lines of the UU and checking the operation of the error detection systems; checking the operation of the error correction system; assignment and execution of the diagnostic operating mode of the UU and the NML.

In order to perform the enumerated operations, the required switches, keyboards and display tubes equipped with inscriptions are available on the control panel.

Equipment Checking Using the Monitoring and Measuring Equipment. In order to measure the parameters, adjust and tune the circuits of the UU NML (YeS-5517) the following are used: an eletronic oscillograph type S1-65; a combination device type Ts-434; the digital frequency meter ChZ-12; the dc voltmeter M109; the stand for checking the special TEZ -- YeS-A104; stand for checking logical TEZ -- YeS-A102. The parameters, the adjustment and tuning of the circuits and assemblies of the UU NML using monitoring and measuring equipment and stands are carried out according to operating instructions.

After preventive, adjustment and checkout operations, a mandatory check is made on the technical condition of the UU under autonomous conditions by performing all of the instructions provided for by the instruction manual and given by the operator from the control panel. Then the unit is checked together with a computer on a test program specially written for this purpose.

Characteristic Failures. Let us consider some characteristic, frequently encountered failures of the UU NML, their probable causes and means of eliminating them.

The device is not switched on, the "emergency" display light burns on the BUP panel. The cause is burnout of the light fuse in the BUP or in the fan.

The instruction is rejected. The "instruction reject" light burns on the display panel of the unit. This can occur when it is proposed that the unit perform a forbidden or inactive instruction or in case of failure of the "instruction refused" signal formation circuit. It is necessary to check the presence of a data protection ring on the reel of the corresponding NML, determine the type of operation, check the ShIN-K reception circuit and the "instruction reject" signal formation circuit. If either of the latter has failed, it is necessary to check the corresponding TEZ on the bench. If when determining the instruction code it turns out that the instruction code does not exist, it is necessary to bring it in correspondence with the program.

The BUS-K error. The "parity BUS-K" display light burns. The reason for this can be improper operation of the ShIN-K reception assemblies, the check circuit, the "BUS-K error" signal formation assembly or the channel itself. In order to establish the location of the error, it is primarily necessary to check the information coming from the channel, then check the operation of the BUS-K reception unit and then the BUS-K error formation unit.

The "intervention required" and "error in the unit" display lights burn. This can be caused when the channel accesses the UU or NML while it is off or it is not ready. If it was discovered that the requested NML is off, then it must be switched on. If one that does not exist or is not ready for operation is requested, then a correction must be made to the program or the NML must be made "ready."

The "parity error in the RP register" display light burns. The probable cause of this is absence of write or read with respect to one of the bits, incorrect operation of the RP or a magnetic tape defect. In the given situation, above all it is necessary to check the presence of write signals from the UU NML to the NML and the presence of read signals with respect to all bits. Then proceed to check out the operation of the RP register, the read information reception module, the

RK register check circuit and the error formation circuit. A magnetic tape defect is discovered as follows: before executing the WRITE instruction, the ERASE INTERVAL instruction is executed, and then the write is done in the zone in one section of the tape. After determining the specific location of the error, the corresponding TEZ is checked on the stand.

The "parity error in the RZS register" display light burns. This situation can be caused by improper operation of the register RZS or the STsK line forming circuit (Skh TsK). It is necessary to check the following: correctness of operation of the RZS register check circuits, the formation of the "RZS error" signal and the "Chet. RZS" signal of the STsK line and also the correctness of entering and clearing information in the RZS. The TEZ of the discovered failed assembly is bench tested.

Skew error. The "skew" display byte burns. This means that the time interval between the first and last bits of the received byte exceeds the admissible value, or the "skew" signal shaping circuit is not functioning. In this case it is necessary to check the dispersion between the read bits and the "skew" signal shaping circuit.

NML reject. The "NML reject" indicator light burns. This state can be caused by losses of the write or read state or during the performance of an operation in the NML, a not ready state has occurred. In the latter case, the NML is made ready, and in other cases, its operation is checked out.

The "echo error" indicator light burns. This can occur when the information is not written on magnetic tape or when the "echo error" signal circuit is operating incorrectly. Therefore, first the presence of signals on the write wires is checked, and then the operation of the "echo error" signal shaping circuit. If it is discovered that the echo signal does not come from the NML, then the failure is looked for in the NML.

In conclusion let us note that both of the presented failures are reported to us by the indicator lights on the display panel of the UU NML, which is one of the positive aspects of all of the units of the unified system of computers.

CHAPTER 12. MAGNETIC DRUM STORAGE

12.1. General Description

Magnetic drum storages (NMB) are among the storage units with cyclic access to the information, for while the drum is turning each cell periodically passes under the magnetic heads. For the most part the NMB are used as buffer memories, and more rarely as external memories. The NMB is very useful for a program generating a large number of intermediate results. It is also convenient to store a copy of the operating system on the drum storage, for the subroutines of the operating system must be accessed quickly, and they are used frequently. In addition, the NMB is convenient for use in collective-use computer systems (VS), in which many programs are executed simultaneously. Here during operation of the VS, copies of new programs for replacing the program executed at the given time must be quickly and frequently input to the OOP. The NMB used as a buffer memory handles this problem most successfully.

The basic disadvantage of the NMB is the fact that the information carrier (the magnetic drum) is not replaceable. In addition, it is significantly more expensive than magnetic disc storage (NMD).

At the present time three types of NMB have been developed and manufactured which are designed for operation in the unified system of computers: YeS-5033 (USSR), YeS-5034 (Poland), and YeS-5035 (German Democratic Republic).

Basic Specifications

	YeS-5033	YeS-5034	YeS-5035
Capacity, megabytes	5.6	2	2
Number of working tracks	800	-	532
Recording density, bits/mm	42	-	33
Average access time, milliseconds	20	20	20
Data transmission speed, megabyte/sec	1.2	0.1	0.8
Drum rpm	1500	-	1500
Drum diameter, mm	450	-	320

The NMB is a device with a magnetic head for each magnetic track. The choice of the required magnetic track is made by electric switching of the magnetic heads.

The only mechanical motion which takes place under normal operating conditions of the NMB is turning of the magnetic drum which is sustained at constant velocity. Inasmuch as we are dealing with a rotating carrier, some time is needed to find the required block of data.

The time required for access and transmission of data in the NMB is made up of three components: the magnetic head access time, the turning delay time (the time required for the carrier to turn) and the data transmission time. The magnetic head access time is small by comparison with the other components. The turning delay time consists of the time of angular rotation of the MB [magnetic drum] required to bring the required zone under the record-reproduction head. This time on the average is equal to half the time of a full turn of the drum. The data transmission time between storage and the OOP is a function of the drum speed and the recording density of the data on the carrier. The NMB are connected to the SK through controllers. The maximum number of drum storages connected to a selector channel is eight.

12.2. Structural Design and Basic Assemblies

The YeS-5033 drum storage is structurally executed on the basis of a standard bay in which the following are located: magnetic drum, cross pieces with magnetic heads control unit with control panel, electronic record, reproduction and magnetic head switching circuits, small standard interface, the feed control unit and the power pack and also fans. In order to realize internal and external connectrions, plugs are used. In the storage a system to protect against loss of power is also provided. When the feed voltage drops, the protection system withdraws the cross piece arm and instantaneously disconnects the magnetic drum. The working surface of the drum used in the YeS-5033 is coated with cobalt-tungsten alloy.

The YeS-5035 magnetic drum storage includes the same functional modules as the YeS-5033. Distinguishing features of this device are a different structural solution and the use of ferrolac as the magnetic coating for the drum.

Magnetic Drum. The basic part of any NMB is the magnetic drum - this is a carefully machined cylinder, the diameter of which can fluctuate for different storages within the limits from 100 to 1200 mm, and the length from 200 to 900 mm. The drum diameters of the YeS-5033 storage are 450 mm, for the YeS-5035 they are 320 mm. The magnetic drum (MB) is made of metal by casting or cold working. The best material for making the MB is stainless steel. It is resistant to external effects and is well subjected to machining.

The drum is a hollow cylinder (Figure 12.1) (solid of revolution) 1. Inside the drum is a built-in reversing type electric motor which contains a rotor 5 pressed into the solid of revolution, and a stator 4 seated on a stationary shaft 3. The feed voltage to the rotor and stator windings is fed over lines that run inside the shaft. The rotor turns in the bearings 2 and 6 seated on the stator shaft. The drum is installed vertically. The drum stator is attached to the cast base using brackets.

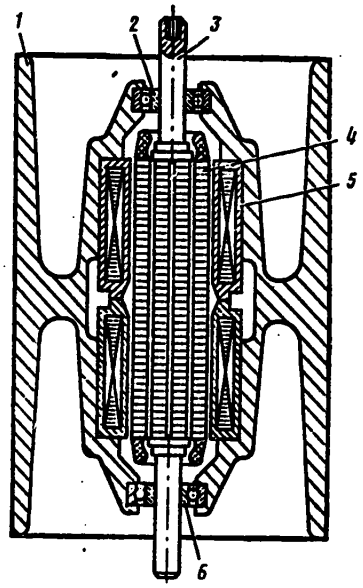

Figure 12.1. Structural diagram of a magnetic drum

The cross pieces with magnetic heads are arranged near the surface of the drum on the generatrix of the cylinder and are attached to the base using special brackets. In the YeS-5033 storage there are 40 cross pieces, on each of which 22 floating magnetic head modules are installed. Each module contains two heads in a single housing. The cross pieces can be rotated on their axes, as a result of which it is possible to bring them up to the magnetic drum surface and withdraw them. The cross piece is moved by electromagnets. When the magnetic drum reaches its rated rpm, a start voltage is fed to the electromagnets. After the cross pieces take up the working position, microswitches respond providing for feeding the working voltage to the electromagnets (3 to 5 times less than the starting voltage). The cross piece is withdrawn by springs installed on the cores of the electromagnets after the feed voltage is shut off.

In order to protect the magnetic surface from damage by dust, the drum is placed in a sealed housing which is reached by air through an oil filter. The housing has an organic glass window designed to inspect the working surface and two removable side covers. In some cases the magnetic drum is placed in a sealed housing filled with helium, use of which lowers the heating temperature of the drum and protects its surface from oxidation. There are sealed plugs to connect the magnetic drum to the electronic part of the storage and the control unit.

In all of the NMB designed for operation as part of the unified system of computers, floating magnetic heads are used. One of the methods of creating the floating heads is based on using the aerodynamic effect. In the case of fast turning of the drum, the surrounding air is entrained by its surface, creating an air cushion. As a result of this effect, the magnetic head is lifted, repelling it from the drum surface. On the other hand, the floating element is clamped against the surface of the magnetic drum by a spring which equalizes the lift of the air cushion. The floating element follows the surface of the drum by this effect. At the rated

drum rpm, a dynamic equilibrium of forces created by the air cushion in the spring is set up. A constant gap of 5 to 10 microns is maintained between the magnetic heads and the drum surface.

In order to avoid spoiling the magnetic coating and the heads during acceleration and braking of the drum the heads must be withdrawn from its surface.

The parallel-series method of locating data is used in the magnetic drum storages of the unified system of computers. For example, there are 800 information tracks on the YeS-5033 magnetic drum. Each track is assigned its own magnetic head. The data are recorded and read simultaneously on eight channels.

The size of the magnetic head greatly exceeds the track width; therefore the heads are placed along a spiral around the drum. The spiral arrangement of the heads permits each of them to take up the required position vertically in spite of its significant width. The sign of the beginning of the drum is an index marker recorded before the beginning of each information track.

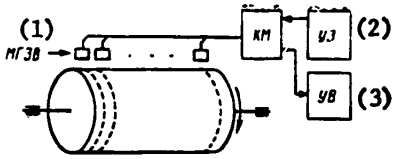

Figure 12.2. Arrangement of information on a drum by the series method
Key:
1. MG EV
2. UZ
3. UV

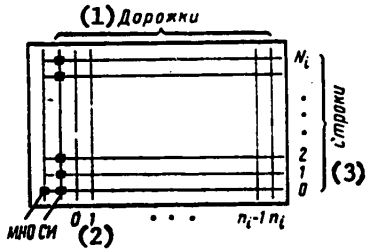

Figure 12.3. Arrangement of information on a drum by the parallel method
Key:
1. Tracks
2. MNO SI
3. Rows

The drum surface is uniformly distributed so that 800 working heads and 80 spare heads can be placed on it. In order that each track be addressed, the magnetic heads are divided into several groups (Figure 12.4). For this purpose the MG [magnetic head] surface is divided into four equal sectors which are assigned the numbers 0, 1, 2 and 3. Each sector takes an arc of 90° and contains 220 magnetic recording and reproduction heads. The given sector includes only the magnetic tracks (heads), the index marker of which is located in this sector.

In each sector there are 10 cross pieces, on each of which there are 20 working magnetic heads and two spare ones. On the cross pieces there are also an electronic switching circuit for the magnetic heads. The cross pieces with even numbers are located in the upper part of the drum, and with odd numbers, in the lower part. The head address (its position) is determined by three numbers: the sector number, the cross piece number on which it is located and its position on the cross piece.

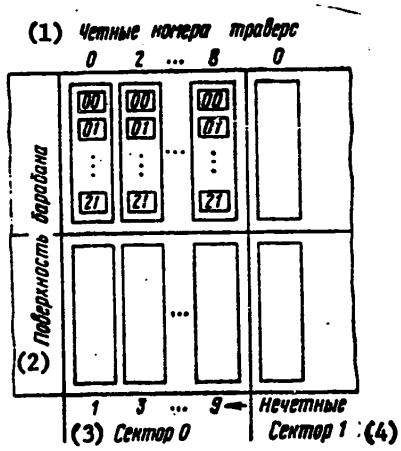

Figure 12.4. Arrangement of magnetic heads in groups

Key:
1. Even numbers of cross pieces
2. Drum surface
3. Sector 0
4. Odd sector 1

If any head or track turns out to be unsuitable, the cable with this head is switched to one of the spare tracks on the same cross piece. Here the spare head and track replace the unsuitable head or defective track.

The circuit diagram of the YeS-5033 storage is executed from series 155 integrated microcircuits. In addition, special TEZ and several nonstandard circuits are used in the storage (pulse shapers, converters of different types of signals to signals with the parameters of the series 155 microcircuits, reproduction and recording amplifiers, electronic switching, filtering and protection circuits).

12.6. Characteristic Failures and Preventive Operations

Operating Characteristics of the Magnetic Drum Storage

In order to maintain fitness of the storage it is necessary to consider its operating characteristics. All of the NMB must operate under conditions stipulated in the operating instructions. During operation of the storage it is necessary to observe the following order of switching on the modules: switch on the three-phase 220/380 volt, 50-hertz voltage; switch on the fan; switch on the dc feed voltage; switch on the magnetic drum.

The storage element is shut down in the following sequence: switch off the drum while pressing the "drum off" key; switch off the feed voltage by pressing the "power off" key; switch off the fan.

The magnetic drum can operate only with the housing and side covers tightly closed. The screws of the housing and covers must be well tightened. It is permissible

to remove the housing and covers only when performing preventive control work. The filler of the moisture-absorbing cartridge and color of the standard applied to the cartridge glass must be different colors. The direction of rotation of the drum must correspond to the direction of the arrow applied to the transparency with the inscription "drum turning direction." On the appearance of drops of moisture on the surface of the magnetic drum or on the inside surface of the inspection glass, it is necessary to replace the moisture absorbing cartridge and check the reliability of the fastening of the drum housing and side covers. For acceleration of the absorption of the moisture, it is necessary to lift the cross pieces, switch on the drum and leave it operating until the drops of moisture completely disappear.

During the first two hours of operation of the storage it is necessary to check the absence (presence) of scratches on the working surface of the drum every 30 to 40 minutes of its operation through the inspection hole, and during subsequent operation of the drum, no less often than twice a day. It is not permissible to bring the cross piece to the drum surface if it has not reached its rated speed. The opening of the drum housing is permitted only in a facility with dust and moisture content admissible for the separation.

Preventive Control Work. Preventive maintenance is performed periodically on the storage after every 500 hours of operation, but no more rarely than once in 3 months. The preventive maintenance operations on the storage include the following: external inspection of the storage and checking the parameters of the output signals with the rated voltages stepped up and down by 10%. During external inspection, the integralness and cleanness of the magnetic coating, the state of the soldering are checked, and the foreign objects, dust and dirt are removed, the fastening of the plugs, terminals, screws and nuts is checked. The surface of the magnetic coating in the inside cavity of the magnetic drum is degreased by a cambric cloth wet in distilled alcohol with subsequent drying with a dry cloth.

After every 2000 hours of operation of the storage, but no more rarely than once every 6 months, adjustments are made as follows: inspection of fasteners and visual inspection of the quality of the magnetic head solder; removal of contamination from the assemblies and parts of the magnetic drum; washing of the plug contacts and the contacts of all the cells of the storage with distilled alcohol; washing of the magnetic coating of the drum and floating elements of the BMG; lubrication of the bearings and working surfaces with TsIATIM-221 lubricant; checking the output signal parameters at rated voltage stepped up and down by 10%.

The field cells, magnetic heads and other elements of the storage are replaced in accordance with the results of the preventive tests. The moisture absorbing cartridge is replaced when the color of the filler (silica gel) becomes identical with the color of a standard placed on the protective glass. After performing the preventive control operations, the fitness of the storage is checked during its joint operation with the UU NMB drum controller under autonomous conditions by a special test program.

Characteristic Failures, Methods of Detection and Elimination. Failures occurring in various functional assemblies of the magnetic storage disturb the normal operating conditions and can lead to impossibility of using the storage for its

purpose. The presence of failures in the storage in the majority of cases is directly or indirectly depicted on the control panels of the magnetic drum storage, the magnetic drum controller and the central processor. The failure is found, as a rule, under autonomous conditions during joint operation of the NMB and the UU NMB controller. The most characteristic and frequently encountered failures indicated in the instructions for operation of the device and also discovered and recorded during working with the drum storage are easily detected and eliminated. It is possible to include the following among such failures.

On pressing the "drum on" key, the magnetic drum does not come on, the "network" indicator lights up on the panel. This is possible if one of the fuses is burned out in the feed circuit for the electric motor that drives the drum or if a relay has failed in the feed control unit. Possible causes of failure must be checked out.

The direction of rotation of the drum does not correspond to the direction indicated on the special transparency by the arrow. This case is observed in case of improper sequence of phase alternation of the primary network. It is necessary to change places with feed phases A and B on the power panel.

When the "drum on" key is pressed, the "phasing" indicator lights on the control panel. This state is observed also in case of improper phase sequence.

The drum turns, and the cross pieces do not move up to the drum. This failure can be caused by the absence of feed voltage on the electromagnets that withdraw the cross pieces or failure of the electromagnets themselves. It is necessary to check for a failure in the fuses or windings of the electromagnets and also the electromagnet feed blocking circuit. The cause of this state can also be incorrect positioning of the "mode," "automatic-manual" flip-flops. In this case the flip-flop must be switched to the "automatic" position.

With the cross piece moved up to the drum, the "cross pieces ready" display does not light up. This can be caused by failure in the light itself or the feed circuit.

There are no output signals when the read operation is performed. Probable causes of this state of the storage can be as follows: absence of one of the feed voltages in the reproduction channel; the cross pieces with the magnetic heads are not in contact with the magnetic drum surface; there is no signal permitting reproduction of information (fed from the computer), the magnetic head switch does not operate. In the first case it is necessary to check the presence of feed voltages in the reproduction channel using the monitor jacks. If one or several feed voltages are absent, it is necessary to discover the cause. In the second case, the failure is discovered and eliminated, as a result of which the cross pieces do not make contact with the magnetic drum surface. In the third case the presence of a signal permitting information reproduction is checked. If the magnetic head switch does not operate, then the failure of the head address decoder DShAG is checked.

The amplitude of the signal reproduced by the magnetic heads of one of the groups is low or less than the allowable. This situation can occur if one or several diodes in the magnetic head circuit is punctured or the surfaces of the drum or floating elements are dirty. In the first case the forward and return resistance of the diodes in the given group is checked out, the module with the failed diode is replaced. If the surfaces of the magnetic head or the floating elements of the magnetic head module are dirty, then they are washed with distilled alcohol or highly pure hydrolyzed alcohol.

There is no recording and reproduction by one or several of the magnetic heads. The cause for this can be a break in the magnetic head circuit or the presence of a bad diode. In the first case the magnetic head module is replaced, and in the second case, the diodes are checked, and if necessary, the module with the failed diode is replaced.

There is no output signal in one of the communication channels between the storage and the controller. The reason for this can be failure of the corresponding magnetic head, failure of one of the cells of the reproduction channel or a breakdown of the output circuit. A failure in the output circuit is checked out by a continuity test, and the failed magnetic head or cell is replaced by a good one.

When reproducing the information on oscillograph screen, the interference signals are seen, their amplitude is higher than the useful signal and disappears when the cross pieces are withdrawn from the magnetic drum surface. This is observed when the winding insulation of one of the magnetic heads is punctured to its core (a magnetic circuit). The failure is discovered as follows. The cross piece is brought up to the drum surface. The oscillograph input is connected alternately to the windings of the magnetic head of the given group. The head in which insulation breakdown has occurred gives out the maximum interference signal amplitude. On withdrawing the cross piece from the drum this signal decreases. The failed head detected in this way is replaced.

On the working surface of the magnetic drum there are bands with the coating disturbed. This can be caused by the presence of foreign particles in the gap between the magnetic head and the drum surface or the presence of embedded particles in the organic glass of the floating element. If on examination foreign particles are detected, it is necessary to find the cause of them. For this purpose, the seal of the magnetic drum housing is checked, integralness of the oil filter is checked and all of the mechanical assemblies capable of becoming the cause of the appearance of foreign bodies are also examined. The contact traces on the drum, the floating elements of the magnetic head are wiped with a cambric cloth wet in distilled alcohol with subsequent drying with a dry cambric cloth. The magnetic heads in which the presence of embedded particles is assumed, is removed and carefully examined to detect the embedded particles. In the absence of such particles the BMG is put in place; in the presence of embedded particles, it is replaced. The magnetic heads are removed and reinstalled strictly in accordance with the instructions for technical maintenance of the storage.

When finding failures and performing preventive monitoring operations, the monitoring and measuring equipment, tools and materials recommended in the instructions for technical maintenance of the storage are used. After detection and elimination of failures, the fitness of the storage is checked out during joint operation of it with the controller in the autonomous mode using a special test program.

CHAPTER 13. MAGNETIC DISC STORAGE

13.1. Basic Characteristics and Structural Principle

The VZU on magnetic discs (MD) are direct-access type storages. They have high information capacity and very high speed. They combine the advantages of the NML having high capacity and the NMB having short access time. By comparison with the NMB, the magnetic disc storage (NMD) in the same physical volume has many times greater working surface of the carrier for storing the information. The capacity of the modern NMD reaches 100 or megabytes, and the information exchange speed reaches up to 10^6 bits/sec.

At the present time NMD (YeS-5050, YeS-5051, YeS-5052, YeS-5055, YeS-5056, YeS-5068, YeS-5060) are an operation which were designed to work as VZU in the unified system of computers. The basic characteristics of all the enumerated storages, with the exception of the YeS-5051 are identical; therefore here and hereafter characteristics of only the YeS-5056 and YeS-5051 are presented:

	YeS-5056	YeS-5051
Capacity, megabytes	7.25	100
Recording density, bits/mm	29-44	29-44
Average access time, microseconds	90	420
Data transmission speed, kbytes/sec	156	83

The YeS-5050, YeS-5052, YeS-5055, YeS-5056 and YeS-5058 storages operate with replaceable discs. The package for each of these storages includes six discs with ten operating surfaces. The YeS-5051 storage is stationary. It has 36 permanently attached discs separated into two submodules of 18 discs each. The total number of working surfaces is 64.

The basic advantage of storages with replaceable disc packages is the possibility of replacing one set with another. In order to preserve the information during storage of the disc in the archive each package is placed in a dustproof shielded container made of impact-resistant plastic.

Magnetic discs are usually made of aluminum and its alloys. They are subjected to careful grinding and polishing, and then they are coated on both sides with ferrolac or metal coatings based on Ni, Co and W. The coating thickness is 1.0 to 2.0 microns. The disc diameter is from 250 to 650 mm, and the thickness is 2.0 to 2.5 mm.

The protective 5, 7 and magnetic disc 6 are rigidly fastened to the drive shaft 4 (Figure 13.1). The spacing between the magnetic discs is 7 to 8 mm from each other. Except for the top and bottom discs, both surfaces of the disc are working surfaces. In the case of the top and bottom discs, only the inside surfaces are working surfaces. Information is recorded and read by floating magnetic heads 3 attached to spring loaded arms. The arms are rigidly attached to a carriage 2 which can move in the horizontal direction. When the carriage moves the magnetic heads move along the radius of the disc. The disc rpm is 2400±48.

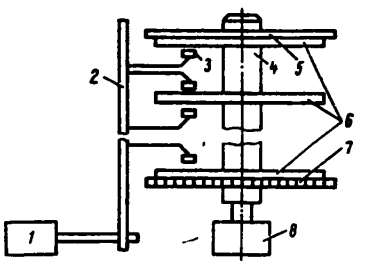

Figure 13.1. Structural design of NMD [magnetic disc storage]

When starting up the NMD from the UU NMD [magnetic disc storage controller], the signal switching it on comes in, the start relay responds, and power goes to the disc drive 8. When the discs reach 70% of the rated speed, the signal is generated for mechanical cleaning of the package of discs. During the cleaning cycle soft brushes installed on opposite sides of the magnetic heads pass over the entire working surfaces of the disc, cleaning dust and dirt off them. After cleaning a waiting time of 200 to 300 milliseconds is allowed. When the discs reach rated rpm, the carriage drive 1 of the magnetic head module is switched on, and the heads are brought up to the working surfaces. Only when this condition is satisfied are the floating magnetic heads supported on an air cushion at the required distance from the disc surface.

The bottom protective disc 7 called a sectional disc, has 20 sectional cuts and projections. When the disc turns the sectional sensor SD (the speed and rpm gauge) for each cut and each projection generates a pulse. These pulses are the input pulses for the control circuit for turning the disc package. Each package of discs has its sectional disc.

The investigated design of the NMD where each working surface has its own magnetic head moving along the disc radius is not unique. In the simpler NMD, there are only two heads in the magnetic head module, one of which serves the upper sides of the disc and the other, the lower.

When selecting the required disc and the required magnetic track on the disc the magnetic head first moves vertically to the disc indicated in the address and then horizontally to the required track. In this case the track access time increases to 0.1 to 0.7 second.

The disc packages for the storages YeS-5050, YeS-5052, YeS-504 and YeS-5058 consist of 203 cylinders of 10 tracks each. The capacity of a cylinder of the enumerated storages is 36250 bytes.

On each working surface of a disc there is a group of magnetic heads consisting of the record-reproduction head and the erase head. Each of the 203 positions of the carriage with the magnetic heads corresponds to the cylinder address, and each track on a cylinder corresponds to the head address (that is, the head address permits determination of one of 10 cylinder tracks). By electronic switching, one of 10 record-reproduction heads is selected by means of which the information is recorded or read on one of the 10 tracks of the cylinder.

The longitudinal recording density of the majority of magnetic disc storages now in operation is: for track No 000, 29 bits/mm; for track No 202, 44 bits/mm.

Magnetic Heads. The disc cannot be made absolutely flat. Even careful manufacture does not permit beating of their surface to be avoided. Therefore in the NMD, a contactless recording is used with the application of floating heads permitting the gap between them and the surface of the carrier to reach 2-5 microns and be held almost constant. Each head has a working "record-reproduction" gap 5 microns wide, 1.13 mm beyond which comes the "tunnel erase" gap 10 microns wide. There are 100 turns on the record-reproduction head, and 50 on the tunnel erase head. The windings are made of wire 0.06 mm in diameter.

The housing of the floating element (Figure 13.6) is made of TsM-332 ceramic. The magnetic heads 1 (one record-reproduction and a second erase head), the cap 3, cover 2 and bushing 4 are glued to the grooves of the housing 5. The magnetic circuit of the record-reproduction head is made of two permalloy cores separated by a nonmagnetic insert made of No 405 alloy 5 microns thick. The magnetic circuit of the tunnel erase head consists of two bronze plates to which permalloy plates are glued on both sides. The nonmagnetic insert 10 microns thick is also made of alloy No 405.

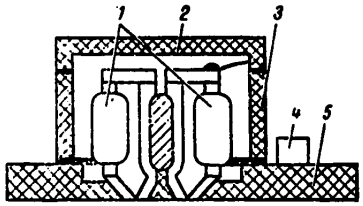

Figure 13.6. Floating element with magnetic head module

The floating element 1 (Figure 13.7) is fastened by screws to the spring suspension consisting of the arm 3, the torsion spring and ring. The arm 3 together with the floating element, cleats 2 and 4 is attached by screws to the adjustment cleat 5. When the carriage is in the withdrawn position, the end of the torsion spring is between the bulge and the arm 3 and the shoulder of the cleat 4. The working surface of the floating element is in this case 10-15 microns from the disc surface, and it is held by the spring of the arm 3.

When the lift of the air cushion becomes equal to the force of the torsional spring, the working surface of the floating element with magnetic head is set at a stable distance (2-2.5 microns) from the working surface of the disc.

In the YeS-5051, YeS-5055, YeS-5058 storages, a hydraulic drive is used, and in the YeS-5050, YeS-5050, YeS-5052, YeS-5056 storages, an electromagnetic drive.

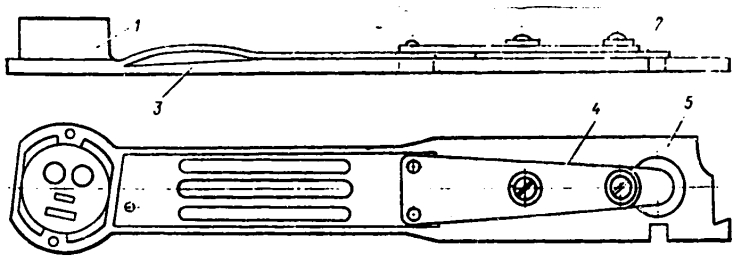

Figure 13.7. Magnetic head module on spring suspension

The electrical part of the YeS-5052 and YeS-5056 storages is primarily made from series 155 integrated microcircuits. In addition, special TEZ are used in the storage and several nonstandard systems. These are pulse shapers, pulse converters to current signals, converters of various types of signals (for example, from photo pickups) to signals with series 155 microcircuit parameters, reproduction and record amplifiers, electronic switching, filtering and protection circuits.

The parameters of the input and output signals of the storage are standardized. The logical "1" corresponds to the upper level of voltage from 2.4 to 44. volts, and the logical "0" corresponds to the lower voltage level from 0 to 0.4 volts. The read pulse repetition period in the YeS-5056 storages from 300 to 550 nanoseconds (the rated value is 400 nanoseconds) for code "1" and from 620 to 1000 nanoseconds (rated value 800 nanoseconds) for code "0." The signals from the storage to the UU NMD [magnetic disc storage controller] arrive in the form of voltage levels. The signals coming from the UU [controller] to the storage have the shape of rectangular pulses or voltage levels with switching time of no more than 50 nanoseconds. The average intake power from the ac network is no more than 1.5 kilovolt-amperes.

Magnetic Head Commutator. Selection of the required magnetic head from the ten heads used in the YeS-5056 storage is made by the magnetic head commutator KMG. It is made from three TEZ, two of them numbered 0101, one of them numbered 0102. The TEZ 0101 consists of four independent and identical MG [magnetic head] electronic switching circuits. The TEZ 0102 contains two independent and identical electronic switching circuits and a circuit for checking the correctness of the choice of magnetic heads. The feed voltages of the commutator are +20, -20 and +40 volts. The input and output signal levels correspond to the signal levels of the series 155 integrated microcircuits. The load of one electronic switching circuit is a magnetic head with record current and erase current of 200 milliamps. The maximum pulse repetition frequency of the input signal is 44 kilohertz, and the input signal duration is from 15 to 20 microseconds.

13.8. Characteristic Failures, Detection and Elimination of Them

The magnetic disc storage NMD is a device that contains complex mechanical, electric and electronic assemblies. Operating failure of even one of the numerous elements in these assemblies can lead to failure of the entire storage.

The search for a failure is not a simple problem. Successful solution of this problem depends to a great extent on knowledge of the operating principle of individual assemblies and their interaction. The experience in working with the storage and also operating instructions offer the possibility of quickly detecting and eliminating the most characteristic failures.

When the power supplies are switched on, the disc package electric motor does not turn, and the "automatic" indicator on the control panel (PU) lights up. A failure is caused by breakdown of the initial register clearing circuit when the power supplies are switched on. The TEZ of this system must be checked out.

The disc package electric motor does not come on, and the "automatic" display lights up on the PU. This situation can occur if the electromagnet for locking the disc package in place is not deenergized. It is necessary to check the relays that control the operation of the disc package locking electromagnet and the relay feed circuits.

When the "automatic-manual" button is pushed, the storage does not convert from "manual" to "automatic," and the disc package stays in place with the covers closed. This can occur if the microswitch of the static charge removal unit or one of the microswitches blocking the operation of the storage element with one of the covers open does not operate.

The electric motor of the disc package has reached the rated rpm, but the carriage is stationary. This means that the disc package speed analysis circuit is not operating. It is necessary to check the TEZ in the carriage electric drive system that converts the signals from the photo pickup to signals with the parameters of the series 155 circuits and display the sectional pulse duration.

After switching on the electric motor of the disc package drive, the carriage goes forward beyond the No 202 track until it stops and does not return. This takes place when the electromagnet of the head feed does not respond. The cause of its nonresponse can be that it is out of adjustment.

Oscillatory movements of the carriage are observed when searching for the cylinder in the vicinity of cylinders 0-202. The reason for this malfunction can be a failure of the difference counter SR or failure of the track position photo pickup.

The search for the cylinders and locking of the carriage take place with non-characteristic "scraping" noise. The probable cause of this failure is not following the carriage movement schedule. A complex adjustment must be performed and the magnetic head drive positioning system checked out.

The error frequency in reproduction has increased, the amplitude of the pulses from the output of the counted pulse shaper is less than normal. This can be caused by dirty disc or MGV or damage to the MGV. In this case the amplitude of the signals picked up from the magnetic head is small. The disc and the MGV must be washed, and if necessary, the MG, replaced.

Failure of the unit during reproduction, absence of a signal at the preamplifier output. This is observed when one of the wires connecting the MGV to the diode matrix is broken. The break is found by continuity testing.

The number of errors on one of the magnetic heads has increased. The probable causes of the errors are as follows: breaking of the ground wire of the magnetic head core; short circuiting of one of the wires connecting the magnetic head to the diode matrix to the housing of the EMB; failure of the assembly for removing static charge from the disc package.

The frequency of errors in all of the magnetic heads has increased, especially after mechanical loads or transportation. This condition can arise from weakening of the mechanical fastenings of the ground circuits, the appearance of additional electrical contacts between the modules having electrical insulation relative to the housing. The detection of this failure is realized as follows. Disconnecting the wires on making the connection between individual modules, the resistance between the bolts and the ground terminals of the modules and the housing of the unit is determined. The resistance must be no less than 100 kilohms.

A failure during performance of the reproduction operation, no information on write. This is observed if the write amplifier has failed. It is necessary to check the TEZ 0103.

Frequent errors in the device when performing the reproduction operation. This situation can be caused by poor quality of grounding the magnetic heads, the housing of the carriage with the EMB plate or exceeding the rated (0.5 ohm) transient dynamic resistance of the static charge pickup unit by several times. It is necessary to tighten the ground screws, wash and dry the brushes and the contact surface of the assembly for picking up static charge. In conclusion, it is necessary to check the transient dynamic resistance with respect to the procedure presented in the operating instructions.

The BUP is switched on, and the "emergency" display lights up. This can occur in the absence of one of the primary feed voltage phases or when pressing the "emergency off" button. It is necessary to take the button out of the on position, check and replace the A, B, C phase fuses on the control panel of the BUP.

Failures occurring in the storage are determined during joint operation of the storage with the control unit based on analysis of external signs and the operating logic of the storage. In order to facilitate and accelerate finding the direct cause of the storage failure, monitoring and measuring equipment is used.

When finding the failures and performing the monitoring and measuring operations with the YeS-5056 storage, it is possible to use the following: the unit for

checking the YeS-A503 designed to check the operation of the storage, the disc control package YeS-A538 designed for adjusting the magnetic heads and the SD, an oscillograph of the S1-17 type with preamplifier modules designed to examine the signals and their time relations, the Ch3-39 digital frequency meter designed for exact measurement of the time intervals, a combination Ts-4312 device with 1.0 to 1.5 precision class, the R316 dc bridge for exact measurements of electrical resistance, the B5-7 type dc voltage supply for adjusting the drive, the drive control simulator for adjusting the drive; the TEZ 0140 is a linear converter of the pulse repetition frequency proportional to the speed of the carriage drive to dc voltage (it permits examination of the graph of the movement of the carriage when adjusting the carriage drive on an oscillograph).

13.9. Preventive Control Operations

Skillful operation and high-quality technical maintenance guarantee uninterrupted operation of the storage within the limits of the service life and the reliability characteristics when designing and manufacturing the storage.

The work time per failure of the YeS-5056 storage (T_0) is no less than 1000 hours; the amount of processed information per error (T_{error}) is no less than 10^{10} bits; the average reproduction time (T_B) is no less than 0.5 hours; the service life of the storage is 12 years.

During operation of the storage it is necessary especially carefully to trace the finish and integrity of the magnetic coating of the disc and also the magnetic heads. Dust and dirt on the discs and heads are one of the principal causes of the appearance of scratches on their surfaces. In the working storage the air in the cavity of the disc package is kept clean and the dust does not accumulate. The accumulation of dust basically takes place when the storage has not been in operation for a long time. Therefore after completion of the operation of the storage it is necessary to remove the discs and put them in a container.

The disc package container must be cleaned to remove dust no less often than once a day.

The preventive control operations are performed daily for 20 minutes, every 2 weeks for an hour, monthly for 2 hours and 6 hours every 6 months. All of the operations are performed with the power off.

The daily preventive control operations are performed with the EMB module, magnetic heads and disc package. Here the EMB module is subjected to external inspection and, if necessary, dirt is removed by a cloth wet in alcohol. The MG is first inspected to determine the cause of damage. Then the carriage is manually withdrawn to the rear position, and the heads are cleaned as follows. A scale is wrapped in two layers of percale cloth, it is wet in highly pure alcohol, introduced between the heads and rubbed back and forth. Then the scale is wrapped in a dry piece of cloth and again the heads are rubbed.

The disc package is subjected to preventive maintenance after 24 hours of continuous operation observing the norms with respect to dust content in the environment. If these norms are not observed, preventive maintenance is performed on the disc package three times a day. Several layers of percale cloth are wound on a rule, and this is wet in isopropyl alcohol. The scale with the cloth is put between the discs and, by rotating the disc package manually, the surfaces of all the discs are wiped off, applying a slight amount of pressure to the disc. Then a dry cloth is used to wipe the discs again. The lint from the cloth is also removed using a scale wrapped in dry, clean technical chamois.

The disc package is replaced when strong beating occurs or in the presence of scratches and embedded particles in the magnetic layer which will not be removed by cleaning and lead to loss of recorded information.

The funnel is wiped with a cloth wet in alcohol. The cover of the disc package in the storage can be washed with water if it is not very dirty. A soft cloth, sponge or chamois is used. If scratches are detected after washing the cover, they can be removed by manual polishing using a special polishing compound.

After 2 weeks of operation of the storage unit, in addition to the above-enumerated operations, a check is made, and if necessary,the electromagnet assembly of the latch is adjusted, the condition of the storage disc package cavity filter is checked and the magnetic coating of all the disc packages used in operation during this period is cleaned.

The monthly preventive control operations include all of the above-enumerated and the following operations. External inspection of the condition of the solders, fastening of the plugs and mechanical assemblies, the presence of oxides or foreign inclusions on the surface of the floating element, magnetic head and discs is carried out. If cleaning of the disc or head package does not improve the surface condition, then they must be replaced. After replacement of a magnetic head, it is adjusted using the control disc package, and if necessary, it is also adjusted according to the instructions.

The technical condition is checked and the filters are cleaned in the following sequence: the fan grill is inspected and cleaned first by rough cleaning and then wiping all of the fan grills with a wet cloth. The fabric of the air filter for the disc package cavity is replaced, and the filter element is wiped with a cloth wet in alcohol. The filter fabric is replaced at least once a month, and the filter element, no less often than once every 2 months.

The monthly preventive maintenance work also includes lubrication of the rack, pinion and latch of the carriage drive, checking the clearances and adjusting the carriage locking mechanism, checking and cleaning the damper. All the operations are performed strictly by instructions.

The semiannual preventive control operations include all of the above-investigated operations. In addition, they include lubrication of the carriage guides, the torsion bar load pinions, checking the dynamic characteristics of the positioner, measuring the signals from the output of the preamplifier, shaper, signals of all photo read channels and the output signals of the storage. Before lubrication, the mechanical assemblies are first cleaned to remove the dust and spent lubrication using a soft, clean cloth. The lubrication points, type of oil and amount of oil are determined by the operating instructions.

14.1. General Description of the YeS-5551 Magnetic Disc and Drum Controller

The NMD and NMB storages (hereafter we shall refer to them as direct-access NPD-storages) can be serviced by the same controller. This is possible as a result of implementing the same principle of accessing them and also installation of couplers in the controllers considering the specific type of storage.

The YeS-5551 controller is designed to control the operation of the magnetic disc storages YeS-5050, YeS-5051, YeS-5052 and YeS-5056, magnetic drum storages YeS-5031, YeS-5033, YeS-5034 ans YeS-5035 and also magnetic card storage YeS-5071. The YeS-5551 controller can be connected to the SK or MK or both channels simultaneously. It can be connected to any model of the unified system of computers or to other computers under the condition of compatibility of the interface and information formats adopted on the unified system of computers.

Up to 8 storages of different types can be connected to the controller. Data exchange between the controller and the storages is realized by the series method (by bits), and between the controller and the channel, by bytes. During data exchange with the storages, the controller uses cyclic control, and when exchanging data with a channel, odd parity control. The controller provides for selecting the storage, reception and execution of central processor and channel instructions, data transmission between the storage and the channel, control of the operation of the storage, and it also generates information describing the state of the storages in detail.

The data transmission rate between the NPD storage controller is 156 kbytes/sec. Automatic and autonomous operating conditions are provided. The autnomous operating mode permits the fitness of the device and the storages connected to it to be checked out with respect to diagnostic test programs.

Structurally, the YeS-5551 is made in the form of an individual instrument bay, the frame of which is assembled from welded frames joined by screws. The frames of the main frame are made of U-section material. On the sides the bay is covered with easily removable panels, and on the front and rear double doors are provided. Both of the doors of the double doors have stops which prevent them from being opened more than 90°. On the right door there is a lock for locking the doors shut. The doors and panels are in the form of a frame made of aluminum angle and protective sheet aluminum. Inside, the doors and panels are filled with foam plastic which creates a light, strong structure.

Inside the bay three frames are provided -- one sliding and two stationary made of special aluminum section. Each frame is assigned its own index (A, B, C) which is located in the upper lefthand corner on the TEZ installation side. The frame has aix basic compartments in which panels for the TEZ and other modules of the device are installed. The rotating frames A and C are locked by locks. Two engineering panels are mounted on the frame C on the TEZ installation side. On the axis of rotation of the frame side (on the end) there are plugs for coupling the frames to each other and to other devices. In order to cool the electronic modules of the device in the lower part of each frame two fans are installed. The air goes from

the facility to the bay through a special filter, it is picked up by the fans and ejected through a lattice in the upper part of the bay.

The overall dimensions of the bay are 1200×750×1600 mm, and it weighs 500 kg. The power supply has a three-phase 380/220 volt, 50-hertz network.

The intake power is no more than 1.5 kilowatts. The delivered set includes the following: the YeS-5551 controller, spare parts and mountings, tools and one set of operating instructions and forms.

The ZUMK [microinstruction memory] is designed to store the controlling and diagnostic programs and for rapid output of microinstructions by the address formed in the UMPU [microprogram controller]. It is a transformer type ROM executed from U-type ferrite cores. The structural and operating principles of the ROM were investigated in Chapter 7. The capacity of the ZUMK is 3072 48-bit words (microinstructions). The ZUMK is implemented as 12 replaceable modules of 256 words each. The access cycle is 500 nanoseconds, and the access time, 250 nanoseconds.

14.4. Controller Circuitry

The circuitry of the YeS-5551 controller is constructed using the series 155 integrated microcircuits, specialized and several master TEZ. The latter are designed to check the special TEZ. They are all structurally executed on a glass textolite circuit board with two-sided printed circuitry and one-sided installation of radio parts. Let us consider the purpose, the circuit diagrams and operating principle of several special TEZ.

Microinstruction Read Amplifier (TEZ of the YeS-5551/0511). The amplifier is designed for amplification, amplitude and time selection of unipolar pulse signals read from the ZUMK and conversion of them to signals with parameters corresponding to the parameters of the series 155 microcircuits. The TEZ contains two identical channels. The feed voltage of the amplifier is 12.6 volts, the bias voltage is +5 volts. The input signal has positive polarity with an amplitude from 40 to 115 millivolts and duration from 160 to 200 nanoseconds. The output signal of negative polarity is as follows: lower level (logical 0) no more than 0.4 volts, upper level (logical 1) no less than 2.4 volts. The duration of the output pulse is within the limits from 140 to 270 nanoseconds, the pulse front is $t_f \leq 35$ nanoseconds, the pulse decay time $t_c \leq 15$ nanoseconds. Each channel contains a line amplifier, power amplifier, amplitude and time selectors and an inverter (Figure 14.7).

The line amplifier is executed by a differential circuit using the transistors T1 and T3 with current generator in the emitter circuit. The current generator is executed from the transistor T2. It is designed to stabilize the operation of the line amplifier. Negative feedback created by the resistor R7 stabilizes the operation of the current generator. The resistors R6, R9 jointly with the capacitor C1 form negative feedback with respect to direct current designed to stabilize the line amplifier. The power amplifier is executed from a transistor T4 by the emitter repeater circuit. It is directly connected with the output of the line amplifier and is designed to decouple it from the load.

The load of the line amplifier is an amplitude selector executed from transistors T5 and T6 by the current switch system. Its response threshold is adjusted by a variable resistor R16. The output signal from the amplitude selector is fed through a matching inverter executed from the transistor T7 to the AND-NOT element (series 155 microcircuit). The AND-NOT element realizes time selection using the "read" gating signal.

For elimination of spurious interstage couplings, filtration of the variable component by the capacitor C2 for a 12.6 volt power supply and capacitor C3 for a +5 volt bias voltage supply is used.

Control Signal Shapers TEZ YeS-7000. On the TEZ card there are eight identical shapers out of the 12 types used in the unit, a complete set of which provides for shaping pulses of different duration within the limits from 1.5 microsecond to 400 milliseconds.

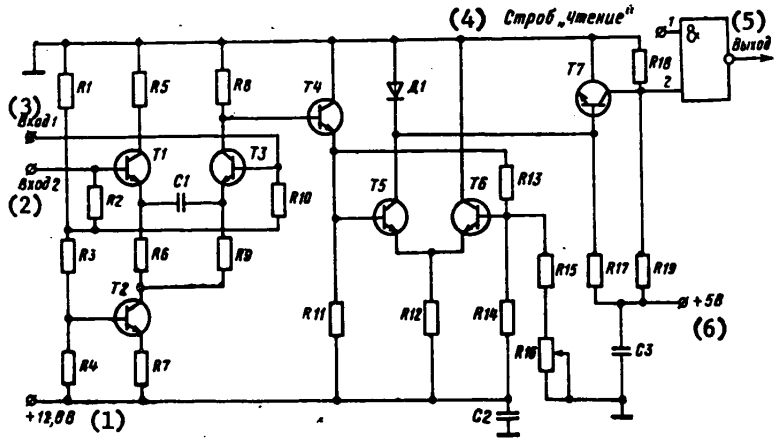

Figure 14.7. Microinstruction read amplifier

Key:
1. +12.6 volts
2. input 2
3. input 1
4. "read" gate
5. output
6. +5 volts

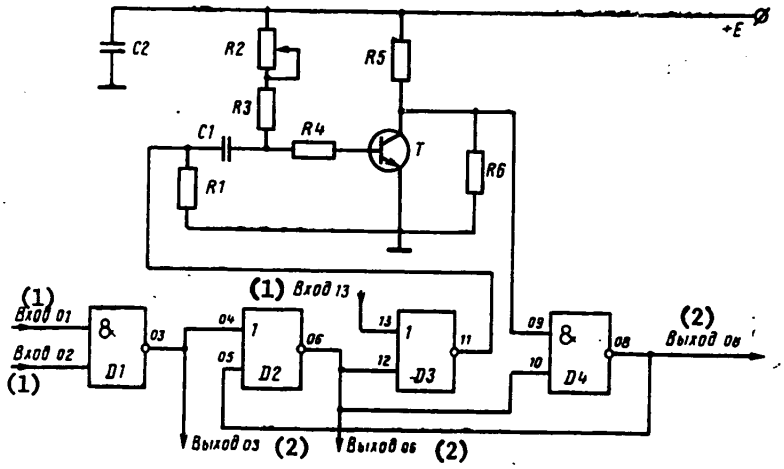

Figure 14.8. Control signal shaper

Key:
1. input
2. output

The shaper circuit (Figure 14.8) contains two AND-NOT elements (microcircuits D1, D4), two OR-NOT elements (microcircuits D2, D3) and time assigning stage executed from the transistor T, capacitor C1 and resistors R1-R6. Obtaining the pulses of given duration is possible as a result of the use in them of the capacitor C1 of defined nominal (680, 2200 and 6800 picofarads; 0.01; 0.033; 0.1; 0.33 and 0.3; 10,33 and 47 microfarads).

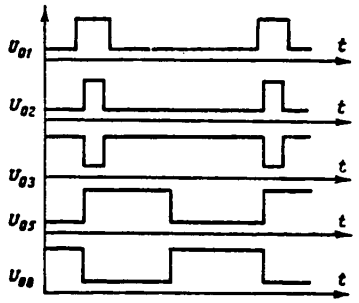

Figure 14.9. Time diagram of the operation of the shaper

The initial state of the shaper circuit is determined by the low signal level at one of the two inputs (01, 02) of the microcircuit D1 and high level at the output 08 of the microcircuit D4. High signal level at the output 08 is insured by the open transistor T, low voltage from the collector of which is fed to the input 09. The high signal level at the inputs 04 and 05 of the microcircuit D2 determines the low signal level at its output and, consequently, the high level at the output 11 of the microcircuit D3 and the low level at the input 10 of the microcircuit D4

(Figure 14.9). Here the capacitor C1 is charged. On arrival of the high signal level at the inputs 01 and 02, in the presence of a gating pulse at the input 13, the signal levels change to the opposite at the outputs 03, 06 and 11. The negative voltage gradient from the output 11 is transmitted through the capacitor C1 to the base of the transistor T and closes it. The high level from the collector of the closed transistor is fed to the input 09. As a result, the low level from the output 08 is transmitted to the input 05. This state is maintained for the pulse duration shaping time by the time-assigning stage. From the time of closure of the transistor, the capacitor C1 is discharged through the resistors R2, R3 and the emitter-collector junction of the open transistor in the microcircuit D3. As the capacitor discharges, the potential of the transistor base T increases. As soon as it becomes equal to the blocking threshold, the transistor opens, fixing the end of the shaping of the pulse. The capacitor discharge stops. The low level of the potential from the collector of the open transistor is fed to the input 09 of the microcircuit D4, at the output 08 of which the low potential level changes to high.

Before the arrival of the next pulse at the inputs 01 and 02 of the microcircuit D2, the charge of the capacitor C1 is restored. The charge of the capacitor is realized through the output impedance of the microcircuit D3 (high potential level at the output 11), the resistor R4, the base-emitter junction of the open transistor T.

The output pulse duration is adjusted by the register R2. C2 is a decoupling capacitor. The shaping of the output pulse can be forbidden by taking the gating pulse, that is, feeding a low level potential to the input 13.

Cycle Pulse Generators. For generation of pulses of cycle frequency 4 megahertz and 2.5 megahertz in the YeS-5551 unit, the TEZ YeS-5551/0501 and YeS-5551/0502 are used. Each cycle generator contains a sinusoidal voltage generator (autooscillator), the emitter repeater and shaper of the pulses (Figure 14.10). The autooscillator is assembled from the transistor T1 and is a sinusoidal voltage generator with self excitation. In order to insure high generation frequency stability, a quartz resonator S is used.

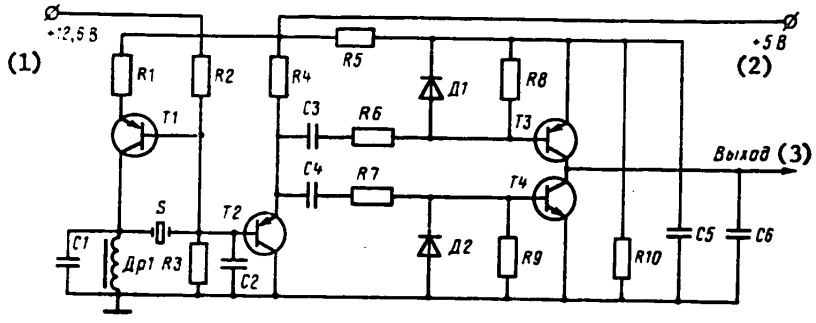

Figure 14.10. Clock

Key:
1. +12.6 volts
2. +5 volts
3. output

The sinusoidal signal from the output of the autooscillator is fed through the emitter repeater executed from the transistor T2 to the shaper. The pulse shaper is a quasiparallel connection of transistorized switches executed from transistors of different conductivity T3 and T4. This system insures additional symmetry of the shaping stage generating the output pulses with off-duty factor of 2. The resistors R6, R8, and R7, R9 form the input voltage dividers, the diodes D1 and D2 protect the base-emitter junction of the transistors T3 and T4 from breakdown, and the capacitors C3, C4 are blocking capacitors.

When a positive halfwave of sinudsoidal voltage comes from the emitter repeater, the transistor T3 is in the cutoff mode, and the transistor T4 in the saturation mode. The saturation of the transistor T4 insures a low level of output voltage. The negative halfwave T3 is saturated, and T4 is in the cutoff mode. Saturation of the transistor T3 is insured by the divider R5, R10 with decoupling capacitor C5. The capacitor C6 eliminates the voltage blips and smooths the output pulse fronts.

14.5. Characteristic Failures

In the automatic operating mode, the failure of the unit is determined by the displays of the check circuits and burning of the "halt" display on the engineering panel or "emergency" on the BUP. In the autonomous mode a failure is indicated by premature holding of the unit while executing diagnostic microprograms, by the error indicators coming on and also by the "emergency" indicator in the feed system.

The search for failures reduces to discovering the failed TEZ and replacement of it by an operating TEZ. The failure is detected on the YeS-A102 bench designed to check out logical TEZ, and the YeS-A104 designed to check out special TEZ. The test is run according to the procedure in the test table in the technical documents for each TEZ. The average time for detection and elimination of failures in the YeS-5551 is 30 minutes. Let us consider the most frequently encountered and possible failures in the device.

There is no primary network voltage in the BUP, and the "network," "power off" indicators do not light up. In this case it is necessary to check out the state of repair and reliability of the fuse contacts in the BUP and the plugs for connecting the power circuit.

In the autonomous mode when pressing on the "power on" button, the power does not come on. The "autonomous-complex" flip-flop and the power on buttons are checked by the continuity test.

The "emergency" display does not light up. This can occur in the absence of +24 volt feed in the BUP or on breaking the light feed circuit. It is necessary to check the presence of the 24-volt voltage on the rectifier. If it is absent, it is necessary to check the state of repair of the diodes by measuring the forward and return resistances. The diodes are first unsoldered. If there is a voltage of +24 volts, then the continuity test is run for the state of repair of the display light and its feed circuit.

A bit of one of the RON registers was not set or is cleared. First of all, it is necessary to check the TEZ of the given bit register. This can be done by replacing the suspected TEZ by a good one. The TEZ is checked out on the bench and the cause of the failure is eliminated. It is also necessary to check the operation of the register bits by setting and clearing them from the panel or by a test program. If the same bit continues to fail, the search for the failure proceeds outside the TEZ.

One or several bits from one modulus of the ZUMP panel with respect to all addresses is not entered in the RMK register, and from the other modules of this panel the given bit (several bits) is read correctly. The probable cause of this failure can be breaking of the U-type core in the given bit of the module. For detection of a broken core, the number of the failed module is found by the connection table, the cover of the module is removed, and the failed core is replaced.

One or several bits from all modules of one panel of the ZUMK is entered in the RMK register, and the rest of the bits are entered correctly. The cause of this situation can be failure of the read amplifier in the given bit (bits) or breaks of the circuit of the given bit from modules to read amplifiers. In this case, the TEZ YeS-5551/0511 are checked on the bench, then the module of the given ZUMK panel and then the electric circuit of the given bit are checked. In the latter case, the points of transmission of the signal are determined by the signal table, and a continuity test is run on it. After elimination of the discovered failure, the contents of the modules of the given panel are entered in the RMK in order to check their state of repair and correctness of their weaving.

All bits of a word of the ZUMK are not entered in the register RMK with respect to one or several addresses. This can be caused by breaking of the address wire in the module or failure of the diodes on the module circuit boards with respect to a given address (wire). In order to check the suspected address wire it is necessary to determine the address of the ZUMK cell, by which a microinstruction is not read. With respect to this address, the wiring on the circuit boards of the module is found in the connection table, the module is removed, and the wires are tested by the continuity test. The broken wire is replaced. During replacement it is necessary to go through the information corresponding to the given address and check its correctness on the RMK. If the address wire is in good shape, the diodes on the circuit boards of the module are checked.

If darkening of the lamella on the printed circuit board of the TEZ or contamination of the contact surfaces on the plugs is discovered when finding the failures, it is necessary to clean these surfaces with alcohol. When finding the location of the failure, monitoring and measuring instruments recommended by the operating instructions must be used. Connection of monitoring and measurement instruments to a unit operating in the automatic mode is not permitted.

18.1. Display Principles

Depending on the type of displayed information the units are divided into alphanumeric and graphical devices.

The alphanumeric units are designed to display symbolic information and various symbols, the configuration of which can be determined in advance and is characterized by a set of symbols, the number of positions and given format of the output message. Devices have been developed which display from 500 to 2000-4000 symbols on a screen; they can be used both as single panels connected directly to the computer channel and as complexes with a large number of screen panels and a group control unit. Both types and means can also be used as terminal panels or complexes in the remote data processing systems.

The graphical displays permit output of graphical information along with symbolic information: graphs, diagrams, circuits, drawings, maps, and so on. Just as the alphanumeric displays, they can be single and group. As a rule, these devices have high information capacity, but in connection with the formation of graphical display on a screen, they are significantly more complicated and more expensive than the alphanumeric units.

With respect to method of forming the image on the cathode-ray tube screen, the display units are divided into two basic classes: the raster scanning (or television) units and coordinate units. In the raster scanning devices, the display is formed by successive (with respect to rows and in side rows) assignment of brightness of the raster points, in the coordinate devices, the display is formed from segments of straight lines (or second-order curves) given by the coordinates of the beginning and end of the segment (the curvature or radii and center of a circle in the case of curves). The method of formation of the display on the screen is essentially determined by the composition of the instructions, the technical solutions, software for the unit and its operating characteristics.

With high resolution the coordinate method permits us to obtain higher quality displays formed by continuous lines. The method of raster scanning realized, as a rule by simpler circuits and structural elements, for obtaining high resolution in the graphical devices requires large volume of the on-line memory and also complication of the operations of quenching and moving the display elements. Accordingly, the raster scanning devices are primarily used in cases where high precision of the display is not required.

With respect to functional possibilities granted the user when working with the system, it is possible to isolate passive and dialog displays.

The passive displays (monitors) permit the user only to observe the image on the screen. Such displays are used, for example, in the centralized system for distribution and sale of aircraft tickets, in the information retrieval and other systems where the operator can only call for visual inspection of the required information. They are comparatively cheap, they have a simple structural design and low information capacity (250 to 500 character positions on the screen).

Significantly greater possibilities are offered the user by dialog displays which have on-line input devices and devices for altering the image on the screen: alphanumeric and functional keyboards, light pencil, coordinate pen, plotting board, and so on. The effectiveness of using such devices in the system depends both on the technical solutions when creating their circuitry and building them,

and the software developed for them. The degree of perfection of the software frequently has decisive significance. The use of dialog devices is especially effective in design automation systems, engineering research, and automated control systems.

Greater functional possibilities are granted the user by devices in which, along with displaying the information on a screen and editing means there are also online means of transferring the image to paper (the devices for obtaining a "hard copy"). During solution of the problem, the user carries on a dialog with the computer, and the final or intermediate results displayed on the screen are transferred as the user wishes to paper. An example of the most widespread structure of dialog displays is presented in Figure 18.1.

The dialog alphanumeric display is connected to the computer by means of a module for coupling to a channel. The codes of the displayed characters are stored in a buffer memory, the word address of which usually is uniquely related to the position of the character on the screen. Using a special converter, a character generator, the character code is converted to control signals, by means of which the character is formed on the screen.

The display has means of editing (controlling) the information depicted on the screen: an alphanumeric keyboard and pointer control keys. Standard characters and symbols are input using the alphanumeric keyboard. The functional keyboard permits the position of the pointer on the screen to be controlled, the image erased, operating conditions established. The operation of the device is organized by the local control unit.

The graphical dialog display is connected to a computer through a module for coupling to a channel. For regenerating the image, there is a buffer memory in which the arrangement of the information can be random, inasmuch as the image is formed by giving the coordinates of the points of the image elements.

Feeding control signals to the beam deflection system causes displacement of the beam on the display screen. The conversion of the digital code to an analog signal required to do this is provided by a converter, a symbol generator and sectional generator.

The dialog between the operator and the computer is carried on by means of alphanumeric and functional keyboards and a light pencil.

The standard display contains a cathode-ray tube (ELT), a character or vector generator which affects the deflecting systems of the cathode-ray tube and input media, that is, a keyboard or a light pencil.

The characters on the screen of the cathode-ray tube are generated by various methods. As a rule, parametric methods are used which are based on controlling the position of the electron beam on the cathode-ray tube screen. Here the light (displayed) point is shifted on the screen under the effect of two analogs of the signals X(t) and Y(t). The third signal Z(t) is used to control the brightness of the depicted point (modulation). The trajectory of the displayed point with corresponding values of X, Y, Z, which are given functions of a common parameter t, is also a reproducible character.

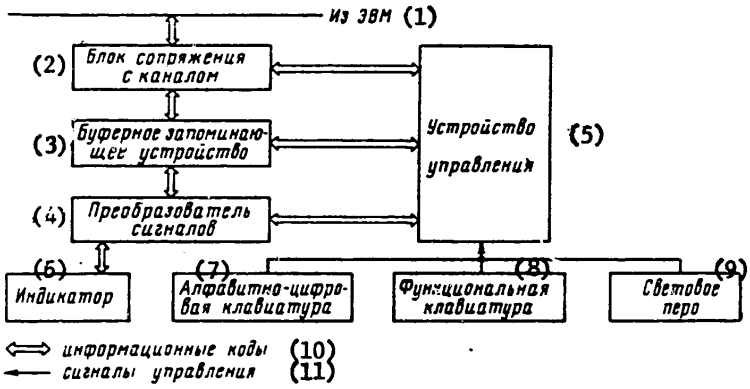

Figure 18.1 Structure of a dialog unit

Key:

1. from the computer
2. Module for coupling to the channel
3. Buffer memory
4. Signal converter
5. Controller
6. Display
7. Alphanumeric keyboard
8. Functional keyboard
9. Light pencil
10. Information codes
11. Control signals

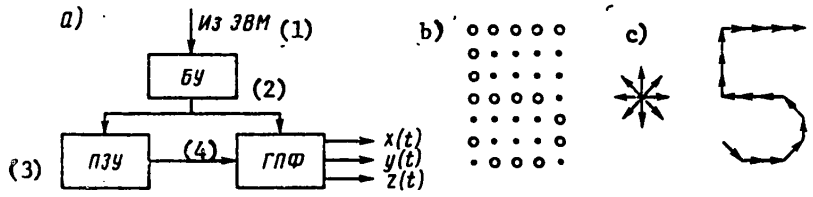

Figure 18.2. Character generator:
a -- structural diagram and principles of formation; b and c -- principles of formation of a character by a matrix of points and vector increments

Key:

1. from the computer
2. BU
3. PZU
4. GPF

The character generator based on the parametric method can be provisionally represented as consisting of three functional parts: the parametric function generator (GPF) X(t), Y(t), Z(t), the control module (BU) and read-only memory (ROM) (Figure 18.2, a).

The parametric function generator must have $2^{N_{char}}$ operating modes with respect to number of reproducible characters (N_{char} is the number of binary bits in the character code). As is known, for establishing the required function generator mode it is necessary to input some information in digital form to it. The volume of this information significantly exceeds the volume of information used in the computer for coding the characters. This explains the presence of an ROM in the character generator. The control word containing from 64 to 128 and more binary bits can be stored in one ROM cell. Rigid requirements are imposed on the ROM with respect to data read time, inasmuch as this time directly determines the total time spent on generating one character.

The operating principle of the parametric function generator essentially depends on the adopted method of drawing the character. The highest quality image is obtained on moving the image point in the X, Y plane with constant linear velocity. In this case the character is made up of standard fragments which are in the general case arcs of some high-order curves. For practice it is possible to limit ourselves to segments of straight lines, arcs of circles and ellipses. Here the configuration of the character can be approximated to printed symbols which are customary for man. The high image quality, as a rule, requires large volume of ROM. In this respect the methods based on using masks which are applied to a constant base image are more economical. The matrix of points 5×7 or 7×9 (Figure 18.2, b) can be such an image. Here the volume of information which must be stored in the ROM is equal to the number of base image elements, and the display time for all symbols for all characters is the same.

The image of a character is higher in quality, the larger the number of elements making it up. However, with an increase in the number of elements, the image forming time increases, which, in turn, leads to a decrease in the number of characters simultaneously output on the screen.

The method based on forming the symbol by growing increments which are segments of equal length of one of eight possible directions (Figure 18.2, c) is of practical interest. Although stylized characters are obtained in this case, their configuration can be approximated quite well to printed type. In addition, the volume of the ROM is found to be comparatively small inasmuch as for one character it is necessary to store a word 40 to 80 bits long. This method is implemented on the alphanumeric information display YeS-7906.

Graphs of the type of $y=f_i(x)$ can be represented on the cathode-ray tube screen by lighting on the individual points or drawing continuous lines.

When mapping graphs by lighting points in order to obtain continuous lines, it is necessary to locate adjacent points on the line with step size corresponding to the resolution of the cathode-ray tube so that the line will be visually perceived as continuous. For a limited frame display time and speeds of the buffered memory and deflecting system of the display which are attainable in practice, the method of lighting the points permits us to obtain only comparatively simple images. Therefore all the devices which depict graphical information have a specialized calculation module which interpolates (defines the coordinates of intermediate points of the lines) -- a vector generator.

18.2. Composition of the Alphanumeric Information Display YeS-7906

This unit is designed for input-output and processing of alphanumeric information when working in the unified system of computers. It can be connected to a selector channel (SS) or multiplex channel (MK) and operate in the multiplex or exclusive mode. The complex can be used as a request or dialog system in automated control systems, as an autonomous subscriber unit for data preparation and processing, to check out and correct computer programs, to correct the contents of the information libraries, and so on.

Its composition (Figure 18.3) includes the group control unit YeS-7566, up to 16 YeS-7066 remote screens and the "Konsul 260.1" typewriter (PM) (the YeS-7172 unit). The display screens are connected to the controller by four lines. On connection of from two to ten remote display screens in series to one line, the last screen is installed at a distance of no more than 300 meters from the YeS-7566 unit. If one remote screen is connected to a line, the maximum distance at which it is installed can be 600 meters. The "Konsul 260.1" typewriter is connected to the YeS-7566 unit by a special lead and can be removed up to 2 meters from it. The YeS-7566 unit is connected to channels of the unified system of computers by a standard interface.

The asynchronous-action YeS-7566 can be used in a group of MK units with any priority. It consists of a module for coupling to a channel, control module, print module, buffer memory modules, engineer panel, operator panel and autonomous electric power supply system (three-phase 380/220 volt ac network).

The YeS-7566 has two buffered memory modules to store the information of the remote panels and typewriter. The buffer memory module of the remote panels, which is an on-line magnetic core memory, has access time of 2 microseconds, word length of 9 binary bits (7 information bits, 1 check bit, 1 bit for storing tags), a capacity of 4096 bytes. The tyepwriter buffer memory module is executed from registers in the integrated execution and has an operating frequency of 500 kilohertz, a word length of 9 binary bits (7 information bits, 2 for storing read and write tags), and a capacity of 1024 bits.

The remote YeS-7066 screens are designed for mapping alphanumeric information on a cathode-ray tube screen (43LM1I), for assembling and editing it by keyboard.

The display has the following parameters: screen operating field size 280×160 mm, color of screen glow green, average duration of screen after glow 10^{-2} second, maximum number of characters reproduced on the screen 960 (determined by the number of connected panels), number of lines on the screen 12 or 5, number of characters per line 80 or 40, size of character 3×5×2.5 mm (with a 12×80 format) and 7×5 mm (with 6×40 format), the information regeneration frequency on the screen is 50 hertz, the number of types of displayed characters 96, method of displaying the characters, vector with the beam running over the outline of the character.

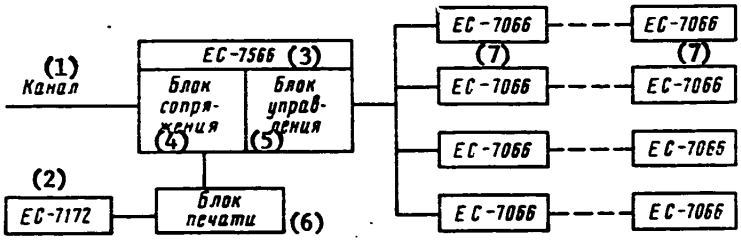

Figure 18.3. Composition of the YeS-7906 complex

Key:
1. Channel
2. YeS-7172
3. YeS-7566
4. Coupling module
5. Control module
6. Print module
7. YeS-7066

The keyboard is equipped with two registers, 22 control keys and 49 alphanumeric keys. The control keys for the pointer and the informationshift conditions operate in the automatic repetition mode if they are held down. The information is picked up from each alphanumeric key independently of whether the rest of the keys are pressed or not. All of the keys are executed from magnetically controlled contacts.

The "Konsul 260.1" typewriter is used only as a print mechanism (the keyboard of the typewriter is not used).

The YeS-7906 (Figure 18.4) includes the following:

A module for coupling the complex to the channel (BS) designed for receiving information, monitoring the information and transmitting requests to the computer; the buffer memory module (BBP) designed to store the displayed information of all of the remote panels; control module (BU) common to all of the remote panels used to generate synchronizing pulses for each of the control units of the remote panels (UU_1 to UU_n), for entering information in the buffer memory, decoding of this information, reading information out of the buffer memory and control of the information transmission process to the remote panels, BP and BS; the print module (BP) used to obtain a copy of the information coming from the channel or any remote panel; the control units for the remote panels (UU_1 to UU_n);

The character generators (GZ_1 to GZ_n) designed for conversion and character generation of informaton on the cathode-ray tubes of the remote panel; remote panel displays (I_1 to I_n).

The remote panel YeS-7066 (Figure 18.5) includes the cathode-ray tube, video amplifier, focusing and deflecting systems, coordinate scanning units, character scanning units, character generator, unit for synchronizing and generating the display address, receiving register, keyboard register, amplifier-receivers, amplifier-transmitters, power pack and keyboard.

By using the cathode-ray tube, the information is displayed on the screen in the form of characters lighted against a dark background. The video amplifier excites a modulating electrode of the cathode-ray tube and amplifies the beam illuminating signals.

The focusing and deflecting systems control the electron beam of the cathode-ray tube. The coordinate deflecting system deflects the beam horizontally and vertically in the field of the entire screen. The character deflecting system deflects the beam in the symbol location field and creates a magnetic field compensating the line scanning field of the screen raster during the character display time.

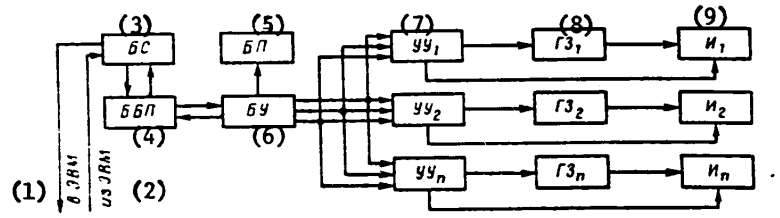

Figure 18.4. Structure of the YeS-7906

Key:

1. to the computer
2. from the computer
3. BS
4. BBP
5. BP
6. BU
7. UU ...
8. GZ ...
9. I ...

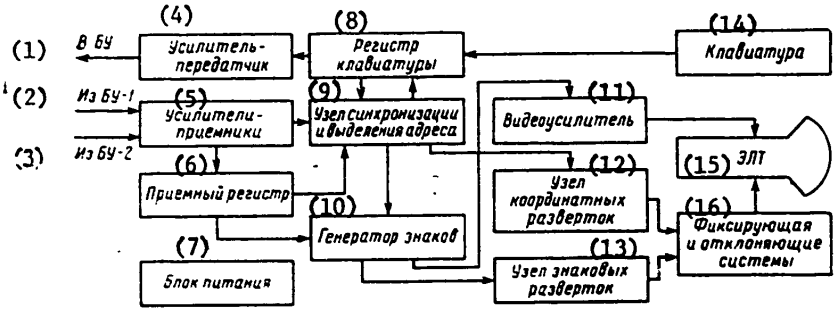

Figure 18.5. Structure of a remote YeS-7066 display

Key:

1. to the BU
2. from the BU-1
3. from the BU-2
4. Amplifier-transmitter
5. Amplifier-receiver
6. Receiving register
7. Power pack
8. Keyboard register
9. Unit for synchronizing and generating the address
10. Character generator
11. Video amplifier
12. Coordinate scanning unit
13. Character scanning unit
14. Keyboard
15. Cathode-ray tube
16. Locking and deflecting systems

The coordinate scanning unit is designed to receive signals that control the duration of the beam path of the cathode-ray tube, formation of currents exciting the coordinate deflecting system.

The character scanning unit forms voltages and currents of triangular-trapezoidal shape to excite the character deflecting system.

The character generator converts information from the internal code of the YeS-7906 to a 32-cycle sequence of 5-bit signals controlling the character scanning unit and the video amplifier.

The unit for synchronizing and generating the display address generates signals that control the operation of the YeS-7066 synchronously with operation of the YeS-7566, generation of the display number and image format.

The receiving register is used for reception of information from the YeS-7566 in series code and output of it to the display in parallel code. Using the keyboard register, information is received from the keyboard in parallel code and it is output synchronized in series code to the YeS-7566.

The amplifier-receivers and amplifier-transmitters receive, amplify and transmit signals along the communications cables of the YeS-7066 and YeS-7566.

By using the keyboard, the information and control signals are put together which define the code of the corresponding characters or instructions.

Synchronous operation of all of the units is insured by a single synchronization circuit placed in the YeS-7566. It includes the pulse generator, the frequency synchronization unit, and the synchronization register.

The generator with quartz stabilization insures continuous generation of pulses with repetition frequency of 4040 kilohertz. The frequency synchronization unit is a system by means of which the period of the frame changing frequency of the image is equated to the feed network frequency period. The synchronization register consisting of 18 counting triggers provides for generation of the operating frequency of the complex of 2020 kilohertz, cycle signals, the signals at the beginning and end of lines and image frames.

On the screens of the YeS-7066 units, the characters are formed under the effect of magnetic fields of special intensity and form on the electron beam. As a result of the effect on these special fields of the magnetic scattering fields of the power feed network, the power elements of the units (transformers, filter chokes) and also a number of standing units, the image is distorted, it becomes unstable and shifts (rocks) vertically and horizontally with periodicity equal to the scanning frequency and feed network frequency difference. In order to eliminate this effect, the inertial method of synchronizing the scanning frequency with the power feed network frequency is used in the YeS-7906, consisting in equalizing the periods of the network frequencies and the frequency of changing the image frames by discrete variation of the duration of the line period.

The starting and synchronizing of the operation of all the devices of the YeS-7906 complex are realized using the synchronization register, which is a frequency divider of the master, high-frequency quartz-stabilized oscillator.

The frequency of the master oscillator is selected by the synchronization register as a function of the frequency of the ac network. Inasmuch as the network frequency can fluctuate from 49 to 51 hertz, the frame changing period varies from 19608 to 20408 microseconds.

For servicing one remote panel, that is, for reading information from memory, processing and transmitting it, 4.5 microseconds are sufficient. However, since the time spent drawing the symbol on the screen is about 16 microseconds, it is possible to access the same remote panel no more often than every 4 cycles (18 microseconds). Therefore simultaneous servicing of four remote panels with 12×80 image format is possible.

With 12×40 image formats the number of panels must be doubled, inasmuch as there are 40 characters per line. In this case the information of the buffer memory corresponding to even positions of the basic format line of 80 characters goes to certain remote panels, and the information corresponding to odd positions, to others. For formats containing 6 lines, the information of the buffer memory corresponding to even and odd lines of basic format goes to different panels.

It must be noted that the total time for servicing all of the panels is constant inasmuch as the total volume of the buffer memory and the information repetition frequency on the screens of the panels are constant.

18.3. YeS-7064 Graphical Information Display

The YeS-7064 display consists of a screen and controller located in the standard bay of the unified system of computers.

The graphical data are depicted on the screen of the unit in the form of a set of points and vectors. Simultaneously with them alphanumeric information and other special characters can be output to the screen. Any nonstandard symbol can be constructed graphically -- from segments of vectors.

The image is formed on the screen under the control of the program entered in the buffer memory from the computer to which the unit is connected through a standard coupling channel of the unified system of computers.

Any output information is addressed in the coordinate system having 1024 points each with respect to the X and Y axes. Thus, any point has its own address. The distance between any two adjacent points (both along the X-axis and along the Y-axis) on the screen is defined as a raster unit. For output of graphical information (vectors) the bytes of data determine the coordinate (final point) to which the electron beam must be set. The beam always moves from the preceding address point to the next addressed point. The vectors can have any length and be depicted at any angle within the limits of the working field of the screen. In the initial

position, the beam is set to the center of the screen by the attribute "beginning of frame copying." If the beam is "switched on" during the displacement time, the vector is reproduced between the end points; if the beam is "switched on" after displacement, the point is reproduced.

Inasmuch as the regeneration process is synchronized by the feed network frequency, the image on the screen is formed in no more than 20 milliseconds. Regeneration is realized automatically under the control of the internal program of the unit.

In order to obtain a copy of the image, a microfilming device can be used in which the screen of the special cathode-ray tube has a coordinate matrix with the points 4096×4096. In order to use the same program during microfilming and output of information, the coding of the images in the program is done within the limits of the same coordinate matrix. On output of information in the YeS-7064 unit, two low-order bits of the coordinate code are dropped, for the coordinate matrix of the device is 1024×1024 points.

The graphical image on the screen is formed from segments of straight lines and points, the coordinates of which are given in the mode of absolute values by 4 bytes or in the increment mode with respect to the preceding position of the cathode-ray tube beam by 2 bytes. The speed of the beam in drawing the vector is 3 to 5 mm/microsecond, and the size of a raster unit is 0.25 mm.

The number of vectors output without flickering is as follows: 3300 short ones (to 64 raster units), 950 medium ones (to 512 raster units), and 400 long ones (to 1024 raster units).

The characters are formed on the screen by the character generator. The characters are formed from beams or segments. The number of characters of basic size in a line is 74, large size characters 49, the number of lines for basic size characters is 52, and for large characters 35. The maximum number of characters on the screen without flickering is 2100; with flickering it is 3848 (the basic size characters) and 1715 (large size characters).

The control of the unit and information exchange with the computer are realized by an operator using an alphanumeric keyboard, functional keyboard having 32 keys and replaceable covers (maximum number 256), a light pencil with flexible light guide, a cooordinate mark control knob, display adjustment elements and operator panel.

The YeS-7064 consists of a bay and a desk. In the bay are the basic control system assemblies: buffer memory, module for connecting to the channel, control module, vector and character generators. On the desk is a display with cathode-ray tube and light pencil and also freely moving alphanumeric and functional keyboards and rigidly fastened operator panel.

In the structural diagram of the YeS-7064 (Figure 18.6) it is possible to isolate three functional parts: the controller, the input unit and the image shaping unit. The module for connecting to the channel, the buffer memory of the BZU and the feed control module are independent.

In the module for coupling to the channel (BSK), all operations are realized for connecting the unit to the computer, channel instructions are executed, and the basic state and sense bytes are also formed.

As a rule, the data bytes go to the BZU through the BSK; in this case the BSK controls the BZU. For example, the program is transmitted from the central processor to the buffer memory of the unit just as data transmission.

The buffer memory contains two modules just as the YeS-7906. The capacity of each module is 4096 bytes, and the access time is 2 microseconds.

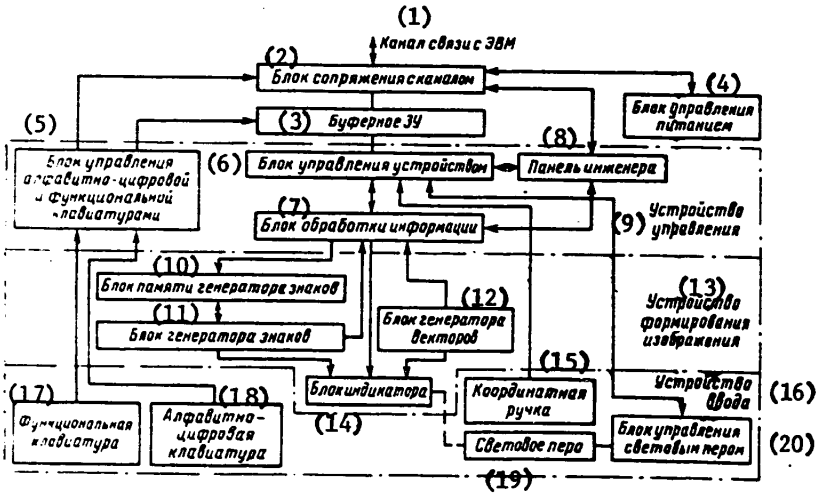

Figure 18.6. Structure of the YeS-7064

Key:

1. Channel for communication with the computer
2. Channel coupler
3. Buffer memory
4. Feed control unit
5. Alphanumeric and functional keyboard control unit
6. Control module of the unit
7. Information processing module
8. Engineer panel
9. Controller
10. Character generator memory module
11. Character generator module
12. Vector generator module
13. Image shaper
14. Display module
15. Coordinate knob
16. Input unit
17. Functional keyboard
18. Alphanumeric keyboard
19. Light pencil
20. Light pencil control module

The buffer memory is designed for storing an image file, copying (regenerating) the image, and it permits editing and compiling of the text independently of the central processor and also the performance of a number of graphical operations.

The feed control unit (BUP) is designed to control switching the feed system on and off (both in the autonomous mode and in the remote mode), signalling in case of the emergency modes in the standardized feed units, switching the preventive control mode on and off.

The control unit includes the control module of the unit, the control module of the alphanumeric and functional keyboards, the information processing unit and the engineer panel.

The controller module (BUU) realizes connection of all the basic modules and generates a set of control signals. In the module a parity analysis made of the information read out of the BZU, the instructions (orders) are separated from the data, the operating conditions of the unit are generated, and in special cases signals are generated for the BSK in order to call the channel.

The alphanumeric and functional keyboard module realizes coupling of these keyboards to the memories and the BUU. In the keyboard control unit, on pressing a key, a single signal is generated, the pointer control is realized, the code of the pressed key of the functional keyboard is stored, and the corresponding signals are formed on pressing the keys of the alphanumeric keyboard.

In the data processing module (BOI), which is a supplement to the BUU, information is prepared for the vector and character generators and synchronization of their operation. In the character mode the module automatically forms the distance between the characters and the lines.

The engineer panel (PI) is a device by means of which adjustment and preventive operations of the unit are carried out, various operating modes are assigned (single or multiple modes, read or write, and so on). Using the panel, manual input of the program to the MOZU [magnetic core storage] is possible. The light signal system of the basic assemblies of the various modules is coupled out to the engineer panel. It includes the drive systems (amplifiers for the display tubes and signal shapers for the knobs and flip-flops.

The input device contains the following: alphanumeric and functional keyboards, the light pencil, the light pencil control module and the coordinate knob.

On the functional keyboard (FK) there are two keys with light display and eight cover code keys. The combination of the cover code with the key code determines the function of the given keys. The function of the key, that is, the subroutine called by it, is determined by the corresponding inscription on the cover. For example, if cover No 19 is set which generates the code 0001 0011 and key No 11 is pushed (the binary code 001011), then the key function is determined by the code 001011 0001 0011. In all there can be 256 covers; therefore when using the FK it is possible to call for the execution of $256 \cdot 32 = 8192$ subroutines in the computer.

The light pencil is connected through a light guide to the light pencil control module (BUSP) consisting of a photomultiplier with amplifier-shaper, high voltage unit for feeding the photomultiplier and amplifier-shaper power pack. There is a pointer control knob with switches.

The image shaping unit contains vector and character generators, the character generator memory module and display.

The character generator module (BGZN) converts the sequence of digital control signals to a sequence of analog signals required to draw the character on the screen. The standard set of characters which can be reproduced consists of 88 alphabetic, numerical and special characters. Either of two sizes of characters -- basic or large (1.5 times larger than basic) -- is selected during programming.

The memory module of the character generator is an ROM [read-only memory] designed to store information about the character configuration. By the character code and by request from the character generator, the module generates a defined set of control signals which then go to the character generator.

The vector generator module is designed to shape analog signals providing for displacement of the beam on the screen of the cathode-ray tube to a given point along a given trajectory. A 20-bit code of the coordinate of a finite point is fed to the module input to which the beam is shifted, and a 20-bit coordinate increment code with respect to the preceding position of the beam. The module insures constant speed of the beam to the given point in the vector mode.

The display is the output module of the entire unit, and through it a direct coupling is realized between the operator and the computer. The module includes a cathode-ray tube (ELT) with a locking-deflecting system, coordinate and character deflection amplifiers, high-voltage and special power supplies, beam brightness control circuit (modulator).

The commands of the unit can be provisionally divided into three groups:

Graphical commands (Figure 18.7) establishing the operating mode of the display (after them come the data indicating the character code or the coordinate to which the cathode-ray tube beam must be shifted); control commands for the order of execution of the program written in the buffer memory; commands establishing the light pencil modes. They are initialized by the command "beginning of copying of a frame."

The light pencil is designed for input and correctionof graphical data.

It is a cylinder 15 mm in diameter and 200 mm long with conical tip. It consists of a housing in which the moving objective and magnetically controlled contact are placed. In the housing a flexible light guide made of fiberglass is installed 1 to 1.5 meters long and 2 to 3 mm in diameter; the light guide is mounted by the other end in a light proof housing with photomultiplier (FEU). For protection against damage the light guide is placed in a metal hose.

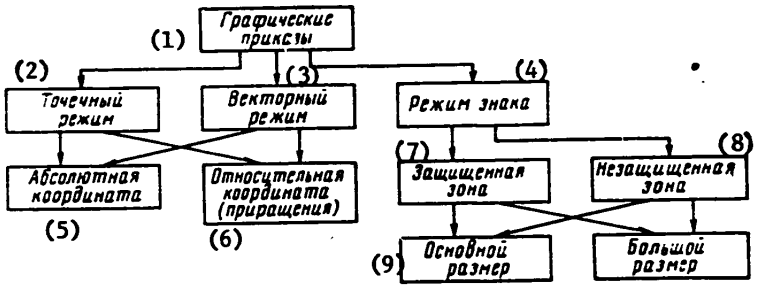

Figure 18.7. Classification of plotter commands

Key:

1. Graphical commands
2. Point mode
3. Vector mode
4. Character mode
5. Absolute coordinate
6. Relative coordinate (increments)
7. Protected zone
8. Unprotected zone
9. Basic size

When the light pencil is pointed at an element of the image on the cathode-ray tube screen, the light flux emitted by the screen phosphor when it is excited by the electron beam goes through the light guide to the photomultiplier in which it is converted to an electric signal which goes to the electronic amplifier and then to the control unit. Here, depending on the external illumination of the screen, the image brightness on the cathode-ray tube can vary by several tens of times. The field of view of the light pencil is 3-4 mm.

Pressing by the point of the light pencil on the surface of the screen, the operator shifts the objective inside the housing. Here the permanent magnet connected to the objective which closes the magnetically controlled contact is shifted. Thus, the operator communicates to the computer about the image element which he is generating by the light pencil.

In order that the operator be able to determine at what image element to point the light pencil, the device has a circuit which provides for flickering of the given element with a frequency of 12.5 hertz. The address of the selected element is stored in the buffer address register, and its coordinate is stored in the mark registers. In the next regeneration cycle the stored address and coordinate are compared with the current address of the MOZU and current coordinate. On output of a mark to the screen, the flickering takes place only on comparison of the addresses, and the coordinates are not stored. On coincidence of the addresses and the coordinates, the beam quenching signal is generated. The flicker trigger is switched off.

Thus, the element, the address and coordinate (or only address) of which are stored, that is, at which the light pencil is aimed, is output to the screen with quenched beam for two regeneration cycles out of four. On the third cycle the flicker trigger is switched off, and on the fourth cycle, the image element is secondarily detected and the address and coordinates are stored.

In order that detection be able to be accomplished in any regeneration cycle independently of flicker, on response of the contact in the light pencil, the single pass circuit responds generating the 20-millisecond pulse which determines the regeneration cycle in which detection of the image element takes place and this is reported to the computer.

20.3. Methods and Software for Checkout and Technical Diagnostics

Special reliability requirements are imposed on any model of the unified system of computers in the real-time process control systems and in the collective-use systems. The operating reliability of the models is insured by a developed monitoring and diagnostic system containing software and hardware which operate both in the basic (working) mode and in the technical maintenance mode.

The hardware realizes operative monitoring of the fitness of the computer, detects errors, and locates the failures. In the operating mode the hardware operates under the control of the operating systems, including the programs for processing error signals. A set of technical maintenance programs KPTO is used in the technical maintenance mode. This set of programs presupposes the use of control and service programs, monitoring and diagnostic hardware.

The monitoring and diagnostic module is used to control the procedures of the "accounting" type by the DIAGNOSTIC command, tests to locate failures TLN, and check out of the on-line memory. This module contains registers, counters and logical control circuits. The registers are used to receive analyzed information, write it in memory, and provide for the preservation of instructions on all levels. The counters are used to count the number of errors, synchronization and monitoring cycles.

The hardware monitoring of the processor provides for continuous parity checking of the data combined with a number of special means of continuous checking of individual assemblies and modules. The operation of any assembly or module of the processors is checked during its operating process; therefore it has no influence on the output capacity of the computer.

The parity check when transmitting information is realized by special standard circuits that check the transmission, storage and basic conversion of the data. For any data conversion influencing parity, preliminary parity checking, conversion and formation of new check bits for the converted information are carried out. The addition of one check bit is provided for each byte of information: 1 corresponds to an even number of ones in the byte, and 0 corresponds to an odd number of ones in the byte. This representation of the check bit permits any number of odd errors to be checked for each byte and also discovery of complete loss of information. Direct parity checking, that is, comparison of the parity of the checked register with its checked bits is done only in the basic register; the rest are checked at the time of transmission of their contents to the checked registers.

Parity checking of the processor memory module takes place in the modules themselves. On detecting an error in the access address to the on-line memory, the contents of the selected cell are regenerated in order to prevent distortion of the information.

The checking of information parity conversion in the processor is done in the counting operations in the binary counters of all modules, the operations of the arithmetic-logic unit, operations of the decimal arithmetic module, operand address modification (calculation) module, during operation of certain information conversion circuits, information decoding in the decombiners of all processor modules.

In addition, operations are checked in the processor, the execution of time of which exceeds 160 milliseconds. This check is made by the counters of the multi-system timer fixing the beginning and end of performance of the operations.

For processor diagnostics in some models, for example, the YeS-1050, a test mode is provided which is analogous to the stock testing of a processor with failure location.

Each test has a fixed format (112 bytes), the entire set of tests is on one magnetic tape. The control of the execution of the tests is realized by the monitoring and diagnostic module. For this purpose, two buffers are reserved in the ready-access memory: the first with the address 8000 to 806F, and the second with address of 8080 to 80 EF.

20.4. Technical Maintenance Software

Adjustment, verification and diagnostic tests which make up part of the technical maintenance software KPTO which includes also a number of control and service programs are used as the monitoring and diagnostic software.

The adjustment tests are designed for correctness of operation of the minutes and modules of the computer, the verification tests are designed for periodic verification of the operation of the units and the computer as a whole during the normal operation process. When detecting a failure, the diagnostic tests are used to locate it.

With respect to organization, the tests are divided into basic tests performed under the control of the test monitor DMES and verification tests of the peripheral devices operating under the control of the operating system of the unified system.

The basic test is a set of adjustment tests, and it is designed for preliminary adjustment and checking of the basic equipment of the processor, the on-line memory, the selector and multiplex channels, the magnetic tape storage and typewriter. Successful performance of it in the future insures loading and operation of the test monitor. Further adjustment and checking of the computer are carried out using the test sections.

The test monitor DMES is a control program designed for loading and controlling the execution of the test section programs.

The test section consists of the heading and a variable number of examples. The test example forms a logically independent module and contains a prefix and the check section itself. The titles of the section and the prefix of the example are regions of interaction of the section and the test example of the test monitor respectively.

The test monitor performs the following functions: it is tuned to the possibility and size of memory of the specific computer, it controls the readiness of the input-output devices, it decodes the commands given by the operator and performs the corresponding operations, it performs preliminary processing of interrupts, it determines the test sequence for the units, it loads the test sections into the ready-access memory and also performs a number of functions which are common to all of the test sections, for example, printing out messages, code conversion, and so on.

For operation of the test monitor and test sections, an on-line memory of no less than 16K is needed and also an operator command input unit (typewriter), a message output unit (typewriter or alphanumeric printer), a unit for loading the test monitor and test sections, that is, magnetic tape storage, magnetic disc storage or a punch card input unit.

For checking the computer using test sections when performing the standard procedure of initial loading of the on-line memory, the test monitor is loaded. Then by instruction from the operator, the test section is input to the region of the on-line memory following the memory section with the test monitor and the test section is executed. The memory occupied by the test section usually amounts to less than 4K. After execution of one section, the next is loaded and executed until all of the sections have been executed which were indicated in the operator's instruction. Then the operator calls the next group of test sections. The total size of the KPTO programs is about 300K.

The communications between the operator and the test monitor are by commands given from the typewriter or entered directly in a defined region of the test monitor (the operator panel buffer).

The test monitor is connected to the test section by its initial region, which is the section heading. The test section can access the monitor on the command SVC (CALL SUPERVISOR) to call the standard service programs.

The initial step in the operation of the test monitor is adjustment of it depending on the computer characteristics. For this adjustment operation, the data on the system configuration of the specific computer punched on punch cards and placed in the subject block of the test monitor or written on magnetic carrier in the test monitor program by means of service programs are used. By these data the test monitor forms the reference table of test sections (SRT), the channel table (CMT), the test monitor input-output unit definition table (DMIO) and the unit definition table (UDT).

The SRT contains information about the possibilities of the processor, the volume of the on-line memory, the program switches of the test monitor used to control

its operating modes, the address of the CMT, DMIO and UDT tables, the waiting factor for a ten-second delay, the panel buffer of the operator and certain other data.

The test section can access this table only directly. If necessary it accesses other tables.

The CMT contains information about the presence of channels and their peculiarities.

The UDT describes the units making up the specific computer, their addresses and characteristics. After loading the test section the test monitor transmits words from the UDT table describing the units required for operation of the given test section to it if necessary.

The DMIO includes three words describing the test monitor loader and input-output unit. Each word characterizes the type of unit, the instruction code which is used during operation of this unit (the instruction code is entered in the USK) and also its address. The input-output units are assigned in the initialization program and can be altered by operator command.

The operating system OS of the unified system of computers YeS-1050 provides for the presence of a control program which permits testing of the peripheral devices in parallel with solving the user problems in the multiprogram mode. The tested units are not assigned for the operating system of the unified system. As a rule, this test mode is possible in the presence of several units of the same type in the computer. Each unit is provided with a set of test sections which differ from the monitor test sections.

20.5. Preventive Maintenance

Checking Operating Fitness Using Tests. Technical maintenance software (KPTO) is available for checking the fitness and locating failures. The KPTO includes complex tests for checking the model and tests for checking individual units.

For storing the test the following are used: magnetic tapes on which the service and verification test programs are written; decks of standard punch cards used for data input in the multiplex channel YeS-4012 test, the test for the punch card input unit YeS-6012 (or YeS-6013) and the test for joint operation of channels; punch tapes used in the test for the YeS-6022 unit and the test for joint operation of the channel; control tapes of the alphanumeric printer for testing the YeS-7032; punch cards with test programs duplicating the magnetic carrier information.

The KPTO consists of the following programs: control (test monitor), basic test for complex checkout of the model, test sections of individual units and the test tape service program. The last program is primarily used for making and checking working copies of the machine carrier and also copies of the machine carrier prepared for the user.

The daily adjustment operations consist in single execution of the base test and test sections jointly with the operating system. Only three magnetic tape storages (YeS-5010 or YeS-5017) and three magnetic storages (YeS-5056 or YeS-5050) are checked. During the next daily adjustment operations, the other three storages are checked.

The order of execution of the test programs written on magnetic tape is indicated in the KPTO operating manual.

During the biweekly adjustment operations, the basic test of the test sections of all units is executed once, all of the magnetic tape and magnetic disc storages are checked out. The service and verification tests on the magnetic tape are used.

During the monthly adjustment operations, test programs are run for all the units (including for all the storages) just as for the biweekly operations. The programs are run three times: with rated voltage of the electric power supply and with 5% deviations from the rated value in both directions.

During the semiannual adjustment operations, test programs are executed for all units (including for all storages) just as for the biweekly adjustment operations. The programs are run four times: for rated values of the frequency and voltage, with deviation of the voltage $\pm$5% and at preventive frequency.

After output of an error message during operation of the test sections, the service personnel refer to the operating manuals for the corresponding test sections, the initial codes (print-outs in assembler language) of the programs for more detailed analysis of the check conditions, and they make the corresponding decision (conversion to the autonomous mode of the test and location of failures, looping of the check without printing out an error message and investigation by oscillograph, performance of various types of program halts using the control panel and other action). In the case of an unstable error it is possible to try to make it stable by varying the voltage or frequency of power supply.

Punch cards are used as the machine carrier if the failure does not permit working with magnetic tape. In this case the test monitor is loaded from the punch cards, and the punch card version of the test sections of the process, the selector channel and magnetic tape is used.

If the test monitor cannot operate with the typewriter or the ATsPU as a result of failure (although the basic typewriter test is satisfied), input of assignments to perform the test sections comes from the computer control panel, and the test sections of the multiplex channel and typewriter are executed. Using the control switches of the test monitor, printout of messages is inhibited and an error halt is permitted (or execution of the example causing the error is looped).

Checking of Individual Units. The checking of the units making up the model can be done in the autonomous and complex modes.

The multiplex channel YeS-4012 is checked as part of the model in the complex mode (the "autonomous/system" switch on the monitor-adjustment panel of the unit is in the "system" position) using the test sections of the multiplex channel. Autonmous checking of the YeS-4012 is done using autonomous means.

For conversion of the YeS-4012 from the complex mode to autonomous it is necessary to open the doors of the first bay, frame A and switch to the "autonomous/system" switch on the monitoring and adjustment panel to the "autonomous" position.

For conversion of the unit from autonomous mode to complex, the "autonomous/system" switch is set to the "system" position. In the complex mode the frame A and the doors of the first bay of the unit must be closed.

The sectional channel YeS-4035 is checked in the complex mode using the selector channel test section. The switching is done using the "autonomous/system" switch on the monitoring and adjustment panel of the channel.

The switching can be done only on arrival of a signal permitting switching from the processor, which is excited if the processor is in the waiting or halt state.

On switching the channel to the autonomous mode, the signal is picked up on the "channel ready" line from the channel to the processor. This leads to setting of the result tag "Z," indicating that the channel is switched off. The tag is generated directly in the processor on execution of the input-output instructions. During operation of the channel in the model the toggle switches on the monitoring and adjustment panels "IMOP," "ZGR ADR" and "IM FI" must be off, and the "Chast." toggle switch must be on.

The on-line memory YeS-3205 can be checked during operation with the processor in the following modes: automatic checking on the test sections of the on-line memory, write and read by a defined address; automatic writing and reading with respect to the entire memory bank.

The automatic test mode in the test sections is designed for complete checking of the operation, prevention and search for failures in the on-line memory. The test sections are put together in such a way that they provide for the creation of modes that are the most serious for storing the modules and the read cycles and checking out the address cycle of the memory.

When executing the test sections, errors are recorded during operation of the unit, and a message is output containing information about the errors. In order to obtain information during error analysis it is necessary to use a description of the test sections.

The YeS-2050 processor is designed to operate only in the complex mode. Therefore checking the processor with the test programs input to the on-line memory is done only in the model.

The search for a processor failure or error is made using the technical servicing monitor programs or the test for locating failures, which is designed for storing the state of the basic registers and the control flip-flops of the processor in a fixed region of memory. This test offers the possibility of performing subsequent analysis of the filled information in order to locate the failures. When recording the state of the processor, it is also possible to enter information in the memory about the state of the memory module in which the error has appeared.

The tests to locate a failure are used in the following cases: on appearance of an unmasked error signal in the processor or memory operating with the processor, initialization of the DIAGNOSTICS instruction cycle counter, if the tag for the "accounting" procedure is present in the control word of this instruction or the "start accounting" button is pressed.

If a processor failure cannot be automatically detected (no monitoring and adjustment test program is run, no monitoring and diagnostic module is in operation), then the search for the error or failure is made manually. For this purpose, first of all an error analysis is made on the basis of the operating logic of the processor and the logic of execution of the given section of the program.

The processor in the preventive mode is checked out on putting it into operation, after prolonged (more than 1 month) idle time or storage, in the presence of frequent short-term errors when solving the problem, although all of the verification tests are performed correctly without errors or with errors in the test programs of the user, during the course of the performance of adjustment operations.

The checking in the preventive mode is done with voltage deviation from rated by 5%.

When searching for unstable failures (errors) of any processor assembly, it is recommended that the voltage of the power pack of the given assembly be lowered, and the voltage of the remaining UBP be raised by 5%.

The preventive mode is also realized on variation of the master oscillator frequency. For this purpose, on the control panel it is necessary to press the "frequency" button and perform a single start of the verification test sections of the processor.

Search for and Elimination of Failures. Variation of the parameters, adjustment and repair of the standardized modules are carried out using special equipment.

In addition to the service equipment, universal, monitoring and measuring devices are used: the oscillograph S1-31 and S1-39, the generators G3-7a and G5-19, the digital volt meter VK7-10A/1, the milliammeter M-254, and so on.

In connection with the variety of logic of the circuits and the instructions executed in the processor it is difficult to recommend a single procedure for finding any failure, for in each case it is determined by the logic of the operation of the circuits and the nature of the failure. However, there are some general methods which are correct for finding the majority of failures.

When searching for the failures primarily it is recommended that the operating mode be set "on command" and the section of the program making the error be executed in this mode, carefully analyzing the result by the control panel display, the result tag and the sequence of the instructions performed and prepared for execution.

When detecting an incorrectly performed instruction it is necessary again in the "on command" mode to execute this section of the program to the incorrectly executed instruction. Then, pressing on the "pulse" button, transfer to the execution of this instruction by one sync pulse, observing the switching of the flip-flops after each pulse on the display.

If in the "on command" and "by pulses" modes it is not possible to detect the improperly executed section of the program on the display, it is possible to cycle this section of the program, successively setting up the numbers 1,2,3 and so on on the instruction execution counter and analyzing the execution of the program to find the improperly executed instruction. Further search for the location of the error in the executed instruction usually is made using the oscillograph S1-31 or S-39 or the digital voltmeter VK7-10A/1.

When searching for unstable errors, preventive voltage is set up in the power pack of the panels, the equipment of which is supposedly making the error, and the error section of the program is executed. After locating the error, checking the feed voltage, inspecting the wiring and contacts, the failure is more precisely defined, and correspondence of the input and output signals (their presence and shape) is checked by the time diagrams for operating in the given mode.

On deviation of the voltages or the parameters of the signals, in the case of reliable contactsor closure of them, it is primarily necessary to eliminate these failures.

If the input signals satisfy all the requirements and correspond to the operating time diagram, and the output signals are distorted, then the module is checked on the bench.

The search for a failure in the electric power supply system is made in the following sequence. Using the voltmeter of the electromagnetic system of accuracy class no less than 2.5 (for example, Ts434), the voltage of the feed network of the distributing bay is measured, to which the cables of the failed unit are connected. The readings of the voltmeter must be 187 to 242 volts. If the voltmeter readings are smaller, it is necessary to check the circuit breakers through which the voltage is fed. If the voltage at the BUP output does not correspond to the rated value with proper readings of the voltmeter, then the BUP is changed.

20.6. Installation of the Unifed System of Computers and Safety Engineering When Servicing Them

All models of the unified system of computers are designed for operation in stationary, heated facilities using ventilation and air conditioning. The temperature must be maintained at 20±5°C, the relative humidity must stay at 65±15%. All the computer units are placed in a machine room in strict accordance with the installation instructions. Variations of the installation layout for any model are permitted only by agreement with the manufacturer. The computer units are set up in zones (Figure 20.3).

In the machine room provision must be made for a process floor mounted on standard metal structural elements at a height of 20 to 40 cm above the main floor. The space under the process floor is used for laying power cables, signal lines, protective and grounding buses. This space is also used as the intake ventilation channel. The temperature of the air fed to the computer must be 14 to 18°C, the relative humidity no more than 70 to 80%, and the dust content, no more than 0.75 millihenries/m^3.

The degree of cleaning of the air fed to the facilities and the units of the unified system of computers must be no less than 99.95% for particles of 5 microns or more, 97% for particles up to 5 microns, 90% for particles to 3 microns and 50% for particles to 1 micron. The dust content in the air in the machine room must not exceed 1 mg/m3 with the particle size of no more than 3 microns. In order to remove the exhaust and dusty air from the facilities, a suspended perforated ceiling is used.

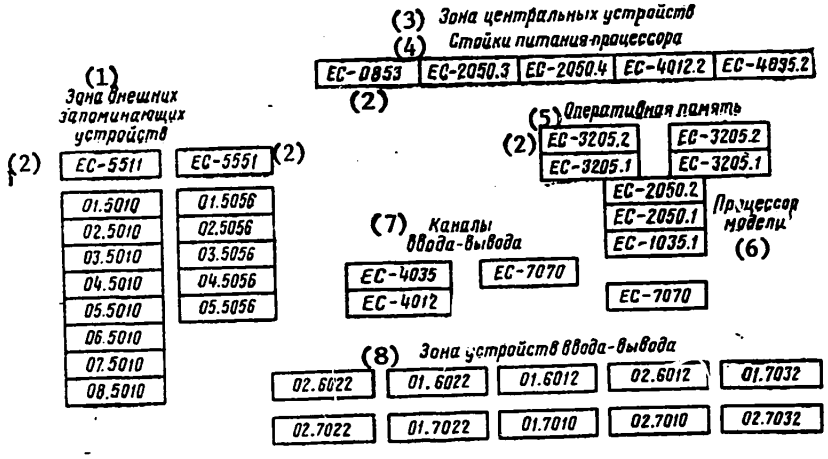

Figure 20.3. Layout of the YeS-1050

Key:
1. External memory zone
2. YeS- ...
3. Central unit zone
4. Processor power base
5. On-line memory
6. Model processor
7. Input-output channels
8. Input-output unit zone

The structural material of the ceiling and walls must insure effective noise absorption (noise level in the machine room should not exceed 75 decibels). For entry to the machine room it is necessary to provide a vestibule with door height of no less than 180 cm and width of no less than 110 cm. Access to the machine room must be strictly uninhibited, and the service personnel must use special clothing and replaceable footwear.

The computers and process equipment are installed as follows: 1. Installation of the ventilation system. 2. Installation of the lighting network and winding up the primary power feeder to the power supply distribution cabinet. 3. Installation of the protective and grounding buses. 4. Assembly of the process ceiling with connection of lights to the lighting system. 5. Lining the walls with sound absorbing panel. 6. Assembly of the process floor, laying the power supply cables and signal circuit lines.

Before installing the computers, the process floor is laid out, holes are cut for the cables and lines to connect the computer bays. The electric power distribution panel is installed. Power instability must not exceed +10% or -15% with respect to voltage and ±1% with respect to frequency. The transient resistance of the protective "ground" bus must not be more than 0.6 ohm.

The units are installed in accordance with the installation instructions in the following sequence: the processor bays, selected channel bays, multiplex channel bays and the basic core memory bays.

The central computer units can be assembled with simultaneous installation of peripheral devices.

The connections between units are made using standardized connection means. They include the following: cables for switching the lines of the input-output interfaces, direct control, small interface, electric power interface; boxes for connecting logical circuits and electric power circuits; resistor modules installed on the units to match the line and also for switching the "access" lines; a plug for switching the electric power control interface lines on switching off the units and also to insure electrical safety of the service personnel when disconnecting the cable.

The cables have different lengths, which makes it possible to install the computers in a facility with different floor plans.

After spreading, they are marked on both sides.

The electric power supply units of the YeS-1050 computer are connected to a three-phase, four-wire 380/220 volt network with grounded neutral.

In the machine room a protective grounding bus (ground wire) is laid with a transverse cross sectional area of no less than 120 mm^2, which is connected to the grounded neutral of the electrical installation. The resistance of the ground, to which the neutral is connected must be no more than 0.6 ohm. The protective grounding bus must be accessible for inspection. The openly laid bus is painted black. Painting the bus another color is permitted to harmonize with the color of the facility, but at the connection and branch points it must have no less than two black stripes running a distance of 150 mm from each other.

The cases of all the computer units are connected to the bus by ground wires which form part of the units. The bus sections are lap connected and welded. The length of the connection is no less than twice the bus width.

In order to observe the electrical safety rules when installing and operating the computer, it is forbidden to perform any installation operations, replace the cells and parts, or to solder under voltage. On connection the oscillographs and measuring instruments to the equipment for monitoring or adjustment, it is necessary to use wires with insulated holders. During the performance of these operations a man must stand on a rubber mat. It is permissible to use only low-voltage soldering irons and 12, 24 or 36 volt lights.

The peripheral devices must not be put into operation with the cases or protective covers removed or with the panels off or open. All of the adjustment, cleaning and lubrication operations are performed with the power off. When it is necessary to shut off the electric circuit quickly, the "emergency off" buttons are used.

In accordance with the fire safety requirements, all of the computer center facilities must be equipped with an automatic fire alarm based on standard equipment (sensors, the alarm signals and wiring). All the computer center personnel must be instructed what to do in case of fire.

20.7. Use of the Unified System of Computers in ASUZhT [Automated Railroad Transportation Control System]

The basic trend in the development of computer engineering is connected with the creation and application of automated control systems (ASU) in all branches of the national economy. In railroad transportation a great deal of work is being done to introduce automated control systems to control the shipping process. Individual automated control systems are joined by the information computer center of the Ministry of Railways, and taken altogether they form an automated railroad transportation control system (ASUZhT) which is part of the national automated data gathering and processing system (OGASU).

The structure of the automated control system in general form is presented in Figure 20.4. In railroad transportation there is a developed control structure including the central apparatus of the Ministry of Railways, the railway administrations, and the railroad divisions. The ASUZhT is being introduced without rearranging this system, retaining all of its links. However, application of a computer permits significant improvement of the quality of control, unloading of the existing control system from performing the technical work of a computational, information and analytical nature, and optimizing the solutions obtained.

For effective application of a computer it is necessary to develop algorithms and programs for the solved problems, coordinate the operation of the computer center with the production process of the object of control and with the requirement of the existing traffic control system. In addition, it is necessary to introduce an information gathering subsystem for gathering information about the shipping process and an organizational communication subsystem for transmitting this information. In railroad transportation the creation of the indicated subsystems is a complicated technical problem.

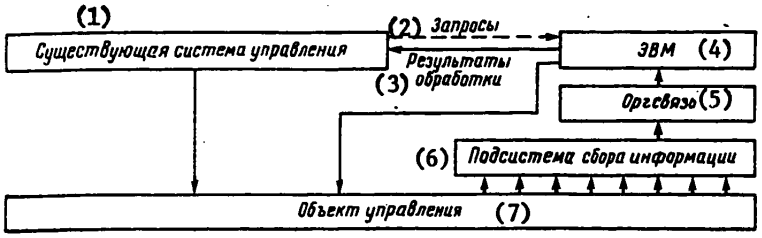

Figure 20.4. Structure of the automated control system

Key:
1. Existing control system; 2. request; 3. processing results; 4. computer; 5. organizational communication; 6. data gathering subsystem; 7. object of control

The ASUZhT is characterized by a set of mathematical economic methods, computer engineering and organizational communications means which permit significant improvement of the quality of the management of the transportation operation and operative accounting for the activity of its subdivisions. The transport process is a dynamic system, the control of which within the framework of the ASUZhT is connected with processing enormous flows of information input to the computer immediately as it is generated. On the basis of this information an entire set of problems can be solved. The more data accumulated in the computer memory, the more efficiently various accounting and management problems can be solved.

Thus, in a computer operating as part of the ASUZhT, an information model of the object of control, that is, the railroad, is created, and the corresponding information is continuously corrected according to the course of the real shipping process. The indicated information model implemented on a computer is the basis for the ASUZhT.

When formulating the ASUZhT functions, it is necessary to isolate the following types of problems as the most urgent: prospective planning of shipping operations and coordination of them with other types of transportation and also with the work of industry and agriculture; operative control of the shipping process and consideration of the operation of the railroad transport subdivisions; control of material and technical supply, use and repair of the track, rolling stock and other technical means; automatic reserving and accounting for places on passenger trains and accounting for passenger flows and ticketing operations; monitoring the document circulation; accounting for personnel and material goods.

The basic links of the ASUZhT are the computer centers in the railroad administrations (DVTs) of which there are 32, and the main computer center TVTs of the Ministry of Railways (Figure 20.5). In the branch subsystem of the DVTs, a railroad communications junction is provided, and in the GVTs MPS [main computer center of the Ministry of Railways], a central communications office.

As a rule, no less than two identical basic computers are installed in each computer center which are capable of working with common memories, with a standard makeup in order to insure continuous operation of the ASUZhT in real time.

The computers operate in two data processing modes: in real time with input of the information directly from the communications channels to the computer complex for implementation of the dynamic model of the shipping process; in the multiprogram package data processing mode with input of the information from punch cards, punch tapes, magnetic tapes and discs. One computer is specialized for regular operation in real time and the other backs it up and processes in the package mode. In necessary cases, with appropriate technical-economic substantiation, further computers can be installed.

As the basis for the GVTs MPS and the railroad computer centers, multiprogram third-generation computers from the unified system (unified system of computers) are used which have the following example technical parameters matched by the temporary operating group of the CEMA with respect to application of computer engineering in transportation: on-line memory access time 1-2 microseconds for 4 bytes (average speed no less than 10^5 operations/second); on-line memory no less than 512 kbytes (with the possibility of adding a rapid-access memory); two types

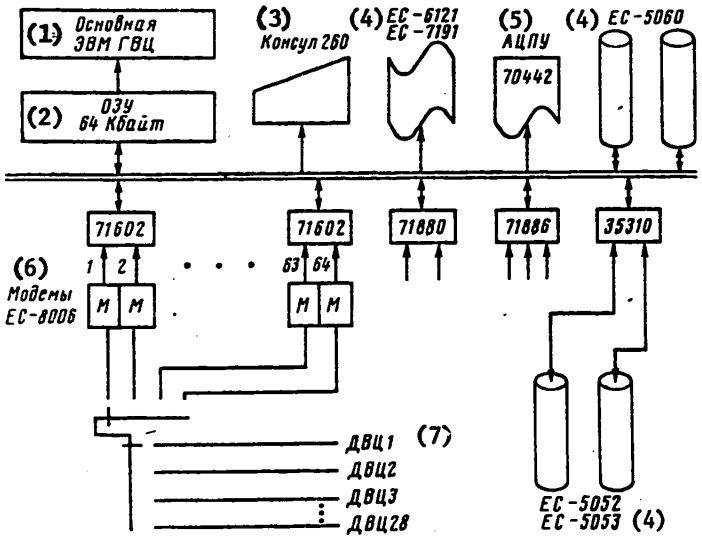

Figure 20.5. Diagram of the basic ASUZhT computer center

Key:

1. Basic computer of the main computer center
2. 64 Kbyte on-line memory
3. Konsul 260 typewriter
4. YeS ...
5. ATsPU = alphanumeric printer
6. Modems YeS-8006
7. DVTs ... [railroad administration computer centers]

of random-access memories -- on magnetic discs (capacity of one replaceable module 7.5 to 15 million bytes) and magnetic drums (no less than 4 million bytes each); "memory" with series access on magnetic tapes (no less than 8 reel type units, capacity 7.5 million bytes for one reel).

Devices for direct coupling in the data transmission network to 126-256 channels operating at speeds from 50 to 2400 baud are mandatory.

Universal computer software includes dispatcher programs, translators, the library of standard programs, and the set of check problems and diagnostic tests.

For the first phase of the ASUZhT, the available second-generation computers are used in the standard makeup for railroad transportation. However, when developing the second phase of the ASUZhT, conversion to the subsequent generations of computers must be considered.

The data transmission networks must be automated and noise immune with transmission reliability of no less than 1 to 10^{-6}. For the first phase of the ASUZhT, the existing telephone and telegraph communications are used.

The basic principle for constructing the data transmission network is the radial-junction principle with switching centers at the GVTs and DVTs computer centers and also using switching units (concentrators) at the large centers. In order to improve the system reliability, alternate routings are provided to set up connections between the switching centers.

In creating the data transmission network, as a rule, the series-manufactured data transmission equipment is used.

APPENDIX

BASIC TECHNICAL SPECIFICATIONS OF THE MINIMUM COMPOSITION OF INPUT-OUTPUT UNITS USED IN THE YeS-1020 and YeS-1033*

YeS-5017 Magnetic Tape Storage

Number of magnetic tape storages in the computer layout	4
Capacity, megabytes	25
Recording density, bits/mm	8 and 32
Information recording method	BVN-1
Tape speed for writing and reading, meters/sec	2
Data exchange rate (with density of 32 bits/mm) kbytes/sec	64

Magnetic Tape Storage Controller

Number of connected storages	to 8
Operating mode with channel	exclusive

Replaceable Disc Packet Storage YeS-5056

Number of magnetic disc storages in the computer makeup	4
Disc package capacity, megabytes	7.25
Recording density, bits/mm	29-44
Number of working surfaces of the disc package	10
Average access time to information, milliseconds	60
Data transmission rate, kbytes/sec	156

YeS-5551M Magnetic Disc Storage Controller

Number of connected storages	to 8
Operating conditions with channel	exclusive

*The minimum set of UVV [input-output units] for the YeS-1022 and YeS-1033 is the same.

YeS-6012 Punch Card Input Unit	
Read speed, cards/min	600
Read method	Photoelectric
Hopper size, cards:	
feed	1000
receive	1000
YeS-6022 Punch Tape Input Unit	
Input speed, lines/sec	1500
Punch tape type	5-8-track
YeS-7077 Console Typewriter with Coupler*	
Print speed, character/sec	10
Character set	92
Number of copies	5
Width of paper roll, mm	280
YeS-7032 Printer*	
Printing speed, line/min	820
Character set	83
Number of characters per line	128
Number of copies	5
Paper width, mm	80-420
YeS-7010 Punch Card Data Output Unit	
Output speed, card/min	100
Hopper size, cards:	
feed	700
receive	2×700
YeS-7022 Punch Tape Output Unit	
Output speed, line/sec	150
Type of punch tape	5-8-track
YeS-9011 Punch Card Data Preparation Unit*	
Manual punch speed, column/sec	15
Duplication speed, column/sec	25
Hopper size, cards:	
feed	500
receive	2×500
YeS-9024 Punch Tape Data Preparation Unit	
Punch speed, line/sec	50
Punch tape type	5-8-track

*The "Konsul-260" typewriter built in Czechoslovakia is used in this unit.

BIBLIOGRAPHY

1. Al'yanakh, I. N. VNESHNIYE ZAPOMINAYUSHCHIYE USTROYSTVA YES EVM [External Memories of the Unified System of Computers], Moscow, Sovetskoye radio, 179, 208 pages.

2. Drozdov, Ye. A.; Komarnitskiy, V. A.; Pyatibratov, A. P. ELEKTRONNYYE VYCHISLITEL'NYYE MASHINY YEDINOY SISTEMY [Computers of the Unified System], Moscow, Mashinostroyeniye, 1976, 672 pages.

3. Kagan, B. M. ELEKTRONNYYE VYCHISLITEL'NYYE MASHINY I SISTEMY [Computers and Computer Systems], Moscow, Energiya, 1979, 528 pages.

4. Kachkov, V. P.; Kondrat'yev, A. P., et al. ELEKTRONNAYA VYCHISLITEL'NAYA MASHINA YES-1022 [YeS-1022 Computer],Moscow, Statistika, 1979, 208 pages.

5. Mayorov, S. A.; Krutovskikh, S. A.; Smirnov, A. A. ELEKTRONNYYE VYCHISLITEL'NYYE MASHINY: SPRAVOCHNIK PO KONSTRUIROVANIYU [Computers: Design Handbook], Moscow, Sovetskoye radio, 1976, 504 pages.

6. Mitreykin, N. A.; Ozerskiy, A. I. KONSTRUIROVANIYE APPARATURY AVTOMATIKI I TELEMEKHANIKI [Design of Automation and Remote Control Equipment], Moscow, Mashinostroyeniye, 1975, 272 pages.

7. Neshumova, K. A. ELEKTRONNYYE TSIFROVYYE VYCHISLITEL'NYYE MASHINY [Digital Computers], Moscow, Vysshaya shkola, 1975, 328 pages.

8. PROTSESSOR EVM YES-1020 [YeS-1020 Computer Processor], edited by A. M. Larionov, Moscow, Statistika, 1975, 160 pages.

9. Ryzhkov, V. A.; Sergeyev, N. P.; Markov, B. M. VNESHNIYE ZU NA MAGNITNOM NOSITELE [External Magnetic Memories], Moscow, Energiya, 1978, 224 pages.

10. SISTEMA DOKUMENTATSII YEDINOY SISTEMY EVM [Document System for the Unified System of Computer], edited by A. M. Larionov, Moscow, Statistika, 1976, 328 pages.

11. SPRAVOCHNIK PO TSIFROVOY VYCHISLITEL'NOY TEKHNIKE [Handbook on Digital Computer Engineering], edited by Corresponding Member of the Ukrainian SSR Academy of Sciences B. N. Malinovskiy, Kiev, Tekhnika, 1974, 512 pages.

12. Flores, A. VNESHNIYE USTROYSTVA EVM [Peripheral Devices of Computers], Moscow, Mir, 1977, 550 pages.

13. Shelikhov, A. A.; Selivanoy, Yu. P. VYCHISLITEL'NYYE MASHINY: SPRAVOCHNIK [Computers: Handbook], Moscow, Energiya, 1978, 224 pages.

14. Shigin, A. G.; Deryugin, A. A. TSIFROVYYE VYCHISLITEL'NYYE MASHINY (PAMYAT' TSVM) [Digital Computers (Digital Computer Memory)], Moscow, Energiya, 1975, 536 pages.

15. ELEKTRONNAYA VYCHISLITEL'NAYA MASHINA YES-1020 [YeS-1020 Computer], edited by A. M. Larionov, Moscow, Statistika, 1975, 128 pages.

16. ELEKTRONNAYA VYCHISLITEL'NAYA MASHINA YES-1030 [YeS-1030 Computer], edited by A. M. Larionov, Moscow, Statistika, 1977, 256 pages.

17. ELEKTRONNAYA VYCHISLITEL'NAYA MASHINA YES-1050 [YeS-1050 Computer], edited by A. M. Larionov, Moscow, Statistika, 1976, 302 pages.

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