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SCIENCE AND TECHNOLOGY

CHARACTERISTICS OF HITACHI M-280H COMPUTER DESCRIBED

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[Article by Kenichi Furumaya (chief), Toshihiko Ktaka, Katsuhiko Takizawa, Fumiyuki Kobayashi, Chikahiko Izumi of Dept. of Development, Kanagawa Plant, Hit Hitachi, Ltd.]

[Text] Abstract by Nikkei Electronics

The M-280H is a general-purpose large computer which has 1.3-1.6 times more throughput than the conventional M-200H. In order to realize this throughput, various improvements have been made in the systems and in the semiconductor technology. Regarding the systems, they are not basically different from the M-200H. However, the M-280H has delicate control, for instance, disorders in the pipeline are reduced by subdividing SS (storage to storage) type instructions for processing. In semiconductor technology, the degree of integration of logic-in memories and high-speed bipolar memories is doubled and quadrupled respectively to give latitude for the expansion of buffer memories. Also, the main memory capacity is enlarged to 32 M bytes from the conventional maximum 16 M bytes, and the channel throughput to the maximum 96 bytes/sec.

The systems for users who utilize large computers have recently increased in scale rapidly, and the mode of use tends to be increasingly diversified. In line with this trend, computer makers strive continuously to develop new large models with better throughput.[1,2,6,7]

The HITAC M-280H (called M-280H hereafter) is the top model of the HITAC M series due to its larger scale, greater versatility and higher performance. It is better than the M-200H announced in 1978.[1]

The M-280H was developed under the following guidelines.

(1) Improvement of Throughput

Using the latest hardware technology, the speed of the logic system was raised, and firmware such as a system expansion mechanism and a VMA (virtual machine assist) mechanism, was incorporated.

(2) Emphasis on New System Mechanism Support and Future Expandability

It is supplied with a main memory which exceeds 16 M bytes and can accommodate over 16 channel connections, and a 3 M bytes/sec high-speed channel connection. Also, it has room for future expansion of the main storage, expansion of the buffer storage and connection for a high-speed I/O unit.

(3) Improvement in Reliability/Maintainability

Highly reliable parts were used, and it is fully equipped with an automatic recovery function and a maintenance function.

(4) Relaxation of Equipment Conditions

Aiming at space-saving and energy-saving, cables for connecting peripherals (discs in particular) are more extendable than in conventional models. Also, an optical channel adapter was provided to make it possible to use optical fibers in lieu of I/O cables.

(5) Improvement in Operability

The console function is fully equipped, and the automatic-run function is reinforced.

Among the above developmental guidelines, the most important item is the improvement of throughput suitable for the top model.

Throughput of computer systems has two aspects: a capability based on how fast a job can be processed and a capability based on how many jobs can be processed in a given time. The former capability is demanded by large-scale science and technology calculations, while the latter capability is demanded by on-line systems for bank deposits and seat reservations. Recently, demands for processing many jobs in a given time, such as on-line processing and conversation processing, are on the rise, and improvement of system throughput has tended to be stressed. However, with the progress of science and technology, demands for high-speed processing of large-scale science and technology calculations (one job) are also increasing.

In November 1980, the U.S. IBM introduced a new large computer, the M-3081 (Model group D). This model is said to have a great improvement in performance over the same company's model 3033, which was the top of the line until then. Also, it was highlighted because of its double-headed processor.[6] In the case of the double-headed processor, two processors operate in parallel, and the capability to process many jobs in a given time is the sum of the two processors, however, the capability to process a job at high speed may sometimes be determined by the capability of one processor, reducing capability, in this case, to half of the total throughput.

With this background in mind, we developed a high-performance processor which greatly exceeds that of the M-200H, incorporating a single processor in order to meet the two demands--improvement of system throughput and high-speed processing (of one job).

The M-280H can use practically all the software, peripherals and terminals of the existing M-series as system components. It is considered that a system composed of this processor, a VOS3/SP (virtual storage operating system 3/system product) which is a new program product, a VMS/ESO (virtual machines system/extended system option) and a new large capacity disc drive (1260 M bytes/spindle) to be supported by these, along with a Chinese character printer and a video data system, can very well accommodate diverse user needs.

I. Processor Outline

Figure 1 shows the external appearance of the M-280H system. Figure 2 gives an example of the architecture of a two-unit close-linked multiprocessor. The M-280H is the sister machine of the M-200H, and its external appearance and logic structure are similar to the M-200H. However, it is a processor designed for high speed and high reliability using newly developed high-integration LSI and semiconductor memories.

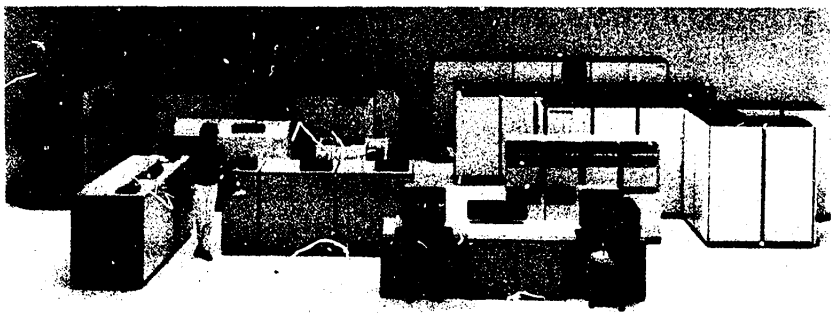


Figure 1. External Appearance of the M-280H Processor

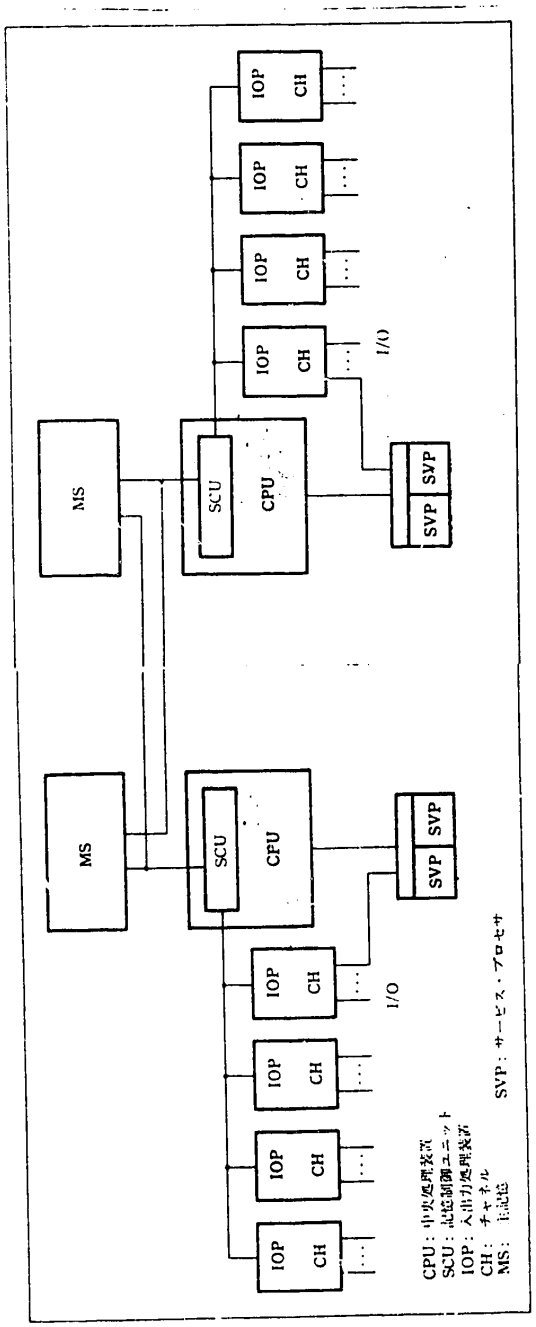


Figure 2. The M-280H Architecture. Chart shows two-unit close-linked multiprocessor architecture. Architectural limit: incorporation of maximum four units.

Key: CPU: central processing unit
SCU: storage control unit
CH : channel
MS : main storage
SVP: service processor

Realization of Throughput 1.3-1.6 Times Greater Than the M-200H

Table 1 gives the general specifications of the M-280H in comparison with the M-200H and the M-180, which were yesterday's top of the line models. The system functional specifications of the M-280H were expanded, for example, doubling the main storage capacity and the channel numbers connectable to the system compared to the M-200H. Also, the channel total data transfer capability is approximately four times better than the M-200H, to a maximum of 96 M bytes/sec/processor.

Table 1. Architectural Comparison of M-280H With Conventional M-200H and M-180. System specifications of M-280H are expanded in main storage capacity and in number of connectable channels.

Item		M-280H	M-200H	M-180
Main storage maximum capacity (M-byte)		32	16	16
buffer storage	capacity (k byte)	64	64	32
	control system, column x line	set associative 64x16		set associative 256x4
	block size (byte)	64	64	32
address translation buffer	setup, entry x level	256x2	256x2	128x2
	number of entries	512	512	256
I/O channel	maximum number of IOP	4	3	2
	maximum number of channels	32	16	16
	total data transfer capability	96	26	16
Integrated array processor		yes	yes	yes
System expansion mechanism		Standard	Peripheral	Peripheral

In performance, the M-280H has a throughput 3.5-5 times and 1.3-1.6 times more than the M-180 and the M-200H, respectively. Figure 3 gives an example of a specific performance comparison when some jobs were processed. In this case, the assigned jobs consisted of two technical calculations, one general compile job and one Cobol office calculation. With the standard M-280H, performance about 4.5-5 times superior to the M-180 (1.4-1.5 times superior to the M-200H) was obtained in handling the technical calculations and the general compile job, while performance 5 times superior (1.6 times to the M-200H) was obtained in the office calculation. In calculations using a M-280H with IAP (integrated array processor), performance was approximately 6 times and almost 14 times better in handling the respective jobs.

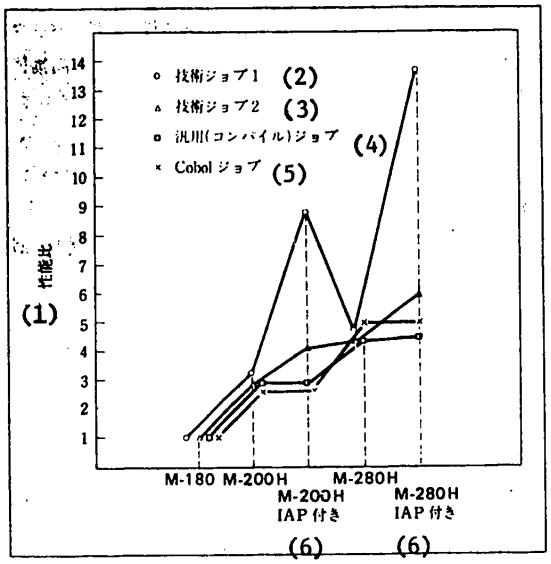


Figure 3. Example of Performance in Benchmark Test Program

Key:
(1) performance ratio
(2) technical job 1
(3) technical job 2
(4) general (compile) job
(5) Cobol job
(6) with IAP

The throughput of technical calculations using this system with IAP is equivalent to approximately 10 MFLOPS (million floating point operations per second). This range of performance is close to that of a supercomputer, and is very difficult for a general-purpose computer to achieve.

The high-speed processing of the M-280H is primarily derived from the shortened machine cycle time. In order to shorten the machine cycle time, we have developed the latest hardware technology beginning with a maximum 1,500 gate/chip high-integration high-speed LSI and logic systems suitable to that, as will be discussed later in this article. Also, high speed is achieved by incorporating a system which was designed to shorten the operation execution cycle in respect to some instructions.

Upgrading of Element Integration and Expansion of System Specifications

In the following, hardware technology, logic systems and system specifications newly developed for the M-280H will be listed in comparison with those of the M-200H.

1. Hardware Technology

Logic LSI with Maximum Gate 550/1500. Improved approximately two-thirds compared with that used for the M-200H in terms of speed power product.

Logic-In Memory Element. Used for address array of the buffer storage. The degree of integration is double that of the M-200H.

4 K Bit High-Speed Bipolar Memory--maintains 7 ns-element-level maximum access time and is used for control storage and buffer storage. The degree of integration is quadrupled compared with that of the M-200H.

64 K Big High Speed n MOS Memory--used for the main storage. The degree of integration is quadruple that of the M-200H.

18 Layer Backboard. Improved in wiring density 33 percent, to 18 layers, compared with the M-200H. The backboard of the M-200H has 14 layers.

2. Logic Systems

The logic systems adopted in the M-280H took basic parts from the M-200H, but those parts were also further strengthened in several ways. What the M-280H took from the basic logic systems[1] of the M-200H are: (1) sophisticated pipeline control, (2) microprogram distribution and layout, (3) 64 K byte high-speed buffer storage accessible every 1/2 machine cycle, (4) 512 pairs of address translation buffers (TLB), (5) high-speed computation mechanism calculable at 1/2 machine cycle, (6) 8 or 16 way interleaves of main storage, (7) integrated array processor (IAP).

In the M-280H, the following further points were reinforced making the most of the characteristics of these logic systems.

Reinforcement of Pipeline Control

- Development of primitive resolution function.
- Augmentation of branch instruction control.
- Augmentation of pipeline disorder factor detection capability.
- Improvement of capability to recover from pipeline disorders.

Shortening of computation cycle numbers of decimal arithmetic instructions.
Integrated array processor instruction expansion
Firmware provided as standard.

3. Expansion of System Specifications

Maximum Main Storage Capacity Expanded to 32 M Byte

That of the conventional M series is 16 M bytes. In order to expand the main storage capacity, it is necessary to expand the effective address from 24 bits. Therefore, the page table entry which translates a logical address to an effective address was expanded.

Maximum Connectable Channel Numbers Expanded From 16 to 32

The channel throughput was enlarged to accommodate an increase of system file capacity and improvement of the processor's internal processing speed.

II. Logic Structure and System Improvement

A big problem in improving processor performance is the architectural method of the main storage system.

Many of the current general-purpose large processors have a bihierarchical storage system comprised of high-speed buffer storage and comparatively low-speed main storage. The M-200H also used a bihierarchical storage system. When striving to enhance the performance of a single processor mainly by upgrading the speed of the machine cycle, it is necessary to improve the speed of the main storage in proportion to improvement of the machine cycle in order to enhance the total performance proportionately to the improvement in the machine cycle.

On the other hand, demand for a larger main storage capacity is also increasing. This is because systems that perform in parallel conversational processing, batchprocessing, data base processing, etc, all in the same system, have increased, and a large main storage capacity suitable for these systems is in demand. These needs are especially prevalent in regard to large computers.

In other words, there are two things demanded of the memory--improvement in the speed of elements and upgrading of the capacity. However, from the aspect of semiconductor technology, a project to achieve higher speed and integration not only encounters technical difficulty but also raises costs, making it difficult to improve the cost performance ratio. Therefore, a general solution to this problem boils down to the adoption of a high-speed buffer storage.

An average instruction execution time Tavg of a processor with a buffer storage can be expressed as

$$Tavg = Tb + \frac{1}{N} \cdot Tacc \qquad (7)$$

The inverse number to this, MIPS (million instruction per second), is often used as an index for performance. Tb is the average instruction execution time when all instructions and operands are present in the buffer storage. Tacc is the access time of the main storage viewed from the processor. N indicates the incidence rate, once in so many instructions in cases where data to be accessed cannot be found in the buffer storage. Accordingly, (1/N)·Tacc expresses time taken for the main storage access in case the buffer storage does not contain data as an average overhead time/instruction.

(1 - 1/N) is the probability of the presence of the necessary data in the buffer storage, and is sometimes called the hit ratio of the buffer storage. The buffer storage hit ratio is determined by the buffer storage capacity and the nature of a job or a program. When a buffer memory is 64 K bytes, generally the ratio will be in the 85-99 percent range.

Incidentally, by accelerating the processor machine cycle, Tb can be proportionately reduced. However, (1/N)·Tacc remains the same if no further measures are taken, and the total performance sometimes may not improve in proportion to the machine cycle. Consequently, it is necessary to raise the previously described hit ratio, that is, increase the value of N (enlarge buffer storage capacity) to enhance the total performance.

Giving Expandability to Buffer Storage by Upgrading Element Integration

Concerning the above described architectural problem of the memory systems, the following guidelines were observed for the development of the M-280H to avoid the complexity of memory architecture as a whole.

(1) Elements for the main storage were highly integrated to enlarge the storage capacity and to give it future expandability.

(2) A bihierarchical memory structure was adapted, and expandability was given to the buffer storage for the improvement of the buffer storage hit ratio.

In line with these guidelines, for the main storage use, a highly integrated 64 K bit n MOS memory was developed which was suitable for enlargement of capacity. Also, for the buffer storage use, a 4 K bit bipolar memory was developed, in consideration of future expansion, which was four times more highly integrated than that of the M-200H. Intensity of integration was doubled for the logic-in memory (to be described later), also for the sake of future expandability.

Meanwhile, in order to reduce Tb, a basic policy was set to develop high-speed and high-integration logic LSI to be packaged at a high density to improve the machine cycle. This idea to improve performance by high-speed high-density packaging will be discussed further later, but at present, specific examples of improvement in logic systems implemented in conjunction with this will be given.

Further Strengthening of Pipeline Control System

The architecture of the M-280H is shown in Figure 4. The internal makeup of the central processing unit (CPU) is similar to that of the M-200H and consists of a storage control unit (SCU), an instruction control unit (IU), an arithmetic unit (EU) and a service unit (SVU).

The M-280H is characterized by the fact that the inside of the arithmetic unit (EU) is subdivided into a general arithmetic unit (GU) and a floating-point unit (FU), each working as independent logic unit.

As described above, by giving an independent control and memory to each separate general arithmetic unit and floating-point unit, it is possible to shorten the arithmetic loop time required for calculation (for example, time taken for work register contents in a fixed-point addition executed by a general arithmetic unit to be added up and returned to the work register), which eventually shortens the machine cycle.

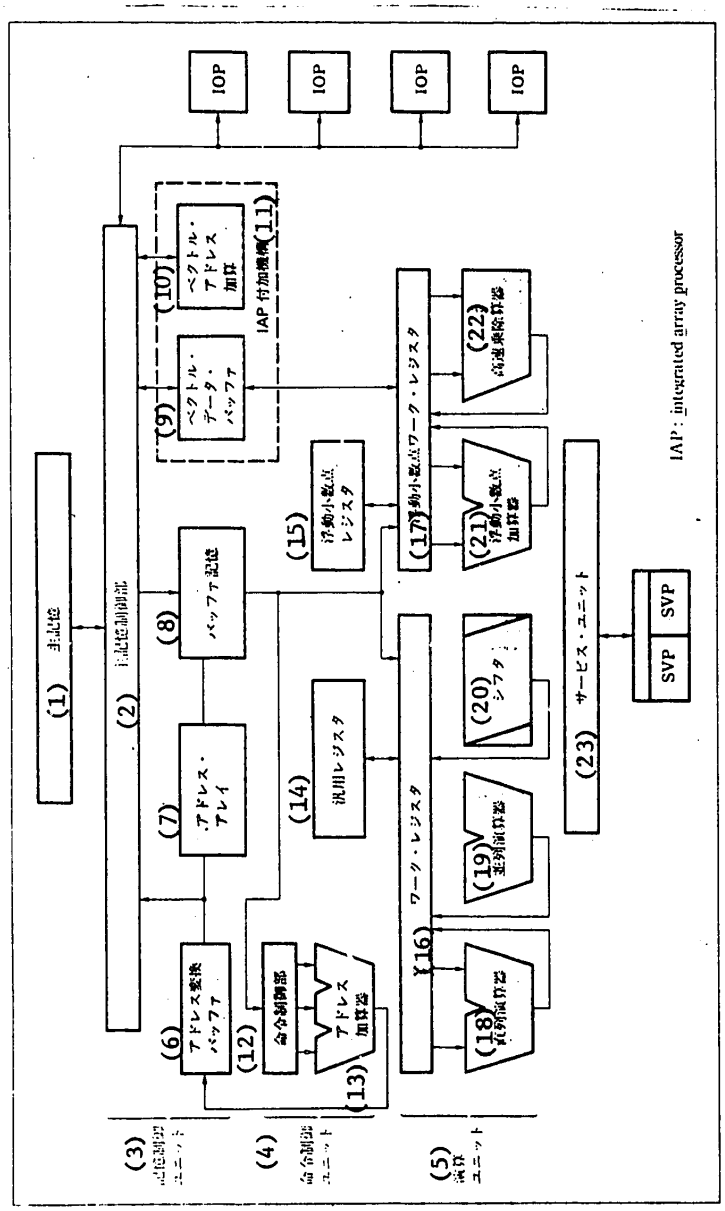


Figure 4. Logic Architecture of the M-280H

Key:
(1) main storage
(2) main storage control
(3) storage control unit
(4) instruction control unit
(5) arithmetic unit
(6) address translation buffer
(7) address array
(8) buffer memory
(9) vector data buffer
(10) vector address addition
(11) with IAP mechanism
(12) instruction control
(13) address adder
(14) general register
(15) floating-point register
(16) work register
(17) floating point work register
(18) serial calculator
(19) parallel calculator
(20) shifter
(21) floating-point adder
(22) high speed HSA
(23) service unit

Regarding GU control storage, the storage capacity is doubled compared to the M-200H for the purposes of supporting an intervirtual memory communication function, providing various firmware as a standard, and shortening the arithmetic cycle numbers.

To realize high-speed operations, the standard operation width is 64 bits. The main calculators are, for instance, a serial adder, a parallel adder, a shifter and a multiplier-divider (HSA).

Next, improvement of the pipeline control system, improvement in reducing the arithmetic cycle numbers necessary for execution of general instructions, and a contrivance for vector processing in an IAP will be described as examples of improvements and contrivances achieved for the instruction processing system.

The pipeline control system, similar to the M-200H, flows as shown in Figure 5 when typical instructions--for instance, Add, Compare, etc--are consecutively given. In processing consecutive typical orders such as this, the IU can transmit an interpreted instruction to the GU at 1 machine cycle pitch. The EU can process this at 1 machine cycle pitch.

The following are possible factors that disturb the above described pipeline control.

(1) Absence of instructions created by the delayed instruction read-out due to the concurring operand read-out and instruction read-out to the buffer storage.

(2) Execution of branch instructions.

(3) Execution of SS (storage to storage) instructions.

(4) Absence of operands by waiting when operands are read immediately after they are written.

(5) Execution of a system control instruction.

(1) is the absence of instructions which occurs when the operand readout of an instruction given four instructions prior to the instruction which must be presently read-out concurs in the same machine cycle in the flow of the pipeline shown in Figure 5, and the instruction read-out in such a case, is put on hold.

To solve this situation, the system was tempered when the M-200H was being developed, so that the simultaneous operand read-out and instruction read-out become possible in the same machine cycle in relation to the buffer storage. Specifically, it was designed to give access to the high-speed buffer storage two times in 1 machine cycle--1 machine cycle was divided into a former-half and a latter-half cycle, and the former-half cycle was used for the operand read-out and the latter-half cycle was used for read/write operation. This system is adopted also in the M-280H. As a result, this problem was completely solved.

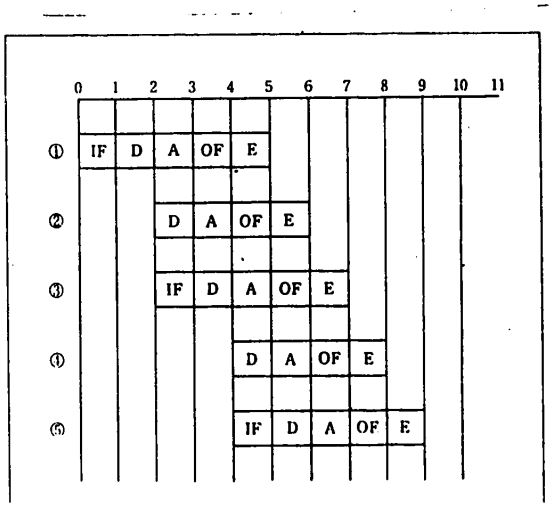


Figure 5. Flow of M-280H Pipeline Control

Key: M-280H pipeline example
IF: instruction read-out
D: instruction decode and address calculation
A: address translation
OF: operand read-out
E: instruction execution

} operation of instruction control unit

} operation of arithmetic unit

(2) is a pipeline disorder during a branch instruction execution due to the absence of an instruction until an instruction is readout from the branch.

In case of the branch instruction, the next instruction is read as an operand. Therefore, an instruction from the branch can be executed at the same time as the execution of the instruction given three instructions later, considering that the data read as an operand is executed as an instruction according to the flow chart of the pipeline in Figure 5.

This flow cannot be essentially avoided. However, in case a negative result is obtained when deciding whether or not to branch based upon the judgment of branching conditions, for instance, in dealing with conditional branch instructions, the waiting time for the results of the judgment of the branch conditions becomes wasteful pipeline disorder time since the only thing to do in reality is to execute the next instruction.

In order to minimize this time, for example, if there are no instructions to change the condition code (CC) before the execution of the branch instruction after the execution of an instruction which determines the CC to be used for the judgment of branch conditions, branching can be contemplated during that time. Specifically, in Figure 5, where instruction(1) is an instruction to determine the CC for judgment of branching, step (4) is a branch instruction, and intermediate (2) and (3) are instructions not to change the CC, branching can be contemplated while executing steps (2) and (3). Such a system was partially adopted in the M-280H to speed up the processing.

SS Type Instructions Loaded on the Pipeline Flow

Next, referring to factors (3), (4) and (5), curtailment of pipeline control disorders derived from these was stressed. As an example of efforts in achieving this goal, let us talk about a high-speed processing method loaded on the pipeline processing flow for SS-type logic operation instructions, which are often used in office calculation programs, on-line programs and control programs.

In the conventional processing of SS-type instructions, pipeline processing was often suspended when these instructions were interpreted because of pipeline processing difficulty due to the procedure where data read from the main storage (or buffer storage) was computed and written into the main storage (or buffer storage).

As a specific instruction, let us think of a move character (MVC) instruction. MVC instruction is an instruction to transfer operands of a certain number of bytes designated by the L (length) field of the instruction from the field designated by the second operand address to the field designated by the first operand address.

For simplification, we shall assume that the length of an operand is 40 bytes, and the operation of the instruction is completed after 5 readings and 5 writings, 8 bytes at a time. Under this condition, we shall assume that 8 byte loading and 8 byte storing will be executed 5 times each, and imitatively, 8 byte load instructions and 8 byte store instructions will be repeatedly processed. By treating this as repetitious consecutive processing of load instructions and store instructions, MVC instructions can be put on the flow of the pipeline processing. The flow of MVC instructions in such a case is shown in Figure 6 (b).

In the flow of the MVC instruction executed in Figure 6, the first operand address is computed in the D1 cycle to keep the address available in the address register. The (OF) cycle is not required for MVC instructions, but it reads out operands in an SS-type logic operation, which uses even the first operand for the operation.

The second operand address is computed in the D2 cycle; the second operand is read in the OF cycle using the above address and written into the first operand address in the E cycle.

Subsequently, 8 is added to the first and second operand addresses and 8 is subtracted from the operand length L, and the processing from the same D2 cycle will be repeated.

With this arrangement, the pipeline processing as shown in Figure 6 (b) can be executed. Figure 6 (a) shows an imaginary computer processing flow without the above described concept. The time to execute the instruction following the MVC instruction is approximately cut in half.

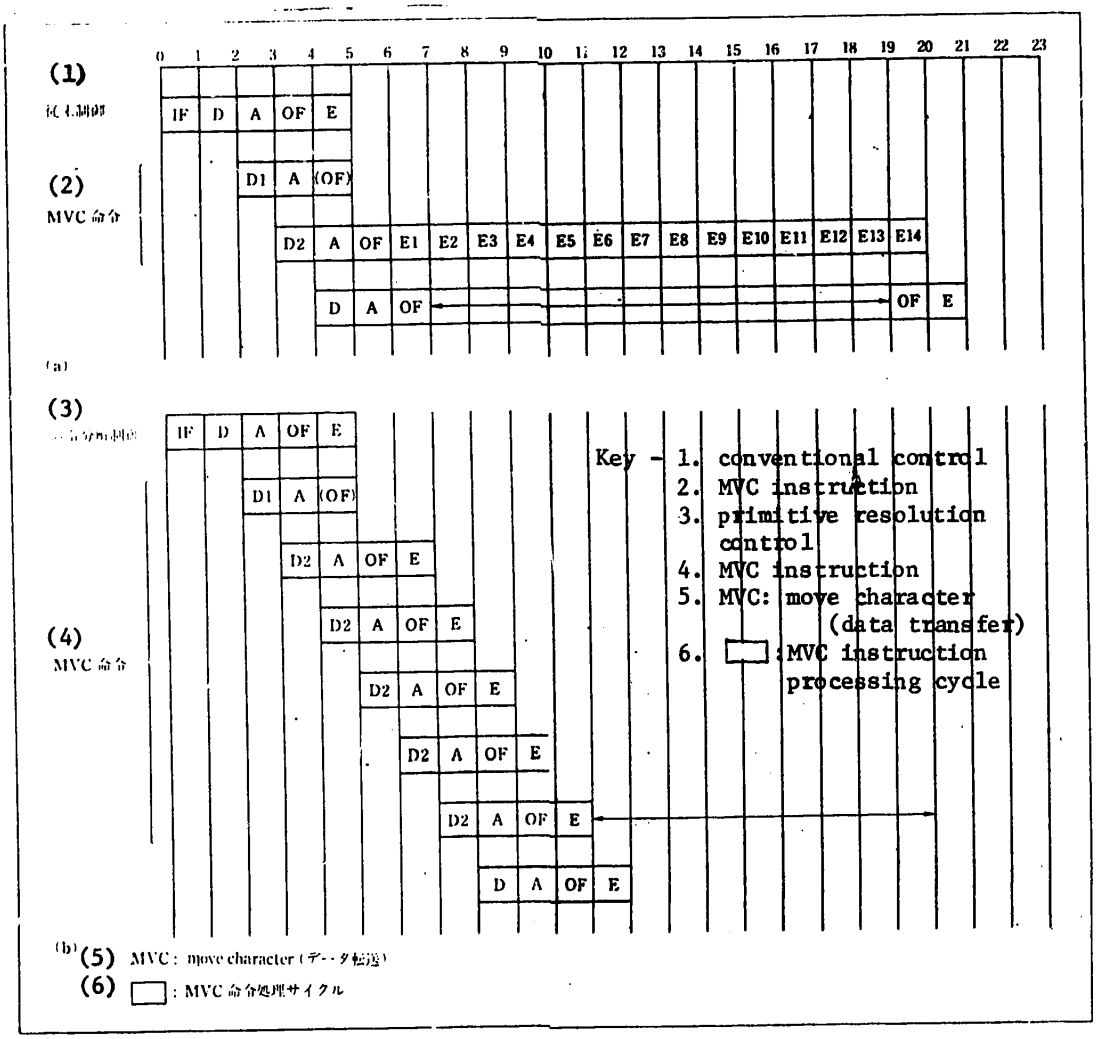


Figure 6. Pipeline Flow of MVC Instruction Processing. The number of machine cycles is nearly cut in half in the M-280H compared to conventional computers.

As an example of speed enhancement by reducing the number of arithmetic cycles, a decimal arithmetic instruction can be given.

In the decimal arithmetic instruction, provisions for a special arithmetic circuit are made when there is a speed-improving effect. At the same time, enhancement of speed was sought by adding specific microprogram routines to respective flows, when, for instance, the processing flow changes due to the difference in the length of operands even within the same instruction.

In Figure 7, decimal instruction performance ratios of the M-200H and the M-280H are shown. On the average, regarding the 6 instructions--addition,

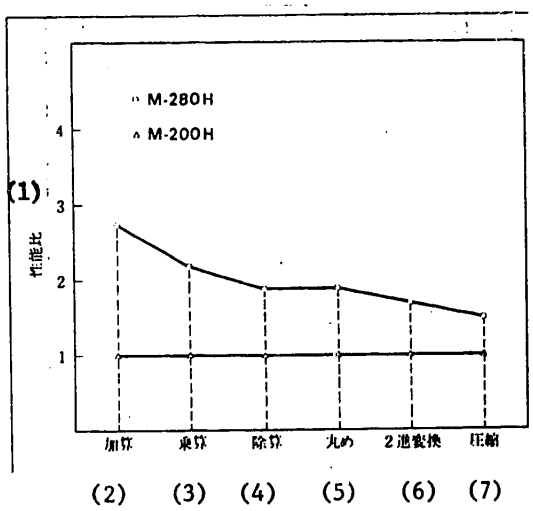


Figure 7. Decimal Arithmetic Instruction Performance Comparison

Key:
(1) performance ratio
(2) addition
(3) multiplication
(4) division
(5) rounding
(6) binary conversion
(7) compression

multiplication, division, rounding, binary conversion and compression--the performance of the M-280H has improved about twofold over the M-200H.

With improvement of the arithmetic systems such as indicated above, the M-280H achieves a throughput 1.5 times greater than the M-200H in the Cobol office calculation programs shown in Figure 2.

On the other hand, for science and technology calculations, it has an IAP add-on mechanism which is unique logic mechanism. The IAP add-on mechanism as shown in Figure 4 consists of a vector data buffer, a vector address adding mechanism and special microprograms.

The IAP converts the innermost side DO loop written by Fortran into a special vector instruction and processes it at high speed using an arithmetic pipeline system which is practiced in supercomputers.

The processing rate at this time occasionally reaches seven-eight times faster than the cases processed by normal instructions.[17] However, the entire program is not processed at such a high speed. Generally, as shown in Figure 8, the processing rate of the entire program becomes 2.5 times faster when, for instance, 80 percent of the program execution time of a normal instruction is converted into that of a vector instruction, and that portion is processed four times faster. The smaller the percentage of the portion which cannot be processed by the vector instruction, the faster the entire program processing rate.

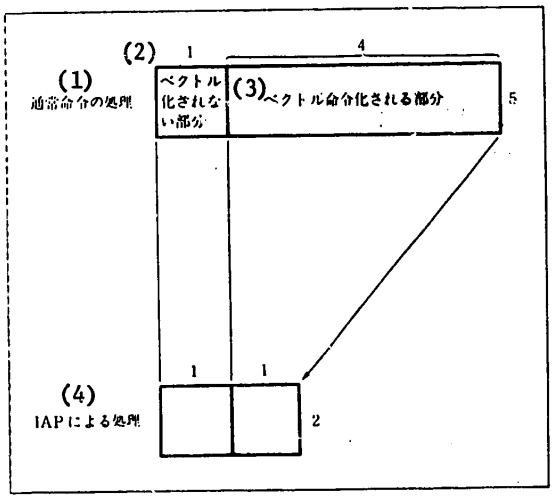


Figure 8. Normal Instruction Processing Time and Processing Time by IAP

Key:
(1) normal instruction processing
(2) portion which cannot be processed by vector instruction
(3) portion which can be processed by vector instruction
(4) processing by IAP

The ratio of this vector instruction processing is designated as vector efficiency, and if vector efficiency is designated as α and the high-speed processing ratio (acceleration ratio) of the vector instruction processing is designated as K, the improvement level of the entire program execution time β can be obtained by the following equation:

$$\beta = \frac{K}{\alpha + K\ (1-\alpha)}$$

As indicated above, improvement of vector efficiency is important for the improvement of general performance. The M-200H has provisions for 18 instructions mainly focusing on four fundamental rule arithmetic vector instructions and vector macro instructions such as an inner product, product sum and summation.

In the DO loops of a science and technology calculation program, the DO loop, which contains conditional sentences (IF statements), appears comparatively frequently but is not suitable for processing the above described four fundamental rule operation and macro instruction by vector instructions.

In the M-280H, a new vector instruction has been added aimed at facilitating vector processing of this DO loop with conditional sentences, in order to improve the vector efficiency.[16] Simultaneously a Fortran compiler was developed, which automatically converted DO loops with conditional sentences into

a vector instruction. By this development, we can expect automatic improvement in vector efficiency and an improvement in the processing rate associated with it.

III. Channel Logic System Design

The channel is under a centralized control system whereby one 0/0 processor (IOP) controls all eight channels, and IOP is highly densely packaged using LSI with 1500 gates to make a more compact architecture than the M-200H. One IOP unit and eight channels are housed on one backboard. IOP is given an image of an independent I/O operation specialty processor with an internal control storage, and has provisions for future functional expansion.

Generally, channel logic sonsists of an I/O interface operation control channel, a data transfer control which controls the data transfer operations relating to the main storage, and an I/O instruction control which controls activations and interruptions. Figure 9 is a block chart which indicates the architecture of an I/O processor with 8 channels connected.

The channel unit contains byte multiplexer channels and block multiplexer channels, and the maximum two units of the former and the eight units of the latter can be connected per one unit of IOP for a versatile connection. The block multiplexer channel, in particular, is equipped with a synchronous transfer function which transfers data at high speed to make 3 M bytes/sec data transfer possible. The conventional maximum 16 channel limit was increased to 32 channels, and the standard block multiplexer channel data transfer speed was upgraded from 1.5 M bytes/sec to 3 M bytes/sec, to achieve an overall throughput increase of approximately fourfold and to make provisions for larger files and a better system throughput.

Data transfer control and I/O instruction control have many interchannel common operations and are independent of the I/O interface operations. Therefore, they are concentrated and compact as a common control. The data transfer control contains data buffer register and address register groups for data transfer. It sends addresses to the main storage in accordance with the read and write requests from the channel to the main storage and reads or writes data from or into the main storage.

The I/O instruction control has a special control storage. Complicated activation and interruption processing are controlled by the microprograms within the control storage.

Also, the I/O instruction control has a channel storage which stores unit control words (UCW)--information that controls the I/O device. The unit control words can be connected to the channel and must be provided with as many as the number of simultaneously operable I/O devices. In the past, 256 words (8 bit address), equivalent to the number of addresses of I/O devices affiliated with the channel, were provided for the byte multiplexer channels in consideration of the connection of the communication lines, but 256 words were not necessarily provided for the block multiplexer channels, considering that the number of simultaneously operable I/O was small. In the M-280H, 256 unit control words

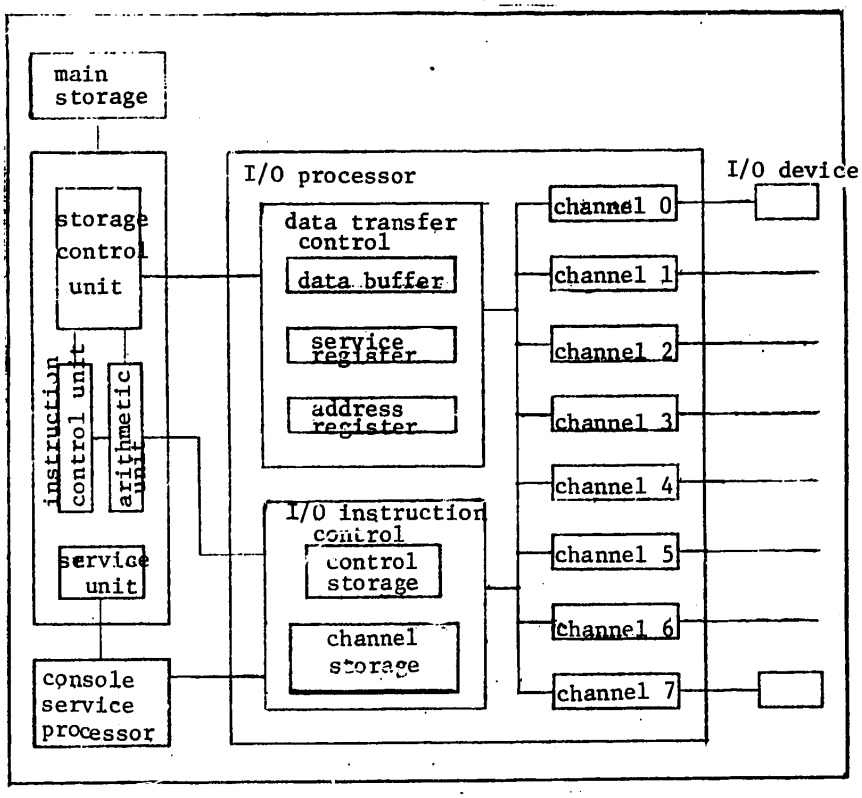


Figure 9. I/O Processor's Logic Structure. Consisting of mutually independent and overlapping channels, data transfer control and I/O instruction control.

are provided for all block multiplexer channels in consideration of the capacity increase of the mass storage system (MSS). The I/O instruction control centralizes and manages channel memories that store the unit control words. Unit control words, for instance, store details of channel command words delivered from software during activation, and the status information is renewed with the progress of the channel operation. After the completion of the operation, part of the details will be reported to the software as interrupt information. Table 2 compares specifications of the new model with the former model.

Table 2. Comparison of Channel Specifications

Number	Item	M-280H	M-200H
1	IOP number/CPU	4	2
2	number of channel/IOP	8	8
3	number of channel/CPU	32	16
4	types of channels		
	byte multiplexer channel	maximum 2/IOP	maximum 2/IOP
	block multiplexer channel	maximum 8/IOP	maximum 6/IOP
5	number of UCW		
	byte multiplexer channel	256	256
	block multiplexer channel	256	64
6	transfer speed		
	byte multiplexer channel	maximum 100	maximum 100
	block multiplexer channel (M bytes/sec)	maximum 3	maximum 1.5 (maximum 3)*

*high-speed block multiplexer channel

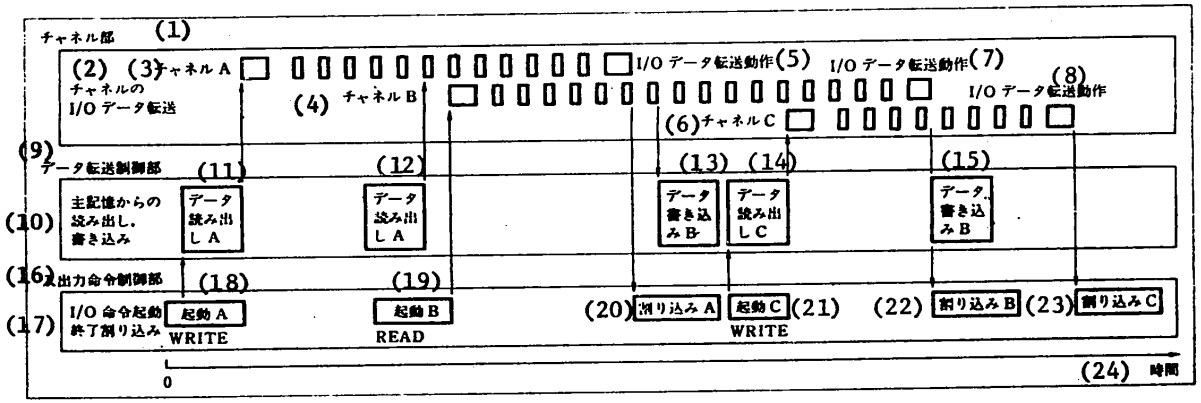
Channel Speed Acceleration by Independent Parallel Operation of Three Basic Units

For the acceleration of the channel operation speed and compaction of architecture, lead control and parallel control are required just as in processors. In a processor, as a basic concept, the instruction control unit, the arithmetic unit and the memory control unit, known as the three basic units, are designated to perform their respective functions independently in parallel for the enhancement of the speed.

Similarly, in IOP, the channel unit, the I/O instruction control unit and the data transfer control unit can perform their respective functions independently in parallel. While multiple channels of the channel unit are performing I/O interface data transfer operations in parallel, I/O instruction control can activate the next I/O instruction received and can execute interrupt handling of I/O operations already completed. Data transfer control can process data transfer requests from multiple channels one after another. Specifically, eight channels, I/O control and data transfer control can mutually overlap and operate. Figure 10 indicates the state of overlap operations.

Figure 10 shows the state of overlap operations in terms of the relationship of the respective operations to time, assuming that channels A and C execute writing into the I/O device (reading from the main storage) while channel B executes reading (writing into the main storage) from the I/O device after three channels, channel A, channel B and channel C, are activated.

Figure 10. I/O Processor Overlap Operation. This chart is an example of time relations and overlap operations of I/O data transfer in the channel, read/write to the main storage in the data transfer control and I/O instruction activation and end interrupt handling in the I/O instruction control. Activations A and C indicate I/O write instruction activation, and Activation B indicates I/O read instruction activation.



Key:

(1) Channel unit
(2) I/O data transfer of channel
(3) Channel A
(4) Channel B
(5) I/O data transfer operation
(6) Channel C
(7) I/O data transfer operation
(8) I/O data transfer operation
(9) Data transfer control
(10) read/write from the main storage
(11) Data read A
(12) Data read A
(13) Data write B
(14) Data read C
(15) Data read B
(16) I/O instruction control
(17) I/O instruction activation and interruption
(18) Activation A
(19) Activation B
(20) Interruption A
(21) Activation C
(22) Interruption B
(23) Interruption C
(24) Time

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In this manner, sufficient transfer capacity has been given to the present high-speed file magnetic disc unit with a capacity of 1260 M bytes/spindle and a data transfer speed of 3 M bytes/sec. As for the IOP throughput, the IOP has provisions for connecting even higher transfer capacity channels when a high-speed file is developed and I/O interface data transfer capability is improved in the future.

IV. Improvement of Semiconductor Element Technology

In conjunction with the above described logic system improvements, we decided to develop a new high-speed high-density LSI and to devise high-density packaging with it.

Assuming that the 1.3-1.6 performance improvement over the M-200H would be achieved basically by improving the machine cycles, a circuit speed goal and an integration goal for elements were determined. Assuming that an average delay/row of gates including wiring delay and loading delay is called a system delay, this system delay must be accelerated at least 1.3 times and more. If this can be achieved only by improving the gate switching time, the machine cycle improvement ratio "y" will be expressed as follows, where "a" is the percentage of gate switching time delay to the system delay and "x" is the switching time improvement level:

$$y = \frac{1}{(1-a) + \frac{a}{x}}$$

If a = 0.6 and y = 1.3, x = 1.6, which means an improvement of about 1.6 times is necessary. The machine cycle was improved from both angles: for LSI with maximum 550 gates, 60 percent acceleration was planned, and circuit delay time 0.7 ns was improved to 0.45 ns. Concurrently, packaging density was enhanced by admixing LSI with maximum 1500 gates to shorten the wiring delay, which contributes to the system delay.

Adoption of Three-Dimensional Packaging System Similar to the M-200H

The packaging system of the M-280H uses three-dimensional packaging which combines two types of substrates called package and backboard just as in the M-200H, with increased package density/capacity.

Figure 11 shows a large high-density substrate (package) of approximately 40 x 20 cm size for loading LSI and MSI. In the M-280H, as in the M-200H, LSI is admixed with MSI and SSI in consideration of gate-pin ratio (ratio of integrable number of gates to a given number of pins). In one package, a maximum of 20 LSI and 20 MSI and SSI can be packaged.

As a connector to connect this package to the outside components, a 50-mil (1 mil = 25.4 μm) pitch connector is used; 580 pins in all, combining front and back terminals, can be used. The substrate is composed of glass-epoxy and has a total of 10 conductive layers. The grid pitch is designated as 75 mils to enlarge the wiring capacity of each layer for the facilitation of high-density packaging.

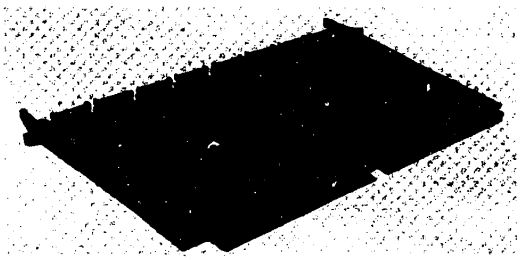


Figure 11. Package Loaded With LSI

The backboard is the substrate on which a package is housed. On one sheet of backboard, 24 packages can be housed as a standard. An entire backboard can house 50 K-200 K gates, and has a total of 18 conductive layers. The wiring capacity is upgraded compared to the backboard (14 layers) used in the M-200H.

Semiconductor Process Technology Improved From the Conventional 3 μm to 2 μm

The semiconductor technology used for the M-280H is in principle an improvement in speed or integration over that of the M-200H. However, the basic technology used in developing these semiconductors is markedly reformed from that of the M-200H.

To improve the speed and integration of semiconductors, the switching speed must be upgraded and the power must be downgraded by reforming the semiconductor process. The following semiconductor technologies were developed using the technologies reformed for this purpose--2 μm photolithography technology, dry-etching type microwiring technology, process technology such as three-layer wiring technology, and technology such as LSI automatic design system, LSI diagnostic system and test system.

1. Logic LSI

The logic LSI was improved in two different ways: 60 percent acceleration of the speed of the conventional 550 gate LSI without changing the number of gates; achievement of high-density packaging of logic with a better gate-pin ratio by a newly developed maximum 1500 gate LSI.

2. Logic-in Memory Element

As a new logic-in memory element, an element which can house a 6144 bit memory and a 770 gate logic circuit was developed. The integration of this element is almost double that of the M-200H. Since this logic-in memory element is called IA (index array), we will refer below to the one developed for the M-200H as IA 1 LSI and the one developed at this time as IA 2 LSI.

3. High-Speed Bipolar Memory Element

A new high-speed (access time 7 ns) and high-integration (4 K bit) bipolar memory element was developed as a memory element to be used for buffer storage and control. This memory has the same access time but is integrated four times better than that used for the M-200H.

4. Main Storage Use 64 K Bit n MOS Memory Element

As a memory element to be used for main storage, a 64 K bit memory element was developed. The capacity of the main storage was upgraded by designing to have virtually the same access time as the 16 K bit memory used in the M-200H with this memory packaged in the main storage. Tables 3 and 4 show specifications of logic and high-speed memory.

Table 3. Comparison of Logic LSI of the M-280H and the M-200H

Item		M-280H	M-200H
1500 gate LSI	number of gates	maximum 1500	
	circuit speed	0.8	
	number of pins	108	
	average power (W)	3.5	
550 gate LSI	number of gates	maximum 550	maximum 550
	circuit speed	0.45	0.7
	number of pins	108	108
	average power (W)	3.3	3.3

Table 4. Comparison of Logic-in Memory and High-Speed Bipolar Memory

Item		Element Developed for M-280H	Element Developed for M-200H
logic-in memory element	number of memory bits	6144	3072
	number of gates	770	470
	memory access time (ns)	6.7	6.7
	average power (W)	5.2	3.9
bipolar memory element	number of memory bits	4096	1024
	memory access time (ns)	7	7
	average power (W)	1	0.8

1500 Gate Masterslice LSI Packaged in the Same Package as the 550 Gate LSI

While a process with a 3 μm miniaturization was used for the 550 gate LSI of the M-200H, the miniaturization was further advanced for the high-speed 550 gate LSI of the M-280H by designating 2 μm as the smallest size emitter. Consequently, speed was accelerated from 0.7 ns/gate to 0.45 ns using virtually the same circuit current. Besides the miniaturization of transistors, the chip size was also reduced to two-thirds in terms of area ratio, from 5.7 mm square to 4.5 mm square, by reducing the aluminum wiring width and span. This size reduction increased the number of chips to be obtained from a wafer of identical size.

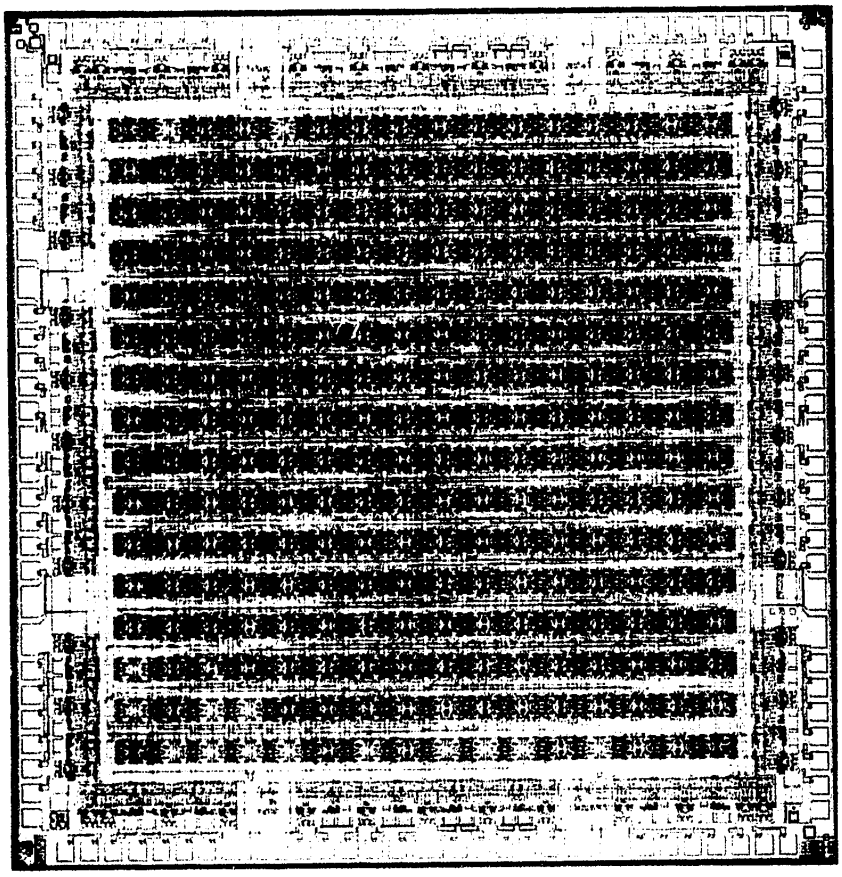
On the other hand, a maximum 1500 gate masterslice model gate array LSI was developed using the 2 μm process for the achievement of high integration.[10] A photo of this chip is shown in Figure 12. This LSI uses a high-speed ECL system just as in the 550 gate LSI. Its power voltage is -4.5V and there are 88 external input/output pins, which are packaged on the same 108 pin flat package.[8] The basic circuit is composed of three input OR/NOR. Wired/OR and Correct/AND are manipulative and can be used as logic gate equivalents, contributing to the higher density of the logic gates. One block is constructed with these four basic circuits, and this block is lined vertically and horizontally in a matrix, with the wiring channels running between the matrix.

An automatic layout and automatic wiring program handles gate layout and integrate wiring. If the wiring channel capacity is too small, it takes too much computer time for layout and wiring and it may take design time for manual wiring in case the unwired space is left to the end. On the other hand, if the wiring channel capacity is too large, the chip size will increase. The optimum number of channels was determined based upon the results of the 550 gate LSI, and 1500 gates were successfully integrated on a 5.8 mm square size chip. The reduction of the chip size leads to reduction of costs and allows the use of the same LSI package as the 550 gate LSI.

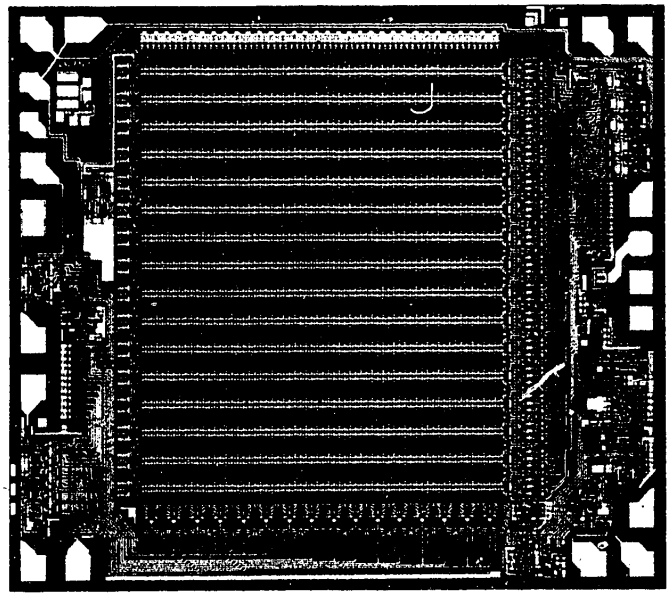
The automatic layout and automatic wiring programs were remodeled for use in the 1500 gate LSI; they can complete layout and wiring virtually within the same time as in the 500 gate LSI.

In order to package the 1500 gate LSI, which is three times more integrated than the conventional LSI, while holding down the electric consumption to the same level on the same package, the following innovations were made. Specifically, the current of the basic circuit was reduced to one-third that of the 550 gate LSI, but the on-load activation current was set at two-thirds. Furthermore, compared to the conventional two-layer wiring on the chip, a three-layer wiring technology was developed at this time; the power wiring was transferred to the third layer while the logic wiring was installed on the first and second layers. In addition to this arrangement, the wiring pitch was 30 percent more densified. The power current is the same as with a 550 gate gate LSI, so that the latest LSI can be used jointly with the former LSI.

In using LSI, a 1500 gate LSI is used for the logic with a good gate-pin ratio, and a 500 gate LSI is discriminately used for other irregular logic. This proper use of LSI resulted in an increase in packaging efficiency, improvement in total system packaging density and shortening of machine cycles.



(b)



(a)

Figure 12. Pictures of the Conventional 550 Gate LSI (a) and 1500 Gate LSI (b)

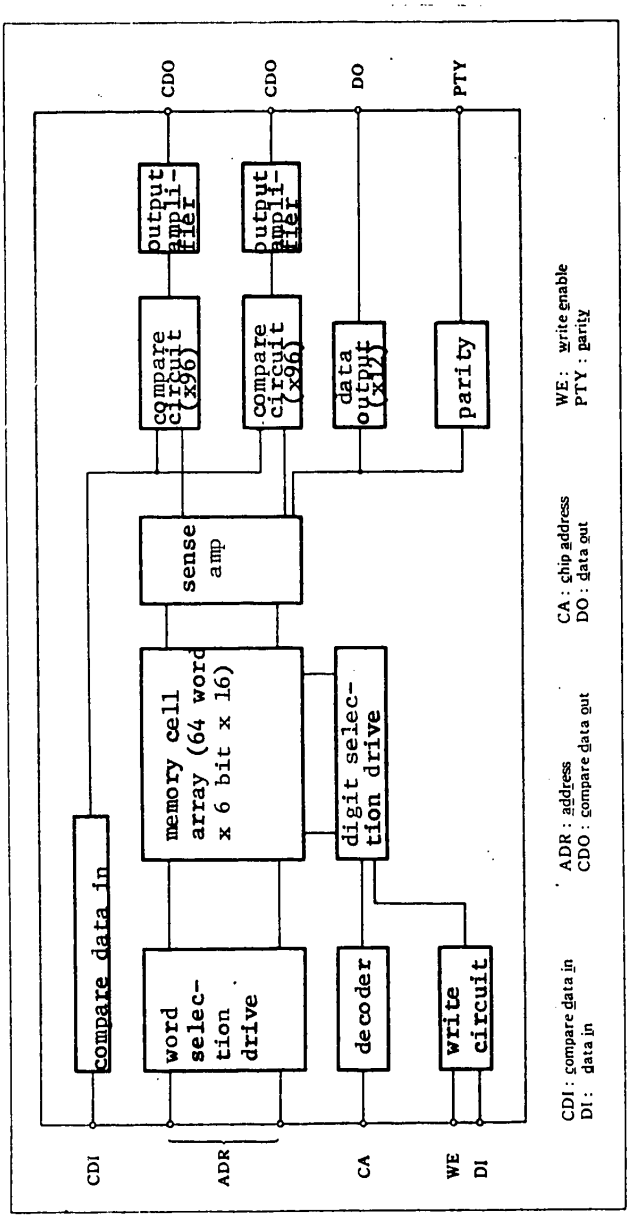


Figure 13. Internal Block Chart of IA 2 LSI. The IA 1 has 64 word x 6 bit x 8 memory cells and 48 compare circuits, while the IA 2 has two each: 64 word x 6 bit x 16 memory cells and 96 compare circuits.

Doubling the Number of Bits and Gates of Logic-in Memory Element

The logic-in memory element has a common use for the address translation buffer (TLB) and the buffer address array (BAA) of high-speed buffer storage (BS). In the M-200H, the memory array and logic were cut out and a 3072 bit and 470 gate IA 1 LSI was developed[11] so that this element could have common use for both a 256 column x 2 line TLB and a 64 column x 16 line BAA. In the M-280H, IA 2 LSI, practically the same circuit speed and doubled integration level was developed to facilitate the improvement of BS packaging density and to make provisions for future capacity expansion.[12] Figure 13 shows the internal block chart of an IA 2 LSI, and Figure 14 shows an example of its application to the BAA. This application method is the same as in application example[1] concerning the M-200H.

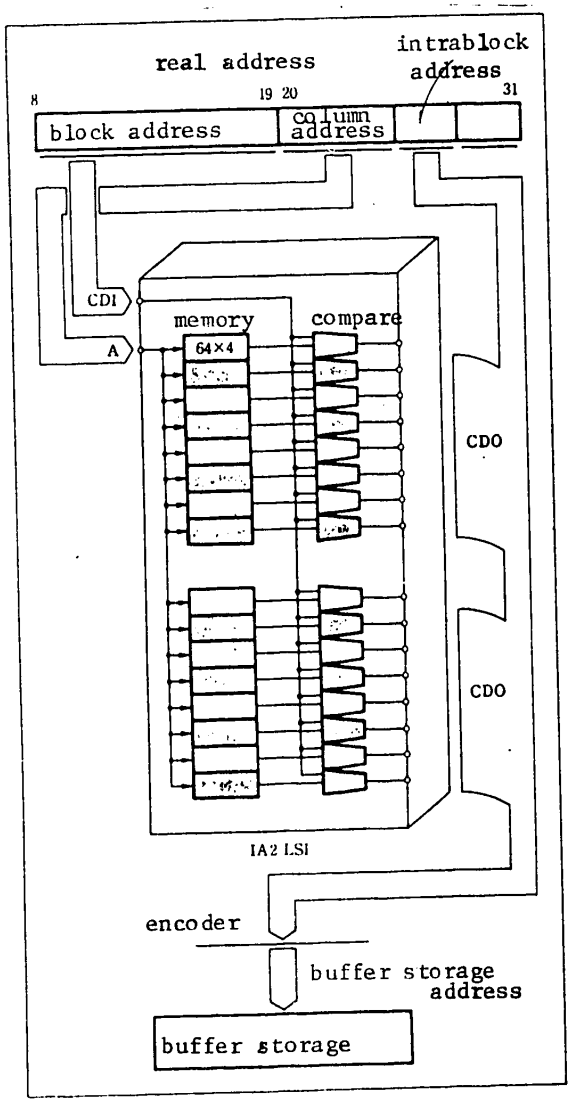


Figure 14. IA 2 LSI Example of Application to BAA (buffer address array). The dark box shows part added in IA 2.

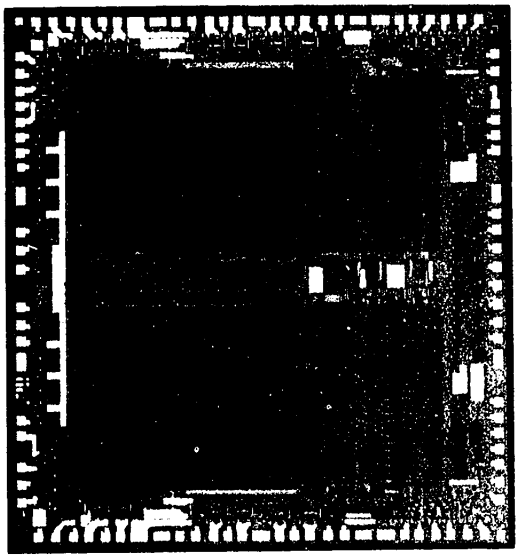
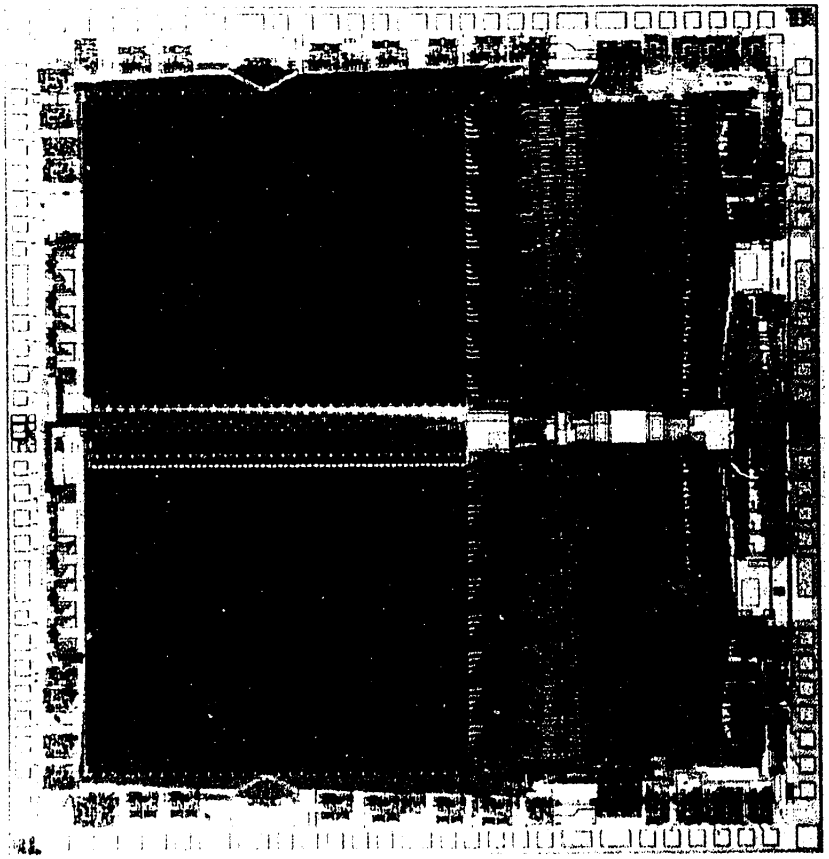


Figure 15. Pictures of IA 1 LSI (a) and IA 2 LSI (b).



The part shown in the dark box is added in the IA 2 LSI. Its speed is 6.7 ns in access time of the memory and 3.5 ns in access time of the compare circuit. This IA 2 LSI was packaged in the same 108 pin LSI package used for the previously described two types of masterslice model gate array LSI so that it could be admixed with logic LSI on the board. Figure 15 is a picture of the IA 2 LSI chip.

4 K Bit Bipolar Memory and 64 K Bit n MOS Memory

The 4 K bit bipolar memory used for buffer storage and control storage is manufactured using 2 μm process technology in common with the IA 2 LSI. This 4 K bit memory is interchangeable--maximum access time: 7 ns, power consumption: 1W, power current: -5.2V and input/output level: ECL 10K. For the package of the element, a 7.6 mm (300 mil) wide DIP (dual in-line package) is used in consideration of universality. Also, to improve the signal-to-noise ratio during high-speed operation, grounding pins were added on to 20 pins. Figure 16 shows a picture of the 4 K bit bipolar memory chip.

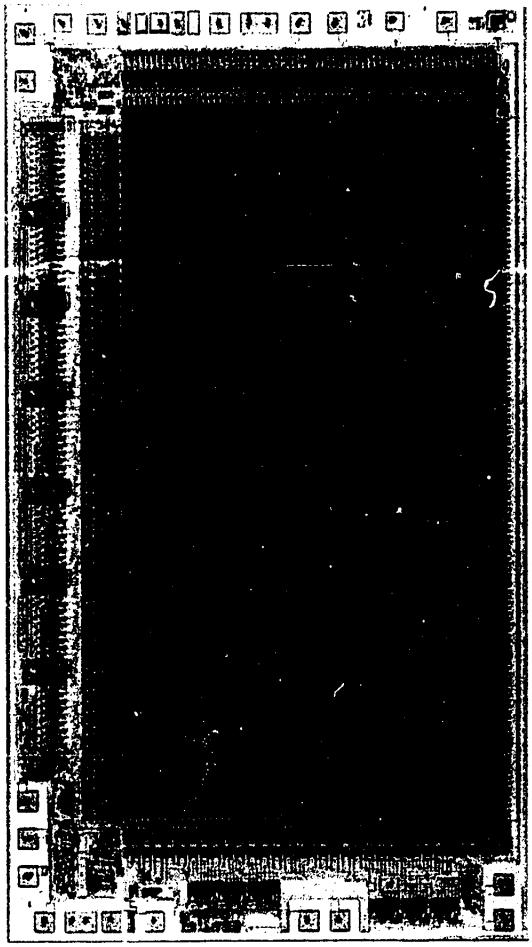


Figure 16. Picture of a 4 K Bit, 7 ns Bipolar Memory Chip

The IA 2 LSI and high-speed bipolar memory are designed to be sufficiently reliable even against alpha-ray obstacles. Generally, soft errors due to alpha rays are more liable to occur in proportion to the advancement in integration and speed of the memory. However, it is proven that the soft error ratio was held below 30 FIT (1 FIT: one defect out of 10^9 parts x time) according to operation results of the 1 K bit memory for the M-200H with provisions for countering alpha ray obstacles such as improvements in circuit technology, chip-coating and quality of packaging materials.[15]

In addition to this achievement, the 4 K bit memory, IA 2 LSI, which incorporates radiation instrumentation, quantitative analytic technology for uranium and thorium contained in very small amounts in packaging materials, high purity, high heat-resistance and improved flexible coating materials,[14] also realizes a soft error ratio equivalent to that of the 1 K bit memory.

The high-speed 64 K bit n MOS memory element used for the main storage unit is slightly slow in access time compared to the 16 K bit element. However, the overall performance of the main storage unit viewed from the storage control unit was made to be the same as when a 16 K bit was in use by using many of the previously described 550 gate and 1500 gate LSI in the peripheral logic of the memory and storage control for the compaction of the overall space. Figure 17 shows a picture of a 64 K bit n MOS memory element.

Complete Supportive Setup for Development

In the above, we have focused on the merits of the logic systems and system specifications and hardware technology that support them, comparing them with the M-200H.

A higher speed was achieved for the M-280H based upon the M-200H using high-speed LSI and high-integration semiconductors, and simultaneously it was designed to meet the needs for sophistication and versatility of the system by extending the framework of system specifications such as expansion of the main storage capacity and expansion of the connectable channels. These expansions of specifications also have much to do with the progress of the semiconductor technology.

Likewise, improvement and development of performance evaluation technology, design automation technology, logic verification simulation technology, circuit delay verification simulation technology, LSI RAM test technology and package diagnostic technology are important, in addition to the development of logic systems and hardware technologies for the development of a processor such as this. Fair and honest efforts to improve these technologies are the foundations for the development.

In conclusion, we would like to express our determination to make use of the technical experience obtained in connection with the development of the M-280H as resources for our future efforts to develop a better system.

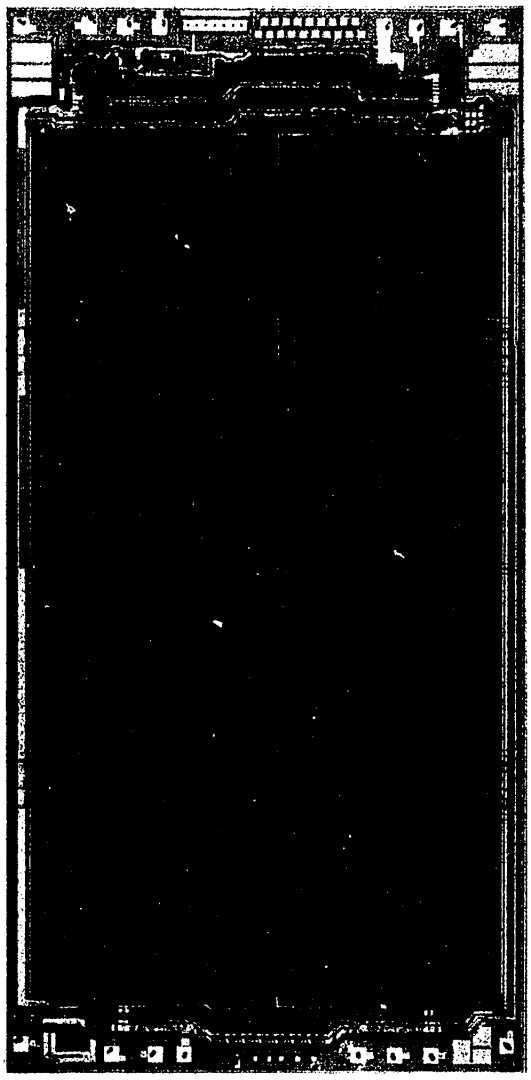


Figure 17. Picture of a 64 K Bit n MOS RAM Chip.

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SCIENCE AND TECHNOLOGY

OVERSEAS PETROCHEMICAL PROJECTS FACE DIFFICULTIES

Tokyo NIHON KEIZAI SHIMBUN in Japanese 18, 19 Mar 82

[18 Mar 82 p 7]

[Text] Overseas petrochemical projects, staked with rosy dreams are having a difficult time. Following the Iranian petrochemical business, which has become almost a "corpse," the Singapore petrochemical enterprise is faced with difficulty now that Mitsui Petrochemical Industry has expressed its desire to withdraw. The enemies of overseas projects include country risks sometimes, and inflated raw material and construction costs at other times. Difficulties which assembling and processing industries will never experience can crop up because of the sheer size of a project. However, overseas expansion is an unavoidable course for Japan's petrochemical industry, because it has a decisive handicap in the area of raw materials. Petrochemical [industry] circles are searching in earnest for the desirable format for overseas projects which can improve profits and reduce risks.

A Sigh Upon Withdrawal by Mitusi Petrochemical

"The inevitable has come." In late February, when it became known that Mitsui Petrochemical had decided to withdraw from the ethylene glycol (EG) undertaking, which is the nucleus of the Singapore petrochemical project, the leaders of industrial circles all sighed equally.

The Singapore petrochemical project was started in late 1971, before the first oil shock, upon the request of the Singapore Government to Sumitomo Chemical Industry for cooperation. The original plan was to use naphtha (crude gasoline) produced by Singapore's petroleum refinery base, which is one of the leading bases in the world, as the raw material and to produce a consistent series of petrochemical products, including ethylene, high-, medium-, and low-pressure polyethylene, polypropylene, and EG to be distributed over the Southeast Asian markets.

At that time, the project was supposed to be complete with three important conditions consisting of raw material, market and infrastructure. However, after the oil shock and the consequent rise in the cost of naphtha, which is produced from oil, it became clear that they could no longer compete with the U.S. and Canadian petrochemical industries, which use cheaper natural gas as

the raw material. Nevertheless, the project was pushed forward according to schedule. In 1975, a basic contract between the Singapore Government and Sumitomo Chemical Industry was signed, and in 1977 the project was upgraded as a national project The project was launched with a hidden Achilles heel--"high raw material costs."

Remaining Group Members Conduct Bitter Negotiations

On the other hand, the price of EG in the Southeast Asian market dropped to 120-130 yen per kilogram, thanks to the offensive launched by U.S. and Canadian products. In the case of the Singapore project, "160 yen per kilogram is the profit line, based on calculations that take into consideration the cost of raw materials and of plant construction. It cannot be lowered any further," (according to Mitsubishi Petrochemical, which participated in its EG enterprise). Under present circumstances, the Singapore petrochemical business must be prepared to lose if it wants to sell in the Southeast Asian market.

"We are already bearing the load of Iran Petrochemical and can bear no more overseas burdens," explained Naritada Tannawa, president of the Mitsui Petrochemical, to the other members of the consortium. But it is quite evident that a loss of confidence in the prospects for a profit on EG from the Singapore enterprise was the major motive for its withdrawal.

The members of the EG enterprise consortium that were left behind after the withdrawal by Mitsui--Mitsubishi Petrochemical and Nippon Shokubai Kagaku Kogyo, together with Sumitomo Chemical--began negotiations with the Singapore Government concerning stopgap measures necessitated by the withdrawal of Mitsui Petrochemical. The Singapore Government is reluctant to raise its contribution rate, however, and bitter negotiations continue.

Singapore was not alone in feeling the impact of the offensive launched by the petrochemical industry based on natural gas.

Korea Suffers From the Same Difficulty

Korea's Honam Petrochemical is a complex built in the Yosu area through a joint effort by Korea and the Mitsui group (Mitsui & Co, Mitsui Toatsu Chemical, Mitsui Petrochemical, and Nippon Petrochemical), which competed with its rival the Mitsubishi group and won the contract. The leading role played by this project in the modernization of the industry was much talked about. They went into commercial operation in the fall of 1979, but they are operating in the red today. The reason for this is the fact that its EG, one of the main products, cannot compete with U.S. and Canadian imports. Fiber products constitute an important part of Korea's exports, so the manufacturers are seeking cheaper raw materials in order to cut costs.

The raw material situation is just as serious in Korea as it is in Japan. So far, its ethylene costs approximately 200 yen per kilogram, which is higher than Japan's 170-180 yen. It is quite obvious that Korea cannot compete with U.S. and Canadian imports. At this juncture, the price of naphtha has dropped

somewhat, but the Japanese (Mitsui & Co.) are apprehensive about "whether this can become a decisive factor by which profits can be improved."

The Saudi Arabian Petrochemical enterprise participated in by the Mitsubishi group received an unexpected blow amid this worldwide relaxation in the demand and supply of oil and the consequent reduction in the cost of oil. All the participating members had expected to reap a plus-alpha profit, aside from the petrochemical business, from the bonus crude oil they are to get over a period of 15 years starting in 1986, when the petrochemical enterprise begins commercial operations, as a reward for their contribution to the development of the enterprise.

The irony of the matter is that the price of oil dropped rapidly in January when advance shipments of the bonus crude oil began. Crude oil whose GSP (official sale price set by the government) is lower than that of Saudi crude—such as Iranian crude and North Sea crude--has even appeared, so the situation that existed last summer, when the price of Saudi crude was lower than that of other crude, has been completely upset.

As a result, the advantage of "cheap Saudi crude" has been lost. The disappointment to the participating members has been especially great, because almost all participating members had counted on the profit they would get from the bonus crude to make up for the risks that go with projects in oil-producing countries. If the relaxed state of oil demand and supply persists, bonus oil can turn into penalty oil. Cries for help have been heard.

The greatest enemy of overseas projects used to be the country risk. The Mitsubishi group is still bogged down in the quagmire of the Iran Petrochemical project as a result of the Iranian revolution and war. In recent years, new types of difficulties, including the cost differential for raw materials, have begun to cast ominous shadows. The distress in petrochemical industry circles can only deepen.

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[Text] Since the year before last, petrochemical industry circles have been jostling around overseas expansion plans centered in the United States, Canada and Australia--including, for example, a Canadian and Alaskan petrochemical base project undertaken by the Mitsubishi group consisting of Mitsubishi Chemical Industry and Mitsubishi Corporation; a South Australiz petrochemical base project, jointly participated in by Asahi Chemical Industry and Mitsui Toatsu Chemical; and a vinyl chloride intermediate raw material project in Alberta, Canada, by Mitsui & Co. The aim of these projects is to use the abundant natural gas as a raw material and to produce basic chemical products and intermediate raw materials which will have a competitive edge in advanced nations where the political situation is stable.

Revised Feasibility Study

The IJPC (Iran-Japan Petrochemical) enterprise has shown us vividly the frightfulness of the country risk (the risk to the investment due to the host

country). Moreover, after two oil shocks, natural gas has become a cheaper starting raw material than naphtha (crude gasoline) refined from crude oil for the production of ethylene--from one-half to two-thirds cheaper, based on the cost of ethylene. It is quite natural that petrochemical industry circles would look to advanced nations with fewer risks and abundant natural gas.

Even these new ventures, however, are not without unexpected miscalculations. First of all, the crude oil price, to which the movement of the petrochemical products market and the raw material costs in Japan are directly tied, has dropped. Executive Director Kenjiro Oka of Mitsubishi Corporation, which is pushing ahead with a petrochemical base project in the province of British Columbia, Canada, lamented about his headaches: "We figured that the project was feasible if the price of crude oil went up to $60-$70 per barrel. But in reality, the price may dip below $30 per barrel, and construction costs are ballooning as a result of inflation. Therefore, even if the project is approved, we must reevaluate the feasibility study. The actual operation date must be pushed back further and further."

No matter how cheap the natural gas may be, it after all is only a portion of the total cost. Unless the movement of petrochemical products can be activated against the background of rising oil prices, there is no appeal to plunging further into development and import activities with huge investment sums. The Alaska project, which requires a much larger investment than the British Columbia project because its industrial base needs to be fixed first, has begun to be referred to as a "21st century project" in some sectors, so completion of this project has been pushed further into the future.

Red Ink Unavoidable for 5 Years

Whether or not the South Australia project undertaken mainly by Asahi Chemical Industry can take off depends in large measure on how many Japanese manufacturers of vinyl chloride are willing to participate and how much assistance the provincial government is willing to offer to fix the industrial base. There is no way of knowing whether or not the project can materialize.

The worldwide slump in petrochemical products and the recent situation whereby U.S. and Canadian chemical products can be imported cheaply are making it very difficult to implement new overseas projects. According to Mitsui & Co., which is making plans to manufacture vinyl chloride intermediate raw materials in Alberta, Canada: "Apart from trade in products, more and more enterprises are exercising caution when it comes to investing" (General Chemical Products Department): This is an indication of how difficult it is to implement a project.

Petrochemical industry circles have their hands full just coping with this unexpectedly severe domestic slump. Although petrochemical industry circles have begun to make preliminary moves to capture the natural gas of advanced nations, they cannot help but be cautious when they think of their own resources. Hiroshi Watanabe, executive director of Mitsubishi Chemical Industries, which is participating in Canada's British Columbia project and the U.S. Alaska project, revealed a cautious attitude when he said: "One must be

"prepared to operate in the red for the first 5 years, because overseas projects are so capital intensive. In contrast, nimble domestic facilities, which have been almost completely depreciated, can somehow weather it for a while, even if raw material costs happen to be high."

In the long run, however, Japanese petrochemical industry circles must follow the path of international production. The Industrial Structure Council, which is investigating relief measures for the petrochemical industry, has pointed out: "To expand into overseas regions where cheap raw materials and fuel are available to develop and import--these are the sole keys to survival for the Japanese petrochemical industry." Amid all this, a number of a new type of overseas expansion plans have attracted attention. These plans include a joint venture between Dow Chemical and four Japanese firms, including Kanegafuchi Chemical Industry, in Alberta, Canada, and a joint venture between Mitsui Toatsu Chemical and the U.S. Bistron Co.

"Toyota-type" Strategy Surfaces

The joint venture with Dow Chemical consists of separating the existing facilities of Dow Canada and absorbing them among the participating firms in order to supply vinyl chloride intermediate raw material to the four Japanese investor firms. The contract for the joint venture is expected to be signed by May. On the other hand, Mitsui Toatsu is to establish an acrylonitrile production base in the United States within 1-2 years by utilizing surplus facilities owned by Bistron, which is the chemical enterprise branch of the U.S. [firm] Standard Oil of Ohio. These projects are comparable to the "Toyota" strategy of utilizing existing GM facilities--unlike Nissan Motors, which is constructing a new plant in the United States on its own.

"If you buy an existing facility today, you can start operating tomorrow. There are no uncertainties related to construction, and there are fewer risks as well. Nor is there any need to bear the interest burden for a period of 2-3 years while construction is under way. Instead of building large-scale new plants, it is time for Japanese enterprises to go out into the world, and especially the United States, and put to good use those plants that are not in operation," declares the head of a large commercial firm.

In fact, in recent years many American enterprises have been approaching big Japanese petrochemical and commercial firms about plant sales. Participating in production is an existing facility or, to go one step further, purchasing existing plants seems to provide Japanese petrochemical industry circles with an effective strategy for realizing their overseas expansion plans.

Major Overseas Petrochemical Project Under Construction

Location	Participating Enterprises of Their Substitute	Products	Target Date
British Columbia Canada	Mitsubishi Corporation, Mitsubishi Chemical Industries, Mitsubishi Petrochemical, Asahi Glass Company, and three other Canadian firms	Ethylene, propylene caustic soda, vinyl-chloride intermediate raw material	1986
Alberta, Canada	Kanegafuchi Chemical Industry, Mitsui Toatsu Chemical, The Shin-etsu Chemical Industry, Mitsubishi Chemical Industries, Dow Chemical Canada	Vinyl chloride inter-mediate raw material	1985
Alberta, Canada	Mitsui & Co, Alberta Gas Chemi-cals, etc.	Caustic soda, vinyl chloride intermediate raw material	1985
Alaska, U.S.	Mitsubishi Corporation, Mitsubishi Chemical Industries, Dow Chemical, Shell Chemical, Du Pont, etc.	Ethylene, propylene, and various other derivatives	1985
Texas, U.S.	Mitsui Toatsu Chemical, Bistron	Acrylonitrile	April
South Australia, Australia	Asahi Chemical Industry, Mitsui Toatsu Chemical, CRA, etc.	Ethylene, caustic soda. vinyl chloride inter-mediate raw material	1986
Atjeh, Indonesia	Exxon Chemical, Pertamina, Tonen Petrochemical, Asahi Glass Com-pany, etc.	Ethylene, polyethylene, caustic soda, vinyl chloride intermediate raw material	1988

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