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USSR Report

ELECTRONICS AND ELECTRICAL ENGINEERING

(FOUO 5/82)

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USSR REPORT

ELECTRONICS AND ELECTRICAL ENGINEERING

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AEROSPACE & ELECTRONIC SYSTEMS

UDC 629.7:621:396.022

OPERATION OF AIRPORT AND AIR ROUTE RADIO EQUIPMENT

Moscow EKSPLUATATSIYA RADIOOBORUDOVANIYA AERODROMOV I TRASS in Russian 1981 (signed to press 10 Dec 80) pp 2,5, 223-224

[Annotation, author's foreword and table of contents from book "Operation of Airport and Air Route Radio Equipment", by Al'bert Andreyevich Kuznetsov and Viktor Ivanovich Dubrovskiy, Izdatel'stvo "Transport", 6000 copies, 224 pages]

[Text] Annotation

This book examines the organizational structure of civil aviation subdivisions involved in operating airport and air route radio equipment, and provides a brief description of the basic types of such equipment. Questions involved in technical and economic planning and organizing the maintenance and repair of radio equipment are explained, and basic information is provided on the acquisition and processing of reliability data. Radio equipment integrity testing methods are explained briefly.

The book is intended for engineering and technical personnel involved in technical operation of air traffic control systems and facilities, and may also be useful to students in graduate civil aviation institutes. 74 illustrations, 17 tables, 26 bibliographic references.

[This book was reviewed by V.S. Novikov.]

Author's Foreword

Efficiency and flight safety in civil aviation are determined to a great extent by the level of development and operating reliability of radio navigation and air traffic control equipment. Civil aviation today has numerous airports within whose zones pass more than 1000 aircraft* per day. Sophisticated air traffic control systems and facilities are needed under conditions of such heavy traffic; therefore, operating aviation enterprises are equipped with route and dispatcher radars, secondary radar facilities, television signal conversion equipment and other technology. Active work is under way on creating and introducing the "Start", "Start-2" and "Terkas" automated air traffic control systems.

Nonetheless, as more complicated air traffic control systems and facilities are put into operation, the amount of production and operating expenses for maintenance and repair increase sharply, and the requirements for air traffic control efficiency and system operating reliability are heightened.

The continuing improvement of air traffic control systems and facilities leads to a quantitative and qualitative change in the engineering and technical staff using it. Furthermore, if we consider that air traffic control system and facility operating costs are nearly as high as the equipment cost, the problem of increasing reliability in reducing operating costs becomes urgent.

The organization of the operation of air traffic control systems and facilities must facilitate the highest possible operational readiness, which is achieved by a high level of organization and by using modern forms and methods of maintenance.

Sections 2.3-2.5 were written jointly by the authors and engineer Yu.G. Kuznetsov, and engineer V.K. Pechenezhskiy participated in writing section 2.6.

*Aircraft is taken to mean both airplanes and helicopters.

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6900
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ELECTRONIC DEVICES FOR SHIPBOARD AUTOMATION

Leningrad ELEKTRONNYYE USTROYSTVA SUDOVOY AVTOMATIKI in Russian 1981 (signed to press 23 Jul 81) pp 2-4, 238-242, 247-248

[Annotation, foreword, table, and table of contents from book "Electronic Devices for Shipboard Automation", by Boris Sergeyevich Taratorkin, Izdatel'stvo "Sudostroyeniye", 4400 copies, 248 pages]

[Text]

Annotation

This book examines the operating principles of solid-state instruments used in shipboard automation devices, as well as construction principles, operating processes and characteristics of analog pulsed and digital circuits used in electronic automation. A great deal of attention is devoted to TTL circuits, combinatory and sequential devices.

The book is intended for students at higher ship-building schools in specialty 0649. It may also be useful to engineers specializing in the area of electronic automation and information-measurement technology, as well as a wide group of radio amateurs who are acquiring expertise in logical microcircuit engineering.

[This book was reviewed by Candidate of Technical Sciences Yu.N. Afanas'yev, Automation Department, Leningrad Institute of Water Transport.]

Foreword

This book is a teaching aid for studying the first part of the course on "Electrical Elements and Devices for Automation" taken by students in specialty 0649 at higher ship-building schools.

The education of a modern engineer working in the area of automating shipboard power installations, individual mechanisms and systems is incomplete without mastery of the operating principles and devices used in electronic elements and circuits for automation. Scientific and technical progress in the area of electronics and automation manifests itself in an unceasing expansion of the types of discrete solid-state devices and integrated circuits, improvement of their properties and capabilities and in the appearance of a series of devices which are new in principle. In contrast to certain other areas of technology, new technical devices do not so much replace existing devices, as was the case with transistors which have replaced electron tubes almost everywhere, as they expand the capabilities of automation facilities by finding specific areas of application. For example, the logic microcircuits which have appeared over the past 10 years have begun to play a dominant role in discrete control automata, narrowing insignificantly the use of low-power and power transistors and other solid-state devices in various types of actuating circuits, in electrohydraulic and electromagnetic mechanisms, in sensors, measuring circuits, etc. This singularity of electronic technology produces a wide spectrum of electronic elements and devices now used for shipboard automation which are gradually proving their advantages in practice over various mechanical, pneumatic and hydraulic devices for controlling objects aboard ships.

Since the operating principles of complex microelectronic devices can be understood only on the basis of a preliminary study of their component elements and characteristic circuit arrangements, the present book examines an extremely broad group of electronic instruments and circuits, starting with diodes and ending with logical automata using microcircuits.

Appendix

Technical Data for Most Widely Used Series K155 Microcircuits

Function and brand	Maximum input current, mA	Maximum output: Current mA	Maximum output: Voltage V	Maximum current mA (Power)	Maximum power, mW (Power)	Number of outputs: Power +5 B	Number of outputs: Power 0 B	Number of outputs: Inputs	Number of outputs: Outputs
4 (2NAND) K155LA3	–1,6	16	5	—	78	14	7	1, 2 4, 5 9, 10 13, 12	3 6 8 11
4 (2NAND) with open collector K155LA8	–1,6	16	15	18	79	14	7	2, 3 5, 6 8, 9 11, 12	1 5 10 13
3 (3NAND) K155LA4	–1,6	16	5	—	60	14	7	1, 2, 13 3, 4, 5 9, 10, 11	12 6 8
2 (4NAND) with power output K155LA6	–1,6	30	5	—	92	14	7	1, 2, 4, 5 9, 10, 12, 13	6 8
8NAND K155LA2	–1,6	16	5	—	21	14	7	1, 2, 3, 4, 5, 6, 11, 12	8
6 (NOT) K155LN1	–1,6	16	5	—	173	14	7	1, 3, 5, 9, 11, 13	2, 4, 6, 8, 10, 12

Function and brand	Maximum input current, mA	Maximum output		Maximum current mA	Maximum power, mW	Number of outputs			
		Current mA	Voltage, V	Power		Power		Inputs	Outputs
						+5 В	0 В		
4 (2AND) K155LI1	—1,6	16	5	33	—	14	7	1, 2 4, 5 9, 10 12, 13	3 6 8 11
4 (2OR) K155LL1	—1,6	16	5	33	—	14	7	1, 2 4, 5 9, 10 12, 13	3 6 8 11
2—2—2—2AND-4NOR with OR expansion K155LR3	—1,6	16	5	—	47	14	7	1, 13; 2, 3; 4, 5; 9, 10	12 (*K*), 11 (*Э*), 8 ($\bar{Q}$)
8AND-OR - expander K155LD3	—1,6	—	—	—	20	14	7	1, 2, 3, 4 5, 6, 8, 13	12 (*K*), 11 (*Э*)
Two Schmitt triggers with 4NAND logic K155TL1	—	—	5	32	—	14	7	1, 2, 3, 4 9, 10, 12, 13	6 ($\bar{Q}$) 8 ($\bar{Q}$)
Four D-flip-flops K155TM5	—	16	5	53	—	4	11	1, 2, 5, 6 (*D*) 12, 3 (*C*)	14, 13, 9, 8
TT-flip-flop with 3&J-3&K logic K155TV1	—3,2	16	5	105	105	14	7	3, 4, 5 (*J*); 9, 10, 11 (*K*); 13 ($\bar{S}$); 2 ($\bar{R}$); 12 (*C*)	8 (*Q*), 6 ($\bar{Q}$)
Univibrator with 2NOT-1-2AND input logic K155AG1	— (1,2≤*R*≤40 KΩ, *C*≤4000 µf)	16	5	40	—	14	7	11—14 (*R*); 11—10 (*C*); 3, 4 ($\bar{S}$); 5 (*V*)	6 (*Q*), 1 ($\bar{Q}$)
Decade counter (2×5) K155IYe2	—6,4	—	5	53	—	5	10	6, 7 (& *R*); 14 (*T1*), 1 (*T2*)	12, 9, 8, 11
Binary counter (2×8) K155IYe5	—3,2	16	5	53	—	5	10	2, 3 (& *R*); 14 (*T1*); 1 (*T2*)	12, 9, 8, 11
Binary-decimal decoder K155ID1	—3,2	7	60	25	132	5	12	3, 6, 7, 8	16, 15, 8, 9, 13, 14, 11, 10, 1

Function and brand	Maximum input current, mA	Maximum output		Maximum current, mA	Maximum power, mW	Number of outputs			
		Current mA	Voltage, V	Power		Power		Inputs	Outputs
						+5 B	0 B		
Four-bit shift register K155IR1	—3,2	16	5	82	—	14	7	7, 6 (*V*); 8, 9 (*C*); 2, 3, 4, 5(*D*)	13, 12, 11, 10 (*Q*)
Two-bit summator K155IM2	—	—	5	58	—	4	11	2, 14 (*A*); 3, 13 (*B*); 5 (*P*)	1, 12 (*S*); 10 (*P*)
Eight-channel switch K155KP5	—0,6	—	5	43	230	14	7	5, 4, 3, 2, 1, 13, 12, 11 (*D*); 10, 9, 8 (*S*)	6 ($\overline{Q}$)
Sixteen- bit operational memory K155RU1	—11	0,25	5	—	—	14	7	5, 6, 7, 8 (*Y*); 3, 2, 1, 14 (*X*); 9, 13 (*W*)	11, 12 ($\overline{Q}$)
1024-bit read-only memory K155RE21	—1	0,1	—	130	—	16	8	15, 1, 2, 3, 4, 5, 6, 7 (*D*); 14, 13 (*F*)	12, 11, 10, 9 (*Q*)
BCD-to-binary code converter K155PR6	—1	0,1	5	104	—	16	8	10, 11, 12, 13, 14 (*D*); 15 (*F*)	1, 2, 3, 4, 5, 6, 7, 9 (*Q*)
Binary-to-BCD converter with open collector K155PR7	—1	0,1	15	104	—	16	8	10, 11, 12, 13, 14 (*D*); 15 (*F*)	1, 2, 3, 4, 5, 6, 7, 9 (*Q*)
Arithmetic-logic device K155IP3	—	—	5	—	—	Casing with 24 outputs			

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BROADCASTING, CONSUMER ELECTRONICS

UDC 621.382.8

CHARGE-COUPLED-DEVICE IMAGERS

Moscow FORMIROVATELI VIDEOSIGNALA NA PRIBORAKH S ZARYADOVOY SVYAZ'YU in Russian 1981 (signed to press 28 Aug 81) pp 2-5, 105-131, 136

[Annotation, foreword, chapter 5, conclusion and table of contents from book "Charge-Coupled-Device Imagers" by Feliks Pavlovich Press, Izdatel'stvo "Radio i svyaz'", 10,000 copies, 136 pages]

[Text]

Annotation

This book examines the operating principles of imagers based on charge-coupled devices. Constructions of linear and matrix imagers are given, and attention is devoted to questions of the technology and utilization of CCD imagers.

The book is intended for engineers involved with the development and application of charge-coupled devices.

[This book was reviewed by Doctor of Technical Sciences Yu.R. Nosov and Candidate of Physical and Mathematical Sciences V.V. Kolotkov]

Foreword

The idea of charge-coupled devices (CCD) appeared in 1969, when work was underway on creating a solid-state magnetic-bubble memory analog [1]. The fact that this work provided the impetus for the appearance of a new type of device can be considered random; the basic reason and motive force consisted of a continuing trend toward processing increasing amounts of information. Increasing the amount of information requires the development of reliable devices with a high degree of integration. The integrated circuits which were known in 1970 were based on p-n junctions, regardless of whether the p-n junction was part of a bipolar or MOS transistor. From the viewpoint of increasing degree of integration and operating reliability, p-n junctions are far from ideal: they take a lot of space, require the connection of contacts, and each p-n junction performs potential-charge conversion and back, which is characterized by some ambiguity. This ambiguity results from the spread between the technological and operating conditions; for this reason, when the number of p-n junctions is increased, information processing performance is unavoidably degraded.

The elements in charge-coupled devices are not made of p-n junctions, but rather more compact MOS-capacitors. The primary fundamental distinction of the CCD was the implementation of the principle of "localized charge transmission by manipulating electrical potentials" [2]. Localized charge (charge "packet") transmission means that information processing does not require that the potential be converted to a charge and back. This conversion is done only at the input and output of the device. Information charge packets are formed at the input of the CCD by the action of light or by charge conversion of the p-n junction potential. By changing the electrical bias, these charge packets are then transferred unchanged from one MOS-capacitor to the next. The charges which were input to the CCD reach the output, where they are converted to potential or current. This principle is simple, elegant and ideally permits high quality information processing. For example, the dimensions of the MOS-capacitors may differ, but if the charge packets do not cause the capacitors to overflow, the spread in the dimensions has no effect on the transmission of information. The absence of a set of p-n junctions and individual contacts, as well as the small areas of the MOS-capacitors, increase the degree of integration: from the moment they appeared, CCD became the largest integrated circuits. If the maximum degree of integration in bipolar and MOS circuits is approximately 10^4 cm^{-2}, this figure reaches 10^5 cm^{-2} in CCD. The power required for information processing in CCD is also an order of magnitude lower than for other integrated circuits: $5 \cdot 10^{-6}$ W/bit.

From almost the very appearance of CCD, three basic areas of application were defined: video imagers, memories and analog information processing devices. The present book examines video imagers: readers who are interested in other types of CCD can find information about them in [3-5]. CCD imagers permit the conversion of an optical image to a sequence of electrical video pulses, replacing television vacuum transmitting tubes such as vidicons.

Over the past 20 years, radioelectronics has been extensively affected by microminiaturization; it is now difficult to imagine a computer or receiver which uses tubes rather than semiconductors and integrated circuits. Television is one of the last remaining areas which uses vacuum devices. Of course, electronic television equipment has long used integrated circuits, but the basic part of any television camera - the imager - is a vacuum device, which is rather cumbersome and requires a heated cathode and a complicated system for controlling the electron beam. Attempts to create a solid-state analog for the transmitting television tube in the form of a photoresistive, photodiode or phototransistor matrix [6] have not met with success, since the operation principle and complex technology made it impossible to obtain a number of elements comparable with tubes. Only the invention of the CCD has brought this idea to reality.

A modern solid-state vidicon analog using CCD is a sheet of silicon about the size of a small postage stamp. The sheet holds several hundred thousand miniature MOS capacitors (each element is approximately 20 x 20 μm^2). An optical image is projected onto the surface of the imager by means of a lens. The photons absorbed by the silicon cause electron-hole pairs to be generated, and the minority carriers from these pairs are accumulated in the MOS capacitors. The amount of charge accumulated in a given well (imager element) is proportional to the number of photons striking that area, i.e., the local illumination. The result is the formation of a charge distribution which duplicates exactly the distribution of illumination in the optical image. By changing the bias on the electrodes of the MOS capacitors, the charges are then moved serially to the output of the imager, thus providing electron scanning. The video pulses which are output are amplified and used to modulate the electron beam in the kinescope. The movement of the beam is synchronized with the movement of the CCD charges, and the picture which was projected on the surface of the imager is drawn sequentially, line by line, on the screen of the kinescope. CCD imagers have a number of important advantages over vacuum tubes. Size and weight are reduced by approximately an order of magnitude, and service life and mechanical strength are increased significantly. No high-voltage power supply, heated cathode, or deflection and focusing system are required. Valuable new properties appear which tubes cannot provide, e.g., high geometric accuracy of the image, absence of dispersion, close coordinate agreement and lack of lag.

This book will acquaint the reader with the operating principles of CCD imagers, the basic types of imagers and their characteristics, methods of constructing and manufacturing devices, the use of imagers in various types of television equipment, and the prospects for further development of CCD. It seems to us that this broad approach to the problem responds to the tasks of the present series, since the book may also be useful for both developers and users of CCD imagers.

5. Imager Application

Imagers are being developed at high rates unusual even for solid-state microelectronics. Only 18 months elapsed from the time of the physical idea, proposed in 1970, to the first experimental television camera using a 128 x 128 matrix. During 1971-1975, military and space organizations in the US (NASA, USN, USAF) concluded major contracts with leading firms working on imager development such as Fairchild, RCA and General Electric. This provided the impetus for imager development, and determined the basic area of their application - special-purpose military and space equipment. The use of imagers in place of vidicons reduces dimensions, weight and power consumption by one or two orders of magnitude, i.e., provides a gain in those parameters which are especially important in on-board equipment. The high cost of imagers (the large-format CCD-221 imager costs more than $3500, and the medium-format CCD-221 costs about $900), coupled with the low percentage of production of good articles, has frightened the developers of industrial and domestic equipment, but is not generally important for military developers because the advantages of the imagers compensate for the cost. Specific singularities of imagers, in contrast to vidicons, include a rigid geometric raster, practically lag-free operation and a low-noise output. It is sufficient to note that the appearance of a hard-raster imager has made it possible to create a guidance system with characteristics which could not be achieved earlier using vidicons.

The use of imagers in applied as well as broadcast television is being delayed by difficulties in producing matrix imagers with 5×10^5 cm^{-2} elements, i.e., large-format matrices. Television cameras with medium-format matrices, both foreign [62, 66] and domestic [63-65], are now being used in industrial television systems, video telephones, various types of testing and monitoring equipment, for production automation, etc.

Color television using imagers is being developed rapidly in Japan. The first report of a joint Japanese-American development of a color television camera using medium-format matrices (288 x 244 elements) appeared in 1975. By 1979 color television cameras compatible with the television standard had been developed by two leading companies in Japan (Sony and Toshiba). Sony expects to reduce the price of a CCD color television camera to $400-800 in mass production [66]. In this case, we can expect wide domestic use of CCD-imager cameras, where they will replace ordinary photographic and movie equipment.

It must be noted that imager developers in Japan are going their own way: without increasing chip size (in order not to reduce the output of good articles), they are increasing the resolution to the level required by the TV standard with the help of special construction and circuit engineering treatment, specifically using the spatial shift method.

Having acquainted ourselves briefly with the general situation in the area of imager application, let us now consider specific developed equipment models (according to foreign and domestic literature between 1973 and 1979). Figure 59 shows a general diagram of the areas of application of imagers.

Military equipment. One of the first imager applications was an aircraft video reconaissance system [67]. A 1600-element linear imager was installed along the axis of the aircraft, and a rotating four-faceted prism formed the scan band. The video data were transmitted to the command point by a television transmitter.

The USAF then used a miniature camera with a linear CCD-121 imager containing 1728 elements. This camera was designed for real-time transmission of video information from low-altitude low-speed aircraft or manned rockets.

The use of mechanical movement of the prism in order to increase the viewing angle reduces system reliability. Systems containing no moving parts, in which a wider view is achieved by using wide-format lenses, are being developed in parallel with these systems. The resolution of the photosensitive element is increased through hybrid assembly of the linear imager. For example, [23, 67] report the development of high-resolution wide-format video systems using three CCD-101 linear imagers (1500 elements) and nine CCD-121 imagers (1728 elements). The total number of expansion elements in the photodetection section can thus be as high as 15,000; in order to have such a "super receiver", it is necessary to use complex, cumbersome objectives with a wide working field and low distortion. The Fairchild Company is developing an aerial reconnaissance system which proposes the use of a two-row collection of 9 or 10 CCD-121 linear imagers and a 140° lens; the size of the lens is only 30 cubic inches (this is pointed out as an achievement, since lenses are usually large, e.g., with lengths of up to 0.9 meters) [67]. The resolution of the system is 0.3 meters through an angle of 120° at an altitude of 65 meters. There are also plans for multi-lens aerial

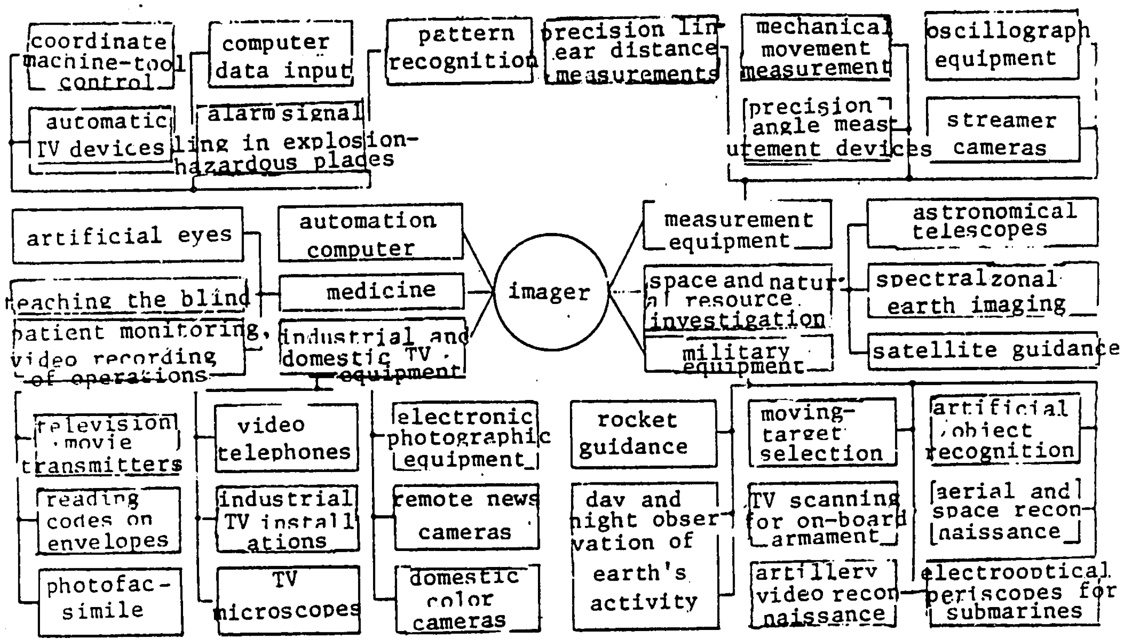

Figure 59. Areas of imager application

reconnaissance devices. RCA and Bourns Inc. are competing in the development of a wide-aperture camera using a Fairchild imager. The RCA camera is based on a standard photographic camera which uses 35-mm film. Each of five lenses projects the image of its own strip on the ground onto five CCD-121 linear imagers containing 1728 elements. The camera is designed to cover a 140° field of view, which corresponds to a strip 1.6 km wide on the ground with the aircraft flying at 300 meters [68].

One shortcoming of video systems using linear imagers in the short accumulation time, so that they can only operate during the day when the illumination is sufficient. This shortcoming can be overcome by using matrix-imager video systems operating in the usual frame storage mode or storage and hold mode.

The MV-250 television camera which uses 244 x 190-element CCD-211 matrix imagers is being utilized in the development of on-board video systems. A design for mini-class piloted rocket equipment with a large-format camera using a CCD-221 matrix (448 x 380 elements) has been reported [69]. The matrix in the television camera is cooled by a miniature cooler. Besides this camera, which works in daylight, an analogous device is being developed in which the matrix is coupled by means of fiber optics to an optical amplifier. The amplifier (of the electron-optical converter type) uses a luminophor which converts the original wide-spectrum image to a uniform image with a narrow spectral interval which coincides with the maximum sensitivity of the imager.

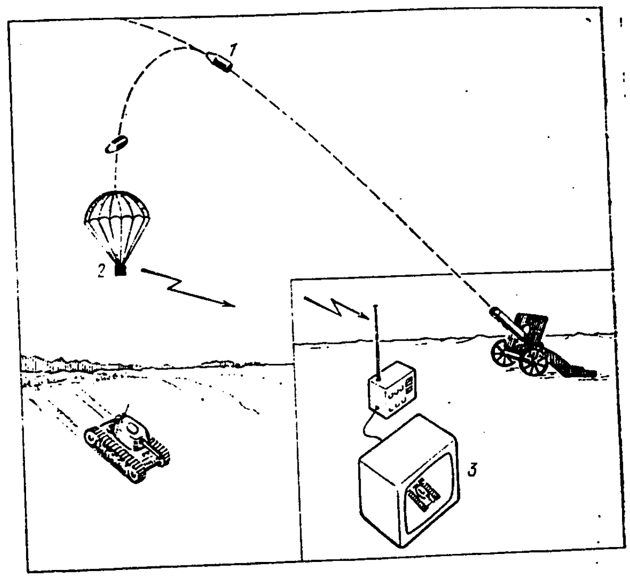

Figure 60. Use of imager in artillery video reconnaissance system: 1--projectile; 2--CCD camera and transmitter; 3--command point.

The unique version of video reconnaissance is provided by a system which delivers the television camera to the required area by means of an artillery projectile (figure 60). The head containing the camera is released from the projectile at the required altitude and dropped by parachute. The transmitter, which is carried along with the camera in the head of the projectile, sends an image of the terrain to the command point in real time. This system, developed by the Fairchild Company, is based on a 155-mm artillery star shell. The camera uses a CCD-211 matrix (244 x 190 elements). "The reality of creating such a system," assert the developers, "is provided only by the use of CCD; a vidicon cannot withstand the 12,000-15,000 g loads which occur at the firing moment" [70]. A prototype camera using a 100 x 100 matrix has been tested under actual conditions: after being fired with acceleration of 8,000 g and ballistic flight lasting 15 seconds, the camera separated and transmitted an image for 100 seconds while being dropped by parachute [70].

The hard geometric raster of imagers is attracting guidance and orientation system developers. There are plans to install a miniature camera using a CCD-221 matrix imager on the stabilized platform of guided air-air missiles [69]. Information about the position of the target within the field of view of the camera is input to a feedback circuit to correct the missile flight. The camera is powered, and the signals processed, by an electronic unit outside the platform. Preliminary bench tests have indicated that the guidance unit can track flying objects without losing the target even when other bursts are present.

The moving-target isolation (selection) process is of major importance in military equipment. Target selection is needed primarily for detecting rocket launches, and for tracking aircraft and satellites. The use of imagers makes the simplest selection method possible. If a matrix imager is provided with an input register, the device can be used in a moving-target indicator in the following way. The indicator consists of two analogous imagers: an image (figure 61) is transmitted onto one of them and is then transferred to the other image where it is stored on a frame. The stored image and the image from the next frame coming from the first imager are applied to a differential amplifier. The inter-frame difference extracted by the differential amplifier will indicate whether the information in the next frame has changed; if the picture has not changed, i.e., there are no moving targets, the amplifier outputs no signal. Cameras which extract inter-frame difference are especially needed for on-board systems, since only the narrowband difference signal, which is easier to transmit and harder to intercept, need be transmitted over the downlink, rather than the entire broad spectrum of frequencies corresponding to the frame recording. A description of an experimental prototype of a moving-target indicator using two 160 x 100 imagers is given in [71].

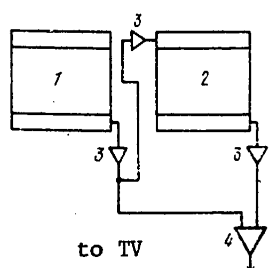

Figure 61. Extraction of inter-frame difference by imager: 1--light-sensitive imager; 2--storage imager; 3--amplifiers; 4--differential amplifier

Imagers are irreplaceable in electrooptical submarine periscopes [72]. The requirements for periscope photoreceptors are high: first, they must be highly sensitive, since periscopes are capable of 360° revolution, and the faster the periscope moves the lower its probability of detection; secondly, it must be burn-resistant, in case the enemy detects the periscope and tries to destroy it with a laser beam. Periscopes use both linear and matrix imagers; store-and-hold matrices, which make it possible to combine a large number of picture elements and high sensitivity, are especially suitable for this purpose [73]. In contrast to CRT (and, of course, the human eye), imagers are not susceptible to burning; when hit by a laser beam an imager is "blinded" and then fully recovers. The unique capability for processing video information directly within the imager chip makes it possible to develop a device for detecting masked man-made objects which is suitable for field operation. The Hughes Research Lab is developing an integrated circuit with three parallel shift registers which allows aperture correction and isolation of the image contours formed by the imager [74]. Using this approach, image processing can be done 300-1000 times faster than by a general-purpose computer. (as is now done).

Study of space and natural resources. The development of the SPOT system is an impressive example of using imagers for observing the ground and prospecting for natural resources. The creation of the SPOT satellite system, which is part of the European satellite observation system, is planned for completion in France during 1983-1984 [75]. The system is based on a Fairchild linear imager containing three rows of 1000 elements each. At an orbital altitude of 809 km, the system can distinguish 20-meter objects on the ground; in the developers' opinion, there are no difficulties in principle in improving the resolution to 10 meters (by comparison, the LANDSAT-D satellite provides 30-meter resolution). The system is designed to operate in the visible 0.48-1.05 μm band, and should have high sensitivity, since the image from a single strip 20 meters wide is stored for 3 msec instead of 1 μsec, as was the case in the mechanical scanning system.

The star orientation system for "flying laboratory" satellites generally uses a vacuum-type television tube, or image dissector [76]. The shortcomings of this system include the distortion inherent in an electron-optical image, sensitivity to electrical and magnetic fields, nonuniform sensitivity across the surface of the tube, requirement for stabilized high voltage, and fragility. Because of this, precise calibration was required prior to each orientation operation, as well as frequent corrections.

The use of imagers makes it possible to avoid these shortcomings and to achieve orientation accuracy of about one angular second. The system first makes a 10-second search for an appropriate star within the field of view of the lens, and then the coordinates of the star are continuously measured with accuracy of 1:7000; the information is output every second. It is noted that if the image dissector accumulates a total of five photoelectrons per element over 10 seconds, an imager can store up to 300,000 as the result of integration: this increases recording reliability significantly. It is proposed that the orientation system being designed use 500 x 500 Texas Instruments matrices which are back-lighted (since interference from overlapping electrodes during front illumination may cause errors in determining the coordinates). The matrix is cooled to -40°C and operates in the slow-scan mode [76].

Thanks to their high sensitivity, imagers are used in astronomy to record images of weakly illuminated objects. Photographic film registers about 1% of incident photons, while the best brightness amplifiers register approximately 20%; an imager using photodiodes as the light sensing elements, or back-lighted imagers, can actually record each photon. In order to reduce the influence of noise, imagers must be cooled with the help of a miniature cooler. The article [77] mentions the use of a back-lighted 400 x 400 Texas Instrument matrix imager in a telescope for photographing deep space. The matrix was cooled to -40°, so that dark currents dropped sharply and the frame holding time could be increased to 10 seconds or more.

Theoretical comparison of multi-element receivers (photoresistive with address switching, imager and vidicon) indicates that the use of imagers is effective for medium and low photon intensity [78]. When working with the low illumination characteristic for astronomy, sample and hold matrices and imagers with electronic image input (and amplification) are of particular interest. The article [79] examines the use of this type of matrix; it is noted that a CCD-201 matrix has been used in the store and hold mode to obtain high quality pictures of the night sky.

Imagers are used in astronomical instruments with wide spectral ranges (from IR to X-radiation). An imager located at the focus of an X-ray telescope provides an X-ray picture of the sky with good angular and energy resolution [80]. Furthermore, imagers can be used for recording and energy analysis of individual X-ray photons. For example, a small-format CCD-202 matrix (100 x 100 elements) has been used successfully to detect X-ray photons with energy of 5.9 and 22.4 keV [80].

Applications and broadcast television. The GOST 7845-55 television standard requires definition of about 600 lines ($5\cdot10^5$ elements per frame). Although large-format imagers have been developed both in the USSR and abroad [17, 18] which are compatible with the requirements of the television standard, it is still early to talk about replacing vidicons with definition of up to 750 lines, especially in studio equipment. However, there still remains a huge field of activity for imagers in applications television. Television cameras using imagers are being developed in three phases: 1) realization of 100-line resolution (i.e., 10^4 elements per frame); 2) 300 lines (approximately 10^5 elements); and 3) 600 lines ($5\cdot10^5$ elements) [81]. Imager cameras with 100-line resolution are of limited interest for television, although they can be used successfully in automation systems, astronomy, etc. Cameras with resolution of about 300 lines are being used widely in applications work. Such cameras can be used, first of all, to create a new generation of industrial television installations. The CRT television camera (vidicon) has always been a complicated, capricious device requiring the qualifications of an engineering specialist to operate it. Because of the use of a heated cathode in the tube, the camera life is short, and the power consumption and heat emission are high. In addition, it has not been possible to reduce the size of the camera significantly, even using transistors and integrated circuits, since size reduction is limited by the unit containing the tube and focusing-deflecting system. These shortcomings of vacuum-tube television cameras have retarded the development of applications television.

The development of television cameras using medium-format matrix imagers (domestic [63-65] and foreign [62]) makes it possible to lay the foundations for the wide penetration of television installations into various areas of industry. As an example, we can cite two domestic cameras using a 288 x 232-element medium-format matrix. Both of these cameras are fully solid-state, and consume 0.5-2 W with a 10-24 V power supply. The cameras operate at frequencies of up to 5 MHz with illumination levels of 1-2 lux, and transmit all of the gradations of a test pattern on the screen of any television receiver with external video signal input.

Television cameras such as these can be used in devices for monitoring various production processes and natural phenomena. As one example, a forest-fire warning system using a network of imager cameras, which are reliable, consume little energy and require no adjustment, can provide a significant economic effect.

In addition to industrial television installations, medium-format matrices are used in video telephony. For example, the "Picturephone" video telephone system uses 256 x 220-element Bell system matrices [5, p. 175]. Cameras using medium-format matrices are produced by a number of companies in two special-purpose versions: for producing a visual image with an analog output, and for various industrial applications - with analog and digital outputs. The General Electric Company, for example, is actively advertising cameras based on charge-injection matrices. The TN-2000 camera is used for imaging; it uses a 244 x 180-element charge injection matrix. The TN-2200 camera is specialized for the requirements of automation, and is produced with 128 x 128-element and 40 x 340-element matrices (for monitoring long narrow objects). There are plans to produce a general-purpose TN-2500 camera with a 244 x 250-element matrix and an analog and eight-bit digital output.

The Fairchild MV-250 cameras, using a medium-format CCD-211 matrix (244 x 180 elements) have been used for several years in military, space and industrial television equipment. Among the areas of application of medium-format matrix cameras are the mining industry, where they are used to monitor boring; the chemical and gas industry, where imager cameras are becoming irreplaceable, since they can operate in explosion-hazardous areas, in contrast to vidicons. The use of a camera with a medium-format matrix converts an optical microscope to a television microscope. Outputting the information to a television screen makes the operator's work easier, and allows the object to be studied by several observers, for example in teaching. A separate area of television technology is represented by facsimile equipment designed to read and transmit texts and graphic images over distances. These devices require linear imagers with over 1000 elements. For example, the CCD-121 linear imager with 1728 elements and the µpD-792 with 2048 elements can be used to read a page of text 216 mm wide and 257 mm long at 10 MHz with resolution of eight lines/mm.

A television camera with a linear imager can be used effectively when the image is unidimensional: for reading envelopes, monitoring monetary symbols, sorting small objects, and monitoring phase boundaries during chemical reactions. An example is the Fairchild CCD-1300 television camera. This camera uses a 1024-element CCD-131 linear imager. Modular construction of the control and signal processing units, operation in both analog and digital modes, automatic gain control and computer interface capability are the basic features of the camera which ensure demand on the part of industry; the cost of the system, including the camera, power supply and lenses, is about $3000.

The use of linear imagers for television transmission of slides and movies is of interest. Item [83] describes the development of an experimental telecine transmitter using a 1024-element linear integer with a latent channel. The Valvo Company has developed a system for showing color slides (television slide transmitter) on a television screen which uses a 500-element linear imager with photodiode light sensing element and peristaltic registers [84]. An industrial FDL-60 color telecine transmitter using three linear CCD-131 imagers (1024 elements) has been developed in the FRG. Figure 62 shows a functional diagram of the telecine transmitter which competes successfully with the familiar travelling beam system.

The transmitter consists of light source 1, tape transport mechanism 2, rotating prism 3 and light splitter 4 with a linear imager. Section 5 controls the linear imager and provides additional correction. This is followed by unit 6, which provides matrixing, black and white level referencing and gamma correction; this section outputs standard color TV signals. Then the luminance and chroma signals are converted in section 7 to digital eight-bit signals (signal/noise ratio 50 dB) and input line by line into a 16 kilobit memory. Frame storage is necessary for interlaced scanning. Unit 8 corrects the color and definition and provides analog conversion of the signals. The entire operation of the telecine transmitter is controlled by an 8080 microprocessor [85].

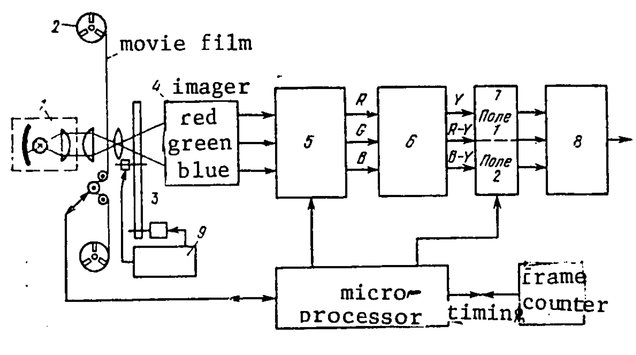

Figure 62. Transmitter diagram: 1--light source; 2--tape transport mechanism; 3--rotating prism; 4--light splitter; 5--linear imager control unit; 6--matrixing unit; 7--analog-digital converter; 8--color/definition corrector/digital-analog converter; 9--light intensity regulator

A domestic camera using a 512-element linear imager has been developed for monitoring the growing of silicon ingots; questions involved in the construction of television cameras using linear imagers and timing generators for controlling linear imagers are explained in [86, 87].

As was noted above, the utilization of imagers in broadcast television is made more difficult by the fact that the definition of large-format matrices is not yet good enough by comparison with vidicons. However, television cameras using large-format imagers are under intensive development worldwide. The very lightest remote news camera using vidicons weighs about 8 kg; the weight of an imager news camera can be reduced to 1.5-2 kg. If television cameras using large-format imagers replace vidicon cameras in domestic equipment (video cassette recorders, video disc players, etc.), thus providing improved reliability, operation, weight and size, imager developers will be ensured an extensive, stable area of application for many years. The appearance of such television cameras will make possible the development of electronic photographic equipment which will replace ordinary equipment, eliminating the need to deal with photographic film and its processing.

One feature of current developments of TV cameras using large-format imagers is the fact that they are primarily intended for producing color images. It is actually in color cameras that the advantages of CCD over CRT (e.g., vidicons) show up most clearly; it is sufficient to note that the hard geometric raster of the CCD makes picture color convergence easier.

There are three possible configurations for color cameras using imagers. In the three-matrix design (figure 63a) one of the matrices (the green channel) forms the definition video signals, so the highest possible resolution is required; the matrices in the blue and red channels can have resolution one-fourth as good (these are actually not fully utilized). Solid color filters are used in the three-matrix camera. The two-matrix design (figure 63b) equalizes the requirements for matrix resolution. One of the matrices works in the green channel just as in the three-matrix camera. A blue and red striped filter is placed ahead of the second matrix; therefore, all of its elements participate in creating the color image. The single-matrix camera (figure 63c) requires a three-color cellular filter containing twice as many green cells as red or blue. Slow-scan television uses a sequential-type single-matrix camera with a rotating disc containing green, red and blue filters in its openings [88]. The three-matrix color camera produces the best picture. The shortcomings of this design require the use of a large number of matrices, which are rather scarce because of the low output of good components, a complex light splitting section and low vibration resistance.

The attempt to increase the output of good matrices by reducing the number of elements along the horizontal, and consequently the size of the sheet, led to the development of the "spatial shift" method. This method consists essentially of shifting the matrices horizontally and using line-frame transfer. As we know, the image formed by a matrix with line-frame transfer leaves "empty" vertical strips which correspond to the shift registers not participating in creating the image. It is possible to insert, so to speak, into these "empty" strips the banded image formed by the second matrix. This image has an analogous structure but is shifted one step horizontally, i.e., by the width of an element (assuming that the width of the light-sensitive element and the vertical shift register is the same). The overall resolution doubles, i.e., in order to obtain the required horizontal resolution it is possible to use matrices with half as many elements along the horizontal.

An effective example of the use of the spatial shift method is provided by the three-matrix camera developed by Sony [89]. This camera uses matrices with a line-frame structure containing 492 elements along the vertical (in agreement with the Japanese TV standard) and a total of 226 elements along the horizontal. The matrices in the blue and red channel are shifted by one-half step horizontally in relation to the green-channel matrix. As a result, the definition of the color image perceived by the eye is increased. The definition can be increased still further by using half the signals from the blue and red channels to synthesize a quasi-green signal.

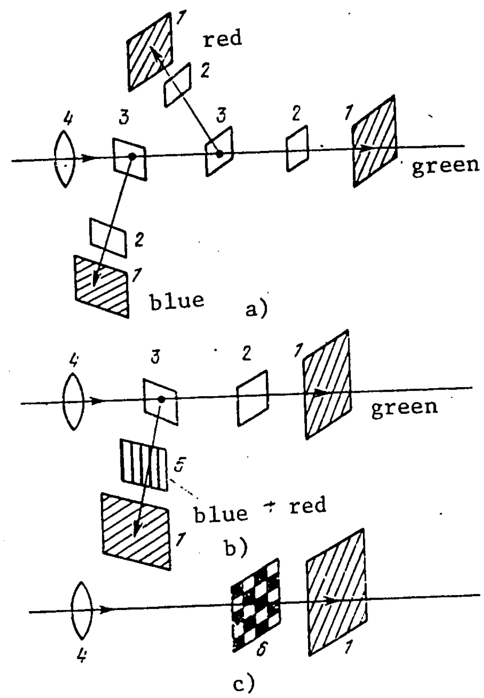

Figure 63. Color imager camera configurations: three-matrix (a), two-matrix (b), and single-matrix (c); 1--imager; 2--solid light filter; 3--separation of light beams; 4--lens; 5--banded light filter; 6--cellular light filter

A three-matrix scheme is being used in a color camera under development in this country [90]. Three large-format frame-transfer matrices containing 575 x 532 elements are used. The use of horizontal and vertical correctors in the camera makes it possible to compensate for inefficient charge transfer [91]. This camera is intended for news reporting.

Two-matric cameras contain fewer matrices, have a simpler light splitting device and are more vibration resistant. The spatial shift method is not used here: both matrices are fully utilized, but each must contain a large number of elements. A two-matrix camera using frame-transfer matrices containing 512 (vertical) x 340 elements is being developed by Toshiba; there are plans to market the camera during the 1980s, and the developers believe that the two-matrix construction responds best to the requirements of color television [92].

The NEC Company (Japan) is developing a single-imager color camera containing 492 (vertical) x 400 elements. The line-frame transfer matrix uses photodiodes as photosensing elements, which makes it possible to improve the sensitivity in the blue region of the spectrum by almost an order of magnitude (by comparison with MOS elements with polysilicon electrodes). The desire to improve spectral sensitivity distribution forces developers to use either photodiodes or MOS elements with transparent electrodes in modern imagers for color television.

Regardless of the fact that cameras using large-format imagers are under intensive development in many countries, the only industrially produced cameras are the Fairchild black and white system using the CCD-221 matrix (498 x 390 elements) and the RCA device using the SID-51232 matrix (512 x 320 elements). These cameras are built by special order, and cost between $5000 and $8000. In 1979, RCA offered the three-matrix SID-51232 camera for sale. This camera was successfully used in a bathyscaph for research beneath the Pacific Ocean at depths of up to 3 kilometers, with good color image quality [93]. The Fairchild black and white camera is used in military equipment. RCA plans to use their camera in 1983 on a space vehicle for investigating Jupiter, as well as in an astronomical telescope [1].

Automation, computers. The simplest automation device is an imager TV camera which monitors some object, process or parameter. Within the extensive class of automatic devices working on the standard-comparison principle, imagers not only replace CRTs, but also provide far better accuracy thanks to hard coordinate tie-in. Devices such as these include, for example, program-controlled machine tools. In developing equipment for fabricating semiconductor devices, imagers can be used in assembly machines which automatically find the contact areas, in photolithographic alignment devices, in devices for monitoring defects and measuring the dimensions of masks, etc.

The continuing increases in the speed and memory capacity of computers requires a shift away from unreliable, slow optical-mechanical paper tape or punch card readers to direct optical input of printed and handwritten text. No less important is computer input of data concerning the movement of equipment assemblies, e.g., tools, the coordinates of stationary or moving objects, variation in the spectral composition of radiation reflected from a surface under investigation, etc. Computer input of more complex half-tone images makes it possible to solve a number of interesting problems: analysis of kinograms of fast processes, studying x-ray pictures and processing spectrozonal and stereoscopic pictures received from satellites. Imager-based sensors have a number of important advantages over familiar optical sensors such as photodiodes and photoresistive matrices, vidicons, photoelectronic multipliers, etc.: they are universal (allowing data input in both analog and digital form), they provide high accuracy in determining coordinates and they are fast.

The item [94] examines examples of the use of medium-format matrix (288 x 232 elements) and linear (512 and 1024 elements) imagers in devices for inputting spatial and angular coordinates of pixels, including stereoscopic, binary data from paper tape, punch cards and holograms, and half-tone optical images. Special note is made of the prospects of using matrix imagers to build pattern recognition devices using the correlation principle. A matrix-imager correlator can execute a two-dimensional correlation function in 10^{-2}sec. To do the same thing digitally requires 10^8 operations, i.e., in order to complete the process in 10^{-2}

sec, it would be necessary to have the extremely high speed of 10^{10} op/sec.

Instrumentation. Linear imagers are ideal devices for precision measurements of remote or inaccessible objects. The contours of the object being measured are projected onto the linear imager, and the number of pulses "contained" between the boundaries are counted. The absolute error is ± 1 pulse; if the linear imager contains 1024 elements, the measurement accuracy can reach 0.1%. A 512-element linear-matrix system is being used successfully to measure the diameter of a silicon ingot and to keep that important parameter at the required value. In a device used to monitor the dimensions of rolled articles, whose temperature can reach 700-1200°C, a linear imager is replacing the optical-mechanical scanner, which is unreliable and slow. Measurement accuracy at distances between 10 mm and 15 m is 0.4-0.5%; 0.1% can be achieved by using the differential measurement method. Linear imagers can replace expensive diffraction gratings in devices where precise coordinate measurement is required. An example is the photoduplicator used to make masks, which registers the coordinates of the moving table along both axes within a fraction of a micron.

Imagers are used extensively in oscillographic instrumentation. Until now, pulse amplitude measurement, curve measurement, and determination of time intervals have all been done very inaccurately using graticules. A simple oscillograph attachment which projects an image onto a matrix imager makes it possible to measure any figure on the screen precisely. Furthermore, thanks to the lack of delay in the imager, it is possible to write high-speed processes from the oscillograph screen and then read them at lower speed.

A CCD-202 imager (100 x 100 ohms) is used in streamer cameras for recording fast processes [95]. Replacing photographic film with an imager has made it possible to increase measurement sensitivity by an order of magnitude; the capability of outputting data digitally provides additional convenience.

Medicine. The high sensitivity of imagers allows them to be used successfully in devices for investigating internal organs (gastroscopes, cystoscopes, etc.). Two-matrix imagers can provide the basis for a device to teach the blind to read; this device analyzes printed texts and transforms the letters into a pin code which is sensed by the hand of the student. A plan for creating an artifical eye is presented in [96]. A matrix of microelectrodes is implanted in defined sectors of the brain where electrical current stimulation produces the sensation of light spots (phosphenes): 64 electrodes are enough for a blind person to have an idea of the shape of nearby objects and to be able to orient himself spatially. The electrodes are coupled with the imager matrices, which are mounted on eyeglass frames, by means of induction coils through the skull. A significant shortcoming of this prosthetic eye is the fact that the electrode connection scheme must be selected for each patient, since there is no direct relationship between the positions of the matrix element and the light spot which it produces.

Miniature color or black and white TV cameras using imagers are extremely useful in operating rooms: placed directly above the operating field, they can make video recordings of complicated operations and display the work of the surgeon to a large teaching auditorium. Simple TV cameras, even with medium-format imagers, can be used to monitor the condition of critically ill patients in wards, to observe neonates in incubators, to provide two-way contact with infectious patients, etc.

Now that we have looked at the basic areas of application of imagers, we shall now consider the operation of this class of devices. The hardware developer must, in addition to having information on imager parameters, be able to build an optimal imager control and video signal processing circuit. Transfer efficiency depends upon the shape of the timing pulses, the amount of overlap and the edge slope. Stray pulses from the electrodes and the reset transistor leak through to the output of the imager: the degree to which they can be suppressed determines the quality of the television image. As an example of solving the circuit engineering problems which arise in imager operation, let us examine the operation of a camera using a medium-format matrix with 288 x 232 resolution elements [63].

Figure 64 shows a functional diagram of the camera, which includes two timing generators comprised of sync generators and phased voltage generators, as well as a video signal generator/amplifier. One timing generator, which operates at 280 KHz, controls the accumulation and storage sections, while the other, high-frequency (up to 14 MHz) generator, controls the output register. The camera outputs to a television monitor without interlaced scanning. The rasters of both fields coincide, each containing 288 lines on the forward vertical scan and 24 lines on the reverse scan. This reduces the requirements for frame synchronization performance; the difference between the frame or line frequency and the standards does not exceed 0.2%. In order to transmit an image, the first field uses odd lines, blanking the even ones, with the reverse being the case in the second field. During the vertical scan return, 144 charge transfers are made from the accumulation section to the memory section. Information is output from the memory section in two-line intervals during the line scan return. The rate of all transfers in these two sections is the same, or approximately 94 KHz.

In order to improve charge transfer efficiency, and to improve the contrast-frequency characteristic, the camera uses optical background charge injection done in the near-IR portion of the spectrum with the help of two emitters. In order to obtain a nonlinear light response (i.e., to do gamma-correction) and to transmit bright details without degrading the transmission of dark areas, the camera changes the capacitance of the potential well during charge accumulation. Gamma-correction is done in one step; at the end of each field, for an amount of time equal to 1/13 the duration of the field, instead of accumulating the charge for the electrodes of one phase, the charge for the electrodes of two phases (first and second) is accumulated. This also makes it possible to reduce the dark currents in the accumulation section (lower voltage is applied during most of the time) and to set the accumulation section to the same state as the memory section which is required for the next synchronous charge transfer.

Induced timing currents are suppressed in this camera by the use of a differential output. There is also a way to control induction by using dual correlated sampling [36]. The use of dual correlated sampling makes it possible to suppress induced timing currents and to compensate for noise in the reading section. The item [65] contains an actual dual correlated sampling circuit. More details on

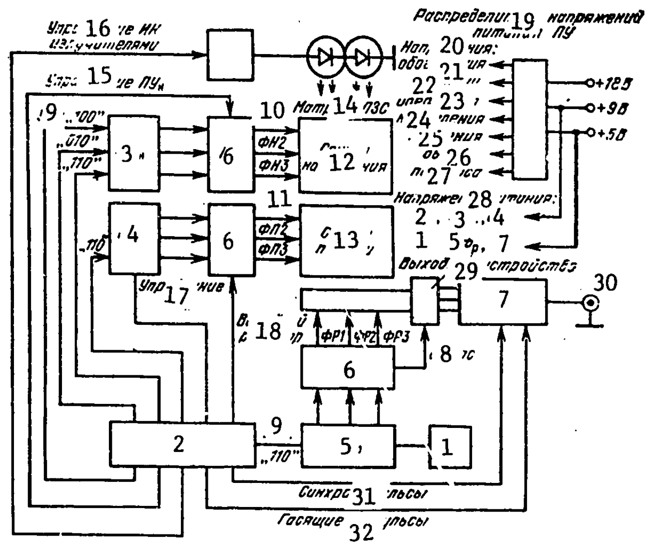

Figure 64. Functional diagram of TV camera using medium-format imager: 1--oscillator; 2--sync generator; 3--accumulation section phase voltage generator; 4--memory section phased voltage generator; 5--output register phased generator; 6--level converters; 7—amplifier-mixer; 8--reset; 10--FN [expansion not given]; 11--FP [expansion not given]; 12--accumulation section; 13--memory section; 14--CCD matrix; 15--level converter control; 16--IR emitter control; 17--level converter control; 18--output register; 19--level converter voltage distributor; 20--voltages; 21—separation; 22--substrate; 23—depletion; 24--accumulation; 25--storage; 26--output; 27--transfer; 28--supply voltage; 29--output device; 30--output; 31--sync pulses; 32--blanking pulses

the construction of the timing generators and video signal processing circuits can be found in [64, 65, 86].

In operating imagers it is desirable to know how the devices behave at high and low temperatures and in the presence of radiation, and how sensitive they are to electrostatic overloads.

Elevated operating temperatures are undesirable for charge-coupled devices, in which the information charge is very low. In the opinion of many hardware developers, the advantages of imagers justify the use of miniature cooling devices. The domestic TEMO-3, MT5-1, and MT9-1 microcoolers are small, which allows them to be installed directly on the frame of large-format matrices.

Cooling of medium-format (288 x 232) and large-format (576 x 360) matrices to -40°C has made it possible to almost eliminate all image defects caused by local sections with increased generation-recombination rate, and to use imagers as analog memory devices which provide a one-frame delay [82, 97]. The frame time can be increased at -40°C to three seconds, while this figure does not exceed 0.5 seconds at room temperature.

Imagers are extremely sensitive to radiation. In devices using a surface channel, the degradation under the influence of gamma-radiation is more severe than in devices with a buried channel [98]. The largest change in parameters is observed in n-type devices using a surface channel (i.e., on a p-type silicon substrate); CCD with p-type surface channel and buried n-type channel are more stable. The state density on the interface boundary and dark current increases by an order of magnitude under a dose of $2 \cdot 10^2$ J/kg in devices with a surface channel. Flat-zone potential also shifts: from -1V at 10^2 J/kg to -4 V for polysilicon electrodes and -2V for aluminum electrons at 10^3 J/kg. A technological process has been proposed for manufacturing CCD which can withstand enhanced doses of gamma radiation [98]. The basic idea is to eliminate high-temperature silicon processing and any other influences which disturb the semiconductor material. For example, it is proposed to apply the oxide pyrolytically at temperatures below 925°C, and to deposit aluminum using the ordinary vacuum deposition method without using an electron beam, since a dose of up to 10^4 J/kg is imposed during electron-beam deposition, and its effect cannot be completely eliminated by annealing. Nonetheless, CCD using a surface channel made using this approach are still degraded significantly after a dose of 10^3 J/kg; after a dose of 10^4 J/kg the transfer efficiency was only 0.992 for a 50% background charge.

Imagers are protected against electrostatic potential, first through design, by introducing guard diodes beneath the contact areas of electrodes, and secondly by using grounded clothing and bracelets, shorting the leads with pieces of foil, using special conducting packaging, etc., during operation. The literature contains no information on the sensitivity of imagers to electrostatic influences, but we can assume that they behave in this respect the same as MOS devices and MOS ICs.

Conclusion

To summarize the content of this book briefly, we can say that the imager is a new, rapidly developing class of instruments which both improve the indicators of photoreceiving equipment and also realize qualitatively new characteristics; progress in the development and application of imagers is determined entirely by the technological level.

The principle of processing information only with the help of charges is in fact a new one and distinguishes CC devices fundamentally from all others. The rate of growth of charge-coupled devices is surprising, even against the background of the rapid development of microelectronics: no more than 18-24 months passed between the appearance of the CCD and industrial production. It must be noted that imagers are hardly likely to become mass-produced devices -- perhaps only later, when domestic color TV cameras using imagers win the recognition of consumers, replacing movie cameras and photographic equipment. The qualitative aspect is now more important that the quantitative aspect in the application of imagers in radioelectronic equipment. Table 2 shows the advantages of charge-coupled devices, and their qualitatively new properties.

The problems which now face integer developers generally consist of the following: increasing resolution, improving sensitivity, especially in the blue region of the spectrum in connection with the development of color television, and controlling image blurring during local light overloads (blooming).

There are several ways to improve imager resolution: simply increase the number of elements on the chip, thus increasing the size of the chip; increase the degree of integration, i.e., reducing the size of the element and increasing the number of elements without increasing the size of the chip; using hybrid assemblies where possible (linear imagers, store and hold devices); using design and circuit engineering approaches such as the spatial shift method.

The trend toward increasing chip sizes which was so evident during 1971-1975 is now absent: this is because of the low output of good devices with large active-region areas. The Bell Labs matrix imager using a 16 x 20 mm crystal is not being produced because of the difficulties in obtaining good crystals. The 1975 RCA matrix (512 x 320 elements) has an active crystal of 149 mm^2; the analogous 1979 matrix from Toshiba reduces this area to 59 mm^2. The maximum number of elements in linear imagers is 2048, with a further increase hardly justified. The number of vertical elements in matrix imagers is fixed by the TV standard (from 488 to 576); horizontally there are between 350 and 500 elements. The Texas Instruments Company announced plans in 1979 to develop an 800 x 800-element matrix, but this imager is intended for special use in astronomical equipment.

Table 2

Comparative Characteristics of Imagers and CRTs

Characteristic	Imager	CRT
Sensitivity (threshold)	High (low output capacitance)	High output capacitance
Resolution	500 TV lines; up to several thousand in hybrid assembly	750 TV lines
Raster	Fixed	Floating
Information processing within device	Easy	Impossible
Arbitrary sampling	Possible (in PZI) [expansion not given]	Impossible

Characteristic	Imager	CRT
Lag	None	15-40%
Power consumption, W	0.5	5
Supply voltage, V	5-25	200-10,000
Weight, g	5	50
Size, cm^3	0.5	5
Service life, hours	15,000	500-800
Mechanical strength, g	To 20,000	1000
Explosion hazard	None	Exists
Microphonic effect	"	"
Sensitivity to magnetic and electrical fields	"	Present

Increasing the degree of integration by reducing element size is attracting far more attention on the part of developers. For example, in a matrix imager using frame transfer, the dimensions of the light sensing elements have been reduced from 30 x 30 μm^2 (1975 level) to 26 x 13 μm^2(1979); the size of the light sensing elements in the Sony line-frame matrix imager is only 7 x 13 μm^2. Imagers with elements this small require not only significant improvement in photolithography quality, but also the use of more sophisticated optics. Switching CRT television equipment over to CCD leads to the need for developing high-speed lenses with resolution of at least 200 lines/mm. The ability to combine imagers in hybrid assemblies distinguishes this class of devices favorably from CRTs. It is difficult or impossible to combine matrix imager crystals using frame and line transfer into a hybrid assembly (which, for example, requires dividing the light beam). At the same time, linear imagers and matrix imagers operating in the store and hold mode can easily be combined into large systems. The number of elements along one axis in such systems can reach several thousand, and there are no particular limitations in principle for increasing this further. From the technical and economic viewpoint, it is better to produce a large number of medium-format linear and matrix imagers with a satisfactory output of good pieces than to try to produce even a few large-scale devices. Hybrid assembly methods become especially important in the area of developing imagers for the IR band, where it has not yet been possible to create integrated devices using narrow-zone semiconductors alone.

The sensitivity of imagers is increased in the blue region of the spectrum, as is noted repeatedly in this book, is achieved in three ways: by replacing polysilicon electrodes, which do not transmit light well, to transparent ones made of metal oxides (tin, antimony); reducing the thickness of the silicon substrate to 10μm and illuminating it from the back; and using photodiodes instead of MOS structures. All three methods are receiving equal development, and it would be hard to predict which of them will win out in the future. Imagers using photodiodes have received slightly more recognition recently; the sensitivity of these devices is an order of magnitude better in the blue region than in imagers using polysilicon electrodes.

The phenomenon of blooming is suppressed best in charge-injection devices which can withstand local light overloads of up to 1000 times. Good anti-blooming characteristics are also exhibited by CCD in which it is possible to construct a drain region for excess minority carriers -- linear imagers with one readout register, and matrix imagers using line-frame organization.

The aforementioned problems refer to imager development and fabrication. These, of course, are not the only problems arising in the development of this young area of microelectronics. For example, the prospects for development of imagers are determined to a great extent by where the devices are to be used. Hardware developers must understand that the application of imagers often opens up completely new possibilities which could not be realized on the basis of earlier image generators. Obviously, it is necessary that we not simply replace vacuum tubes with charge-coupled devices, but that we find, as a first priority, types of equipment in which the switchover to CCDs is most justified.

We can hope that resolution of most of these problems, through the joint efforts of imager and hardware developers, will promote further progress in microelectronics and television technology.

Table of Contents

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CIRCUITS & SYSTEMS

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ELECTRONIC CIRCUITS WITH NONLINEAR FEEDBACK

Moscow ELEKTRONNYYE SKHEMY S NELINEYNYMI OBRATNYMI SVYAZYAMI in Russian 1980 (signed to press 15 Dec 80) pp 2, 278-280

[Annotation and table of contents from book "Electronic Circuits With Nonlinear Feedback", by Yuriy Vasil'yevich Safroshkin, Izdatel'stvo "Nauka", 2700 copies, 280 pages]

[Text]

Annotation

This book explains the conception of the formation of analog-discrete properties in inseparable electronic circuits with stepped (piecewise-constant) feedback. The physical aspects of feedback are clarified on the basis of a closed method of direct measurements of reverse transmission, and generalization of its properties for various circuits. A classification of such circuits is proposed, and basic principles for utilizing them are formulated. A unified engineering approach to the investigation and calculation of statics is presented along with the fundamentals of the dynamics of modern circuits using operational amplifiers with nonlinear feedback. New capabilities are explained. A number of practical directions are developed, investigated and extended for utilizing analog-discrete properties. A great deal of experimental material is presented, and specific developments of instruments and equipment for scientific research are described.

The book is intended for scientific workers and engineers interested in modern circuit engineering and circuit theory and their applications to problems of instrument building, radio electronics and automation.

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6900
CSO: 1860/212

UDC: 621.382

HYBRID IC FOR CHARGE-TIME INTERVAL CONVERSION

Moscow PRIBORY I TEKHNIKA EKSPERIMENTA in Russian No 1, Jan-Feb 82 (manuscript submitted 31 Jul 80) pp 102-104

[Article by S. G. Basiladze, Yu. Yu. Dotsenko, P. K. Man'yakov and S. N. Fedorchenko, Combined Nuclear Research Institute, Dubna]

[Text] This article describes a hybrid integrated circuit for linear charge-time interval conversion with input speed of a few nanoseconds. The circuit can be used in energy measurement channels, in time-digital converters and in modified form in amplitude-digital converters. The circuit has a fast reset input for stopping the conversion process. The minimum measurable signal range is 256 pC or 250 mV in the amplitude measurement mode. The maximum conversion time is 50 μsec, and integral nonlinearity amounts to 0.3%.

The functional designation of general-purpose analog integrated circuits do not always respond to the requirements for analog-digital code converters used in nuclear physical experimentation. For example, one specific requirement for converters is that of rapid cessation of the conversion process and restoral of the initial state if the event recognition system outputs a negative decision. Transistorized analog-time interval converters contain approximately 50 electronic components, consume about 400 mW, and occupy approximately 20 cm^2 on a printed-circuit board, which makes it impossible to accomodate more than 8 10-bit analog-digital code converters in a CAMAC unit. In addition, the thermal stability of the "pedestal" of the converter is not very good.

The present article describes a hybrid integrated circuit for linear charge-time interval conversion with input speed of a few nanoseconds. This circuit can be used in channels for measuring energy (pulse "area"), in time-digital converters and in modified form in amplitude-digital converters. The circuit has a fast reset input to cut off the conversion process, and is held in a 14-lead 25 x 20 mm^2 case.

The converter, whose schematic diagram is shown in figure 1, consists of a buffer amplifier, linear throughput circuit, capacitor charge dc source and time interval extraction unit. The buffer amplifier (E_1, E_{2-2}) is a current follower which provides low input impedance and high output impedance through negative current feedback. The current gain of the amplifier is near unity. The amplifier can work with negative input current pulses (shown in figure 2a and b) and with low-amplitude positive pulses (figure 2c). The maximum negative working current pulse is 20 mA, while the maximum positive voltage pulse is 300 mV[1].

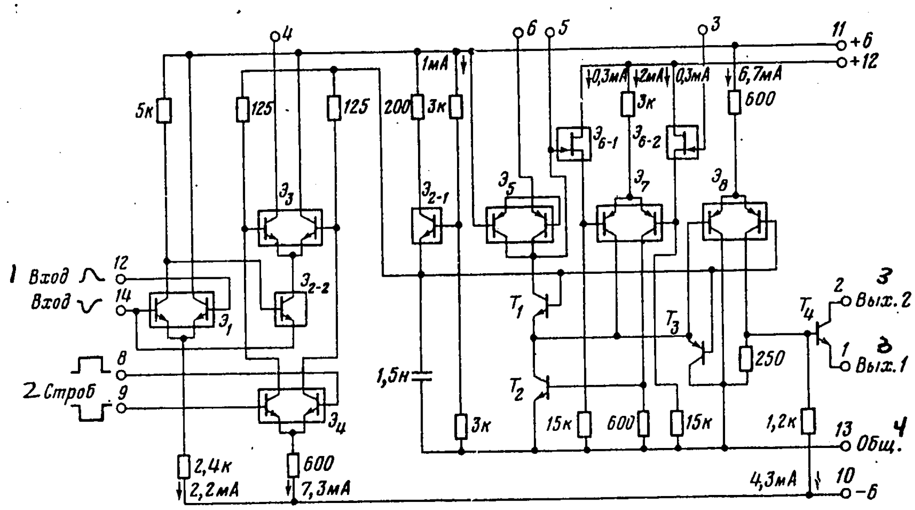

Figure 1. Schematic diagram of converter. 1, input; 2, strobe; 3, output; 4, common.

The linear throughput circuit selects the input pulses by means of the paraphrase Strobe signal (e.s.l. [expansion not given, possibly emitter- coupled transistor logic--Tr.] levels). The current from one transistor in E_3 is switched to the other transistor, and the linear throughput circuit switches from the normally closed state to the open state. Resistor R_1, which is connected to output 14 (figure 2), determines the initial current through the circuit and assigns its "pedestal". The recommended "pedestal" current is 100-300 μA, and the value of $E_1 \geq 6$ V. Transistor pair E_4 matches the levels. Transistor E_{2-1} is the internal +2.3 V source.

The output of the linear throughput circuit (lead 4) can be connected to lead 5 (charge measurement mode, figure 2a) and to lead 3 (input pulse amplitude measurement mode, figure 2b and c).

The extracted input current pulse charges C_3. This is an external capacitor, which means that its value can be varied in order to change the conversion factor of the circuit and to allow it to be used in amplitude measurement channels. In

[1] A signal divider can be connected to the input of the converter, since the conversion factor in the amplitude measurement mode is much greater than unity (cf. below).

the charge measurement mode, the minimum value of C_3 is 130 pf, and 300 pf in the amplitude measurement mode. The working pulse amplitude range for C_3 is 0-2 V. The recommended value of resistance R_1=200-510 ohms.

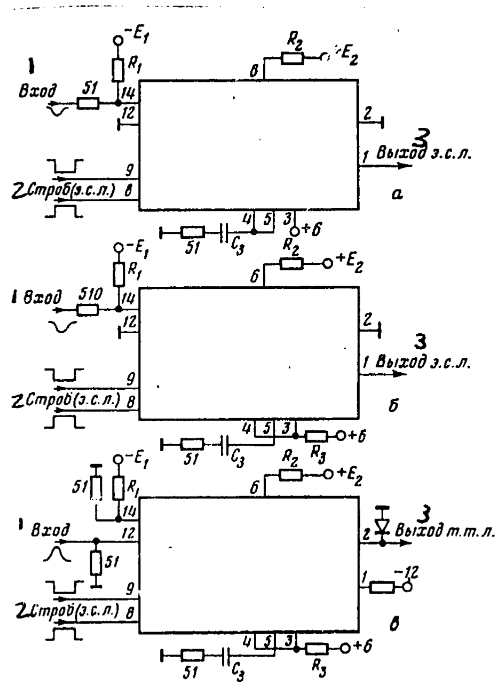

Figure 2. Converter hookup variations: a - measuring pulse charge; b, c- measuring amplitudes for pulses with negative and positive polarity; 1, input, 2, strobe (e.s.l. [possibly ECTL-Tr.], 3, e.s.l. output.

Capacitor C_3 is charged with dc whose value is assigned by external resistor R_2 and voltage $+E_2$. The only elements in the charging-current source which belonged to the circuit is transistor assembly E_5, the transistors in which are connected in a Darlington circuit in order to reduce temperature drift of the charging current due to variation in a current gain α. The value of the charging current can vary between 10 and 100 μA, while $E_2 \geq 12$ V. A fast-charge current generator for C_3 with value of up to 5 mA can also be connected to lead 6.

The time interval is extracted by the comparator, which uses an operational amplifier (E_6, E_7, T_1, T_2) with nonlinear feedback over two channels: over the primary gain channel (E_{7-1}, T_2, T_1) and over a parallel channel (E_{7-1}, T_1) to ensure stability of the amplifier. During time interval extraction transistor T_1 is closed, T_3 is open and the feedback in the amplifier is disrupted. The circuit produces a standard output signal in ECTL levels (cf. hookup in figure 2a and b), or TTL (open collector from lead 2, cf. figure 2c. The pulsed current applied to the load does not exceed 10 mA.

Parameters	Present Circuit	QT100B
Input impedance, ohms	1	6
Coefficient of reflection of signal from input, %	10	14
Input pulse duration, ns		
in charge measurement mode	≥5	≥5
in amplitude measurement mode	100 with C_3= 300 pf	No
Switching time of throughput circuit, ns	3.5	2*
Smallest measurable signal range		
in charge measurement mode, pC	256 with C_3= 130 pf	256
in amplitude measurement mode, V	0.2	No
Maximum conversion time, sec	50	50
Integral nonlinearity, %	0.3	0.5
Fast convertor reset time, sec	0.5	0.5
Temperature drift conversion factor, 10^{-4}/°C	1	4
of "pedestal", pC/°C	0.02 for I_{ped}= 100μA (T_{strobe}=100 ns)	0.2
Power consumption, mW	240	54*

*The circuit of the QT100B does not have a unit which refers the strobe pulse to the ECTL levels; the circuit has a nonstandard capacitive input requiring large strobe-signal pulses.

The table presents the basic characteristics of the present circuit. For comparison, the characteristics of the analogous QT100B circuit produced by the Le Croy Company [1] are also given.

It follows from the table that the converter in question is superior to the QT100B in terms of a number of parameters, especially temperature stability.

In conclusion, the authors would like to express their graditude to V. I. Kakurina for technical assistance and to A. F. Belov for his support of the work.

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6900
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COMPUTERS

UDC 681.3.06:621.396.6

COMPUTER MODELING AND OPTIMIZATION OF RADIOELECTRONIC DEVICES (INTEGRATED CIRCUIT DESIGN)

Moscow MODELIROVANIYE I OPTIMIZATSIYA NA EVM RADIOELEKTRONNYKH USTROYSTV (PROYEKTIROVANIYE NA INTEGRAL'NYKH MIKROSKHEMAKH) in Russian 1981 (signed to press 18 Jun 81) pp 2-4, 270-272

[Annotation, foreword and table of contents from book "Computer Modeling and Optimization of Radio Electronic Devices (Integrated Circuit Design)", by Zalman Mikhaylovich Benenson, Mikhail Rostislavovich Yelistratov, Lev Konstantinovich Il'in, Sergey Vladimirovich Kravchenko, Dmitriy Mikhaylovich Sukhov and Mikhail Abramovich Udler, Izdatel'stvo "Radio i svyaz'", 25000 copies, 272 pages]

[Text]

Annotation

This book presents methods for modeling and optimizing radioelectronic devices in a computer-aided design system. Modern algorithms for computer design of these devices are examined. Descriptive languages for radioelectronic devices are given. The book is intended for radioelectronic equipment, control system and computer-aided design engineers and developers.

[This book was reviewed by Professor A.I. Petrenko, doctor of technical sciences, and Doctor of Technical Sciences M.I. Peskov.]

Foreword

Computer-aided design systems are used in all stages of developing radioelectronic devices. The introduction of these systems began with the automation of a number of design operations: the arrangements of components and functional units in various standard constructions, arrangement of wiring and printed-circuit conductors, and production of paper tapes for controlling the manufacture of multilayered printed circuit boards and integrated circuits. Computer-aided design systems now include subsystems for modeling and optimizing radioelectronic devices which make it possible to improve characteristics significantly and to reduce the debugging time of designed equipment. These subsystems are especially effective in calculating the characteristics of switching circuits and automatic control devices.

Significant difficulties arise when computer-aided design systems are used to model radio receiving and television devices due to the fact that the intrinsic oscillation periods in them are much shorter than the transient processes. These types of electronic devices can be modeled by computer only if an integrated solution is found for the problem of increasing computer output, creating special-purpose terminal and computer devices within the computer-aided design system and constructing efficient algorithms which allow for the circuit engineering singularities of high frequency radioelectronic devices.

Increasing the degree of IC integration introduces significant complication to radioelectronic equipment models based on a composition of models of individual components, i.e., the dimensionality of the equations to be solved increases sharply. Dimensionality can be reduced by using the macro-modeling method in which the model of the IC included in the overall mathematical model of the device is represented by a simplified circuit or simplified system of equations. When this is done, acceptable accuracy should be achieved in approximating the output characteristics of the IC within the operating range of input effects.

In addition to the difficulties enumerated above, difficulties in formalizing the problem also arise in optimizing radioelectronic devices. These are usually multicriterial optimization problems, which are the most complex problems in the theory of mathematical programming. Successful formulation of the optimization criteria and the approach to constructing the target functions and limitations can in many respects help to achieve a successful choice of the best electronic device parameters with acceptable amounts of computer time.

The present book is devoted to modeling and optimizing radioelectronic devices in computer-aided design systems. This theme has been reflected in a number of references, the contents of which can be used to track the development of problem-solving methods and the development of the areas of application of computer-aided design systems. The primary attention here is therefore devoted to problems which have become most urgent in recent years: the construction of IC macro-models and functional radioelectronic units, methods and algorithms for solving linear and nonlinear equations with a large number of variables and rarefied coefficient matrices, algorithms for defining steady-state modes and transient processes in weakly-damped high frequency systems, construction of target functions of the optimization problem and universal languages for describing radioelectronic equipment, as well as accommodation of the interactive mode in the computer-aided design system. In addition, certain related problems are examined which arise in designing radioelectronic equipment: modeling of static magnetic fields and thermal analysis of radioelectronic equipment. The connection between these and traditional problems involved in analyzing electrical circuits is demonstrated.

Analysis of the methods used to model and optimize radioelectronic devices, as well as experience from the practical utilization of computer-aided design systems, indicates that the areas of application of computer-aided design systems and radioelectronic device design can be expanded significantly.

This book was written by a collective of authors. Sections 1.1-1.6, 2.8, 3.1-3.10 were written by Z.M. Benenson; sections 1.7, 3.12-3.14, 6.1-6.3 by S.V. Kravchenko, section 2.1, 5.1-5.3, 5.5, 6.5 by L.K. Il'in; sections 2.3-2.5, 6.7, 6.8 by M.A. Udler; section 2.6, 2.7, 4.1-4.7, 4.13, 4.15, 6.6 by M.R. Yelistratov; section 4.8-4.11 by D.M. Sukhov; seccions 2.2, 5.4 by Z.M. Benenson and L.K. Il'in; section 3.11 by Z.M. Benenson and M.A. Udler; section 4.14 by Z.M. Benenson and D.M. Sukhov; section 6.4 by Z.M. Benenson, S.V. Kravchenko and L.K. Il'in.

The authors are deeply grateful to reviewers Professor A.I. Petrenko, Doctor of Technical Sciences, and Doctor of Technical Sciences M.I. Peskov, who provided valuable comments which helped to improve the content and structure of the book.

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6900
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6TH INTERNATIONAL SYMPOSIUM ON ELECTROMAGNETIC COMPATIBILITY

Moscow ELEKTROSVYAZ' in Russian No 2, Feb 82 p 16

[Unsigned article]

[Text] The next International Symposium on Electromagnetic Compatibility (EMC) will be held in September 1982 in Wrocław (Polish People's Republic). The reports will cover the following themes: radiation, susceptibility and induction in EMC systems and subsystems; radiation and susceptibility of electronic devices and elements; spectrum utilization and frequency planning for intelligence-bearing signals; undesired influence of electromagnetic radiation on fuel and explosive substances; investigation of origin and characteristics of natural and man-made electromagnetic radiation for the case of separate sources and aggregate sources; measurement methods and equipment; antenna behavior outside working band and outside primary operating direction; general fundamentals of standardization; computer analysis and design of EMC. A special section on the biological influence of electromagnetic radiation is also planned.

An exhibition will be held during the symposium which will display the following: modern instrumentation; noise and crosstalk suppression elements; screen chambers; shielding and observing materials; non-radiating and noise-protected devices; modern devices for tracking EM spectrum.

The official languages of the symposium will be English and Russian.

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APPROVED FOR RELEASE: 2007/02/09: CIA-RDP82-00850R000500070027-0

UDC 550.837/550.838/621.370

ELECTROMAGNETIC DETECTION OF ENGINEERING SERVICE LINES AND LOCAL ANOMALIES

Kiev ELEKTROMAGNITNOYE OBNARUZHENIYE INZHENERNYKH KOMMUNIKATSIY I LOKAL'NYKH ANOMALIY in Russian 1981 (signed to press 10 Dec 81) pp 2-5, 225-226

[Annotation, foreword and table of contents from book "Electromagnetic Detection of Engineering Service Lines and Local Anomalies" by Vladimir Ivanovich Gordiyenko, Vladimir Petrovich Ubogiy and Yevgeniy Vasil'yevich Yaroshevskiy, Izdatel'stvo "Naukova dumka", 1000 copies, 227 pages]

[Text] Annotation

This book presents a systems analysis of passive and active electromagnetic systems designed for detecting underground and underwater local anomalies and engineering service lines, for determining their depth and paths followed. The fundamentals of physical modeling of problems involved in terrestrial and maritime electromagnetic surveying are developed. An installation is described for harmonic-field monitoring of a broad class of problems. Results of the modeling investigations are presented. Industrially produced devices for detecting underground engineering service lines are described.

The book is intended for specialists involved in developing the theory and equipment for detecting engineering service lines and local anomalies.

76 illustrations, 10 tables, 215 bibliographic references.

[This book was reviewed by Ya.I. Burak and L.A. Koval']

Foreword

One of the main national economic problems associated with continuously developing civil and industrial construction and the extensive network of hydraulic structures is the detection of the branching underground and underwater network of service lines such as communications cables and various types of pipelines. This problem is difficult to solve because the various processes occurring in the ground and under water (chemical, electrochemical, geological, hydrodynamic, etc.) during extended operation causes the depth and position of these lines to change constantly.

Electromagnetic methods are used widely in detecting engineering service lines [2, 18, 19, 31, 55, 57, 59, 67, 82, 111, 139, 143, 154, 156, 163, 164, 169, 170]. However, regardless of the abundance of methods and devices used to carry out these tasks, their efficiency remains low, and the data provided remains ambiguous.

All of the existing instruments described in [7, 124] can only be used to test depth discretely, i.e., at particular points along a cable while the operator making the measurements is stopped; in addition to electrical calibration, most of these devices require that the primary transducer be moved mechanically across the cable path during each measurement.

No standards have been set for the basic error of series-produced instruments for determining depth [7,124], i.e., these are essentially indicating rather than measuring instruments, which do not provide good performance in monitoring depth and correcting cartograms.

These shortcomings in measuring devices make it significantly more difficult to do the required amount of work in making depth measurements and finding cable paths; these shortcomings are generally caused by imperfection in the measurement methods upon which the devices are based, as well as imperfection in the primary and secondary transducers. Task of developing new methods and means for determining routing and providing continuous depth monitoring with sufficient accuracy therefore remains urgent.

Theoretical questions relating to the creation of electromagnetic devices for detecting and testing the condition of underwater pipelines and main communications cables are also underdeveloped [34, 33, 85, 161]. The primary attention of the authors is therefore focused on the development of principles and ways of constructing electromagnetic detection systems, by which we mean functionally closed autonomous structures which represent as a unified whole all of the interconnected functional units, and which ensure execution of the required task.

The first chapter analyzes electromagnetic systems for determining the routing and depth of engineering service lines carrying alternating current. A classification is given for the induction method of measuring the depth of service lines by means of contact excitation of the latter. Existing and developed structural versions of primary measurement transducers are examined, and requirements are formulated which an electromagnetic system for determining the coordinates of engineering service lines must satisfy.

The second chapter analyzes active systems for maritime electromagnetic surveying using a low-frequency harmonic field, which contain dipole radiators and differential receivers, in order to establish rational geometry alternatives.

The methodical errors of these systems caused by geometric instability during electrical surveying work in motion are investigated.

The third chapter explains the theoretical foundations of physical modeling of problems of marine geophysical surveying using a harmonic field, and presents the basic indicators and similarity criteria which determine the interconnection between the working frequency, linear dimensions, electrodynamic parameters and electrical and magnetic field values under actual conditions and in the model. Requirements are formulated for the electrical and design parameters of models of the radiating and receiving elements, and conditions for modeling problems of detecting engineering service lines are defined.

The fourth chapter is devoted to a description of a modeling setup developed by the authors which is characterized by a high degree of automation of the amplitude-phase and relative (impedance, admittance or dimensionless) measurements and recording of the investigation results. This setup has expanded functional capabilities and supports investigation of a broad group of problems in underground and maritime electrical surveying using a harmonic electromagnetic field.

The fifth chapter consists essentially of an analysis of the results of modeling investigations of active electromagnetic marine surveying systems designed for detecting underwater pipelines and local anomalies on the ocean bottom.

The results of theoretical and experimental investigations and conclusions from their analysis contained in the first five chapters of the monograph have served as the basis for developing passive and active systems for detecting and modeling the coordinates of engineering service lines and local anomalies, for which the functional diagrams are described in the sixth chapter.

The seventh chapter is devoted to a description of expanded functional capabilities and schematic diagrams of instruments which are being used in practice and which were developed with the participation of one of the authors.

Chapters 1 and 7 were written by Ye.V. Yaroshevskiy, and 2 and 3 by V.I. Gordiyenko and V.P. Ubogiy jointly. The authors contributed equally to writing the fourth, fifth and sixth chapters.

The authors will be pleased to receive any remarks on this work, which should be addressed to the Physical-Mechanical Institute of the Ukrainian SSR Academy of Sciences (L'vov, 47, ul. Nauchnaya, 5).

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6900
CSO: 1860/239

ELECTRON DEVICES

UDC 621.385 (03)

DOMESTIC RECEIVING AND AMPLIFYING TUBES AND THEIR FOREIGN ANALOGS

Moscow OTECHESTVENNYYE PRIYEMNO-USILITEL'NYYE LAMPY I IKH ZARUBEZHNYYE ANALOGI (SPRAVOCHNIK) in Russian 1981 (signed to press 13 Jul 81) pp 2-4, 455-456

[Annotation, foreword and table of contents from book "Domestic Receiving and Amplifying Tubes and Their Foreign Analogs (A Handbook)", by Boris Vladimirovich Katsnel'son and Aleksey Stepanovich Larionov, Energoizdat, 100,000 copies, 456 pages]

[Text]

Annotation

This handbook presents information on domestic receiving and amplifying tubes which are widely used in modern radio equipment (low-noise, pulsed, tubes for color televisions, movable-electrode tubes, high-reliability tubes), as well as foreign tubes which are analogs of the domestic versions. In contrast to the 1974 edition, the present edition includes information on new tubes; information on obsolete tubes with limited use has been eliminated.

The book is intended for specialists involved in developing and operating radio-electronic equipment, and may also be useful to students of institutes of higher learning and technical training schools during course and diploma design.

[This book was reviewed by N.V. Parol'.]

Foreword

Modern electronic devices are distinguished by high quality, improved reliability and service life, as well as significantly improved parameters and characteristics.

Extremely modern electronic vacuum devices of various classes are now in production, including receiving and amplifying tubes which are widely used in measurement, medical and domestic radio equipment and in widely varying receiving and transmitting devices. Since these devices are reliable and have good parameters, the receiving and amplifying tubes will be in extremely wide use for a long time, which is confirmed by the experience of many other countries. This is necessary both to ensure the usability of industrial and domestic devices produced earlier, and also in connection with the fact that the conditions do not yet exist for replacing all tubes in many types of equipment.

The significant expansion in international scientific and technical cooperation, rapid development of export and import of electronic equipment and international cooperation in the area of television determine substantial interest on the part of a wide group of readers in questions of the interchangeability of domestic and foreign tubes.

The third edition of the handbook contains information regarding 340 domestic receiving and amplifying tubes, as well as their foreign analogs produced in the SEV [Council of Mutual Economic Assistance] member countries. These tubes are used widely, and data on their parameters and properties are needed by specialists, as well as radio amateurs, students, and consumers who use domestic radio equipment, since the tubes in television sets, radio receivers and other widely used radio devices can be changed by nonspecialists.

In contrast with the preceding edition, the handbook has been revised and supplemented significantly. Over 90 new types of devices have been added, including color television tubes, high reliability tubes, a number of original devices with special properties, including electronic movable-electron tubes, as well as certain widely used foreign tubes. In addition, the handbook contains important changes and clarifications associated with improvement in the parameters of more than 100 tubes.

Because of space limitations, the present edition of the handbook does not include obsolete types of limited-use tubes; the reference data on a number of other tubes are presented in slightly abbreviated form, without graphic characteristics.

For convenience in using the handbook, all of the tube nomenclature is conventionally divided into sections which combine the lamps in terms of number of electrodes (diodes, triodes, pentodes, etc.); within the sections tubes are grouped in terms of operating properties, for example 6P14P, 6P14P-V, 6P14P-YeV.

Many of the tubes produced in various countries have identical or very close parameters and dimensions and like function and can be interchanged in equipment. These tubes are usually called analogs. Various modifications of the same types of tubes, e.g., long-life tubes, are sometimes produced both here and abroad. These varieties of tube analogs which differ in terms of some special properties are not included in the groups of tubes in the handbook; only the parameters of the basic tube are given.

The analogs of domestic tubes are indicated for their type designation. Evaluating the conditions for interchangeability of tubes in certain types of equipment, depending upon the application and operating conditions, requires examining more extensive data than are provided in the present handbook.

In addition to complete analogs, which can be exchanged with no circuit or mode changes without disturbing performance, there are also similar tubes which differ in their base-connection diagram, design configuration or certain parameters. Interchanging tubes such as these requires modifications of the equipment, for example, resoldering board contacts, replacing resistors, etc. Such tubes are sometimes called "partial analogs". The most commonly used types of such foreign tubes, which have close parameters, are also included in the handbook.

The information on analogs are based on SEV data, company catalogs, foreign handbooks and other materials.

The handbook was compiled using standards in effect in the USSR, general technical specifications for receiving and amplifying tubes, operating recommendations and other technical documentation.

The following information is given for each tube:
--type designation;
--size and weight;
--basic electrical and other parameters;
--nominal parameter measurement mode;
--limiting operational data, including resistance to external effects.

In addition, the electrode-pin connection diagram is given for each group of tubes, as well as standard averaged anode and anode-grid characteristics. Scale drawings of the tubes are presented at the end of the book.

This handbook does not replace official documents (standards and analogous technical documents) which set requirements for tubes and determine their performance.

The preceding edition of the handbook engendered definite interest on the part of radio amateurs and specialists. The authors are grateful to readers who submitted their suggestions and remarks, most of which were able to be incorporated in the present edition. The author is also grateful to Docent Candidate of Technical Sciences N.V. Parol' for his valuable remarks and advice provided during editing of the manuscript.

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6900
CSO: 1860/222

MICROWAVE THEORY & TECHNIQUES

UDC: 621.317.72

INTEGRATED 10-BIT SEQUENTIAL APPROXIMATION ANALOG-DIGITAL CONVERTER

Moscow PRIBORY I TEKHNIKA EKSPERIMENTA in Russian No 1, Jan-Feb 82 (manuscript received 31 Mar 80) pp 115-117

[Article by A. I. Antonevich, V. V. Butskiy and A. M. Sarzhevskiy, Belorussian State University, Minsk]

[Text] This article describes a 10-bit analog-digital converter built with 6 integrated circuits and 2 stabilizer diodes. The conversion time is 32 μsec, input signal range —10 mV—10 V, conversion nonlinearities 0.1%.

Analog-digital converters which use the sequential approximation or bit-weighting method provide high resolution and high speed [1,2]. Series production has now begun of the K155IR17, K572PA1, K521SA3 and K597SA3 microcircuits, which can be used to build high-performance analog-digital converters with simple configurations (cf. figure).

To begin with, let us consider briefly the function and operating principle of these microcircuits. The K155IR17 microcircuit is a 12-bit sequential approximation TTL register which is used as a controller in analog-digital converters. This register is examined in sufficient detail in [3,4]; however, some clarifications are needed. First of all, applying the logical zero level to the $\overline{S}$ input sets all of the auxiliary flip-flops of the register to "1", i.e., prepares it to operate. In order to start writing the information in the register, the "1" level must be applied to the $\overline{S}$ input. As a result, the leading edge of the first timing pulse causes the primary high-order bit flip-flop to switch to state "0", and the flip-flops of the other bits to "1". Secondly, when all of the bits have been filled, the register switches to the data hold mode until a "1" reaches the $\overline{S}$ input. The $\overline{E}$ is used to write a "1" in the high-order bit and to block data from being written in the remaining bits. The K572PA1 microcircuit is a 10-bit digital-analog converter which converts reference voltage to current whose value depends upon the digital code applied to the inputs of the circuit. The control signal levels are the same as for TTL circuits. K521SA3 [5] and K597SA3 microcircuits are designed to operate as precision voltage comparators with high maximum achievable differential and phased voltages (>10 V).

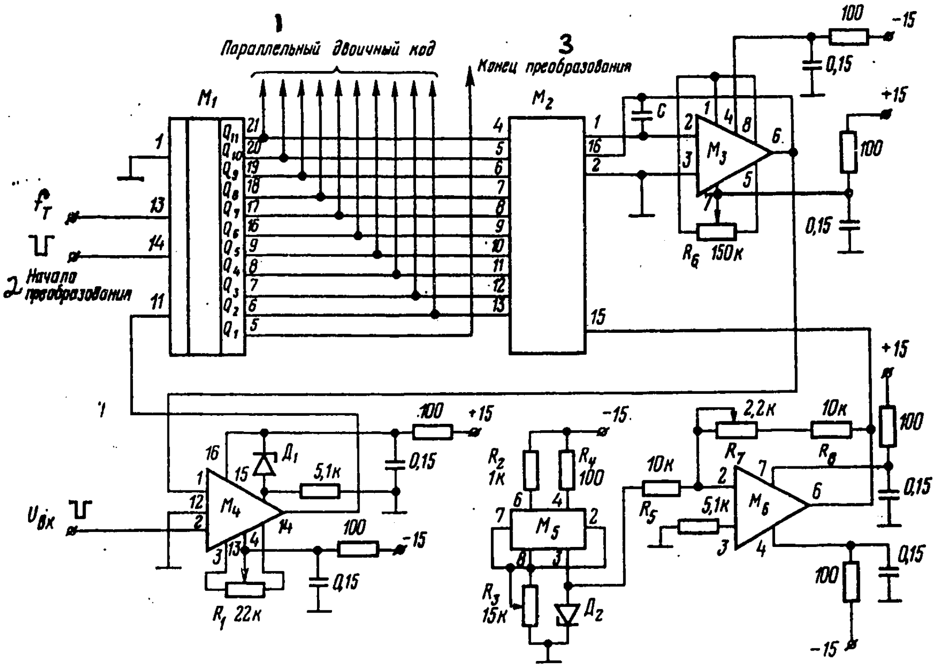

Figure. M_1-K155IR17, M_2-K572PA1A, M_3-K544UD2A, M_4-K597SA3, M_5-K159NT1V, M_6-K140UD7; D_1-KS210Zh, D_2-KS191F. Adjusting resistors R_1, R_3, R_7-SP5-14, R_2, R_5, R_8-S5-55, R_4-S5-5-1, R_6-SP3-19. Others - OMLT-025; capacitors-KM6; 1, parallel binary code; 2, start conversion; 3, end conversion.

The analog-digital converter (cf. figure) consists of 6 microcircuits and 2 stabilizer diodes. Input signal U_{in}, which is a negative-going pulse with length equal to the conversion time, is applied to the inverting input of comparator M_4 and compared with the signal coming from the output of the digital-analog converter. The digital-analog converter is made up of reference voltage source with microcircuits M_5, M_6, reference voltage-to-current converter using M_2 and current-voltage converter using M_3. The reference voltage is set by resistor R_7, and consists of having voltage of —10.23 V at the input of M_3 when a logic 1 supplied to all of the control inputs of M_2. Resistor R_6 balances the bias voltage of M_3, while capacitor C corrects the voltage set time at the input of the digital-analog converter U_{dac}. The value of this capacitance is refined during alignment of the analog-digital converter, and is between 10 and 30 pf.

The signal from the output of M_4 is applied to the D-input of microcircuit M_1 and controls writing 0 or 1 in the primary flip-flops of the register. During the 11th cycle from the beginning of conversion, register output Q_1 produces a negative-going End of Conversion signal which is used to read the code obtained. The conversion time of the analog-digital converter is thus $T_{co}=11/f_t$, where f_t is the timing frequency. The value of f_t depends upon the speed of the register and of the digital-analog converter. According to [3], f_t=15 MHz for K155IR17. However, the set time in the K572PA1 microcircuit with U_{dac}=5 V (weight of high-order bit) is approximate 2.5 μsec. Therefore, f_t was selected as 350 KHz, so that T_{co}=32 μsec. The length of the triggering signal is 3 μsec, with negative polarity.

This analog-digital converter has the following basic characteristics: input signal range 10 mV-10 V; polarity - negative; output code - parallel 10-bit; differential nonlinearity 0.1% of total scale; integral nonlinearity of scale 0.1%; conversion time - 32 μsec; temperature drift 50 μ/°C; input impedance 10 KΩ. This analog-digital converter is used in a device which transmits data from an instrument used to measure scintillation-type signals to an "Elektronika-D3-28" microcomputer.

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FUNCTIONAL TESTING OF LOGIC CIRCUITS BY EXHAUSTIVE SAMPLING OF PERMITTED STATE

Moscow MIKROELEKTRONIKA in Russian Vol 11, No 1, Jan-Feb 82 (manuscript received 9 Sep 80) pp 45-53

[Article by G. Kh. Novik, All-Union Scientific Research Institute of Electromechanics]

[Text] Functional testing of logic circuits, especially microcircuits, is extremely important in ensuring high quality of electronic equipment. This problem is now being solved with the help of the cumbersome, expensive equipment involved in traditional methods of recording the output responses of tested logic circuits. However, non-traditional methods of recording the output responses of tested circuits, in particular the signature analysis method [1], make it possible to realize compact, flexible equipment, in quantity, for functional testing of logic circuits which is so necessary for the acceptance testing by bulk users of microcircuits and which is based on the proposed method of exhaustive linear sampling of permitted inputs.

This method is based on the use of signature analysis, with which it is possible to "compress" binary sequences of practically any length to short sequences 16 bits (i.e., four hexadecimal digits) long - data series or code signatures with extremely high accuracy $(1 - 1/2^{16})$ which characterize the original "compressed" binary sequences. The output response signature obtained in testing a logic circuit is compared with a standard signature which has been verified experimentally. The result of the comparison is the criterion for correct functioning of the microcircuits. Since in the case in question the length of the output binary sequence (output binary vector) is practically irrelevant, and the number of input test sets may also be fairly large, it is possible to do a complete linear sampling of the input states except, of course, for any possible forbidden states. The main shortcoming of the exhaustive sampling method is that the test cycle takes more time than, for example, the use of minimized test procedure sets. However, for a large class of microcircuits, there are no more than 28 leads on the case. Since two leads are generally used for power, and no more than 8 leads serve as outputs, we can assume that the number of leads serving as inputs does not exceed 20. Even at a timing frequency of 2 MHz, the sampling frequency of each output is 2 $MHz/2^{20}$ = 2 Hz, i.e., the test cycle takes 0.5 seconds. For microcircuits in cases with 14-16 leads, this time amounts to fractions of milliseconds.

Figure 1 shows an expanded flowchart of a test algorithm which serves for both combination and serial microcircuits. The algorithm includes analysis of the truth table of the microcircuit, linear connection of the microcircuit inputs to the outputs of the test generator, which is based on a binary counter, formation of a separate binary output vector for each output of the tested circuit, analysis of the binary vector obtained, machine analysis of the signature of the vector and experimental verification on a known good microcircuit. (If the analytical and experimental results differ, the truth and switching table must be reanalyzed, and the wiring of the switch must be checked.) Since the length of the output binary vector is practically irrelevant, the output sequences from all of the outputs of the tested circuit can be automatically multiplexed, i.e., the binary vectors from all of the outputs can be arranged in a single common output vector whose length is a multiple of the number of outputs, obtaining the overall signature of the microcircuit case by "compressing" that overall vector, which simplifies the test procedure significantly by reducing it to recording only the overall signature. The capability still remains of doing output diagnostics by recording the signatures for each output.

Combination-Type Logic Microcircuits

In accordance with the common expanded algorithm, the truth table of the tested circuit is analyzed from the viewpoint of classification of the type of function it executes (combination, serial). If the circuit in question is a combination circuit and has no special additional inputs (two-phase OR expansion inputs in TTL circuits, and single-phase inhibit inputs), its inputs are connected to the outputs of the input signal generator in arbitrary order. Each subsequent input of the tested microcircuit is controlled by a signal having a repetition frequency which is half that of the preceding input. The signal at the final input, which has the lowest frequency, is the "start/stop" signal for the signature analyzer and determines the length of the measurement window. The microcircuit section with a given output implements its function once during the measurement interval. The preceding sections of the microcircuit being tested realized their functions repeatedly, since the frequency of their input signals is higher, i.e., they are tested redundantly, and the output vector of the corresponding section of the microcircuit will contain periodically repeating components. The output vector corresponding to each output in this case is formed "manually" using the heuristic approach. The truth table and switching (distribution) scheme of the outputs is used to do this. The overall binary vector of the microcircuit is formed by compiling and arranging the vectors of each output sequentially. If the number of outputs of the microcircuit is a multiple of a power of two, the common output vector is composed of only the binary vectors of each output. If the number of outputs of the case being tested is not a multiple of a power of two, the common output vector is made up by adding a "ones" vector to the vector comprised of the binary vectors from the individual outputs. This ones vector has a number of ones equal to the length (in the sense of the number of cycles) of the measurement window for an individual output. The output binary vector obtained from the time diagram is analyzed for correspondence to the truth table, i.e., for correspondence between the output response and the input signals. If the correspondence is present, the signatures are then computed by machine. In order to do this, the binary vectors are represented in a fairly simple input language which defines the number of ones and zeros in a row in the form $\ldots N_0 + K_1 + L_0 + M_1 + \ldots$. If a vector contains periodic components, it can be represented by expressions of the form $D(B(N_0 + K_1) + L_0 + \ldots$, where D, B, N, K, L, M, ... are decimal numbers with subscripts indicating the type of binary information (0 or 1). A plus means that the indicated numbers of zeros or ones is "built up" sequentially. Constants without subscripts indicate the number of repetition cycles contained in parentheses, of the periodic components of the binary vector. The computed signature values are compared with experimental values obtained using a group of known good circuits. When they agree, the set of input test signals is assumed to be completely correct, albeit redundant. The signatures obtained are kept for the signature library and entered on the test chart.

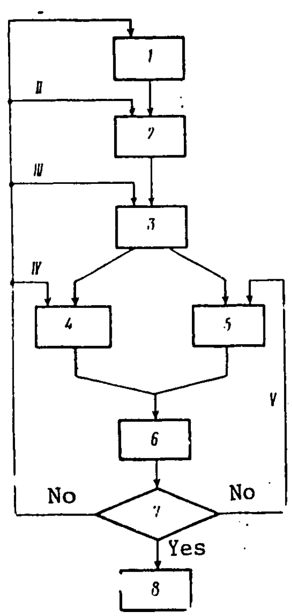

Fig. 1

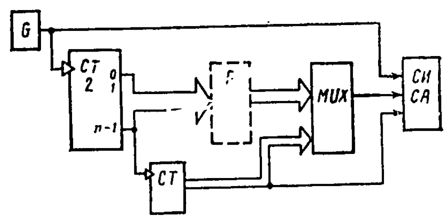

Fig. 2

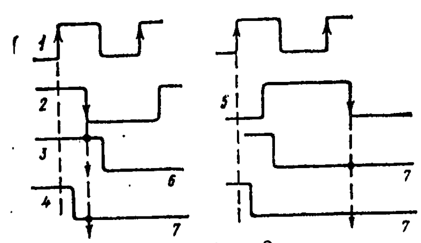

Fig. 3

Figure 1. General flowchart of algorithm used to form binary output vectors and signatures for logic circuits: 1--truth table analysis; 2--connection of tested circuit inputs to driver outputs; 3--formation of binary output response vectors of each output of tested circuit; 4--computation of signatures of output binary vectors and overall signature of case; 5--experimental measurement of signatures of binary output vectors of each output and overall signature of case; 6--analysis of agreement between computed and experimental data; 7--corresponds to "?", 8--inclusion in tested microcircuit library and output of test chart; I --truth table analysis error; II--rearrangement of inputs; III--output response formation error; IV--input error; V--switch wiring error.

Figure 2. Connection of tested logic circuit (F) to driver-counter (CT_2), multiplexer (MUX) and signature analyzer (CA).

Figure 3. Prevention of undefined situations in strobing data reception into flip-flop register by inverting low-order counter-driver signal: 1--main sync signal; 2--CT_0 (strobe input); 3--CT_1 (input D) -- switching later than CT_0; 4--CT_1 (input D) -- switching earlier than CT_0; 5--CT_0 inversion (strobe input); 6--1 received; 7--0 received

If the computed and experimental signatures do not agree, the wiring of the switch is checked carefully once trivial errors in manual input of data regarding the binary vector components have been eliminated. The adequacy of the input signals can be monitored by oscillograph during the experiment. In addition, the binary vector from each output is checked for agreement with its truth table and with the switching scheme of the line switch.

If a combination circuit has additional special-purpose inputs, e.g., two-phase OR expansion inputs for TTL circuits, an OR expansion microcircuit is connected to the inputs of the tested circuit; one of the inputs of the expansion circuit is connected to the high-order bit of the output of the signal generator, and the other inputs are connected linearly to the inputs of the generator. The rest of the process by which the output binary vectors are formed is analogous to that explained above for combination circuits. The periodicity of the output vector components change, since the input of the OR expander does not act upon the microcircuit during the first half of the measurement interval, and it usually blocks the operation of all other inputs during the second half. When a microcircuit being tested has an inhibit input, there is no need to connect additional elements. Depending upon the input signal level (active, null, unity), the microcircuit is tested in the functional sense either during the first half of the test period, or during the second, which is of no special importance.

Output vectors can be formed for various sections of a combination microcircuit by implementing the conception of exhaustive linear sampling of input signals from a natural binary counter (figure 2) in which the output signals of the binary counter are represented as periodic binary vectors. If a combination circuit (AND, OR, NAND, NOR) with n inputs is being tested, these inputs must be controlled by using counterbits 0, 1, 2...i, ... (n - 1). Designating the switching time of bit 0 as a sequence of 10 and 11, i.e., $1_0 + 1_1 = 2_0^0 + 2_1^0 + 2_{0/1}^0$ (where the plus sign indicates sequential arrangement), the second-bit switching period $2_0 + 2_1 = 2_0^1 + 2_0^1 = 2_{0/1}^1$, and the ith bit switching period 2 [text garbled - Tr.] we obtain a length for the measurement interval formed by the (n - 1) th bit of $2_0^{n-1} + 2_0^{n-1} = 1 \cdot 2_{0/1}^{n-1} = 2^0 \cdot 2_{0/1}^{n-1}$ (where the multiplication symbol indicates the number of sequential periods). Accordingly, the number of i-bit periods per measurement interval period is $2^{n-1-i}:2_{0/1}^{i}$ $(2^{n-1-i+i+1} = 2^n)$. For bit 0 (i = 0), the number of periods is $2^{n-1}.2_{0/1}^{0}$ $(2^{n-1+0-1} = 2^n)$. If a k-input AND gate with its kth input driven by bit i of the counter-driver is being checked in a tested case with n inputs, the measurement window will obviously be $2^{n-1-i}.2_{0/}^{i} = 2^n$ cycles. The ones components of the output vector will be determined by the (i - (k - 1))-output of the driver, and the output vector of the AND gate in question will be defined by the expression

$$2^{n-1-i}\cdot(2_0^{i}+2_0^{i-1}+\ldots+2_0^{i-(k-1)}+2_1^{i-(k-1)})$$

or

$$W_{AND}=2^{n-1-i}\left(\sum_{j=1}^{k}2_0^{i-(j-1)}+2_1^{i-(k-1)}\right).$$

Accordingly, the output vector for an NAND gate will be

$$W_{\overline{AND}}=2^{n-1-i}\left(\sum_{j=1}^{k}2_1^{i-(j-1)}+2_0^{i-(k-1)}\right).$$

For a k-input OR gate

$$W_{OR}=2^{n-1-i}\left(2_0^{i-(k-1)}+\sum_{j=1}^{k}2_1^{i-(j-1)}\right).$$

For a NOR circuit

$$W_{\overline{OR}}=2^{n-1-i}\left(2_1^{i-(k-1)}+\sum_{j=1}^{k}2_0^{i-(j-1)}\right).$$

Table 1

Binary Vectors and Signatures of K155LI1 Microcircuits

Element	Window	Output	Signature	Output binary vector
D1.1	256	3	2P36	$64\ (3_0+1_1)=n_1$
D1.2	256	6	9F79	$16\ (12_0+4_1)=n_2$
D1.3	256	8	1108	$4\ (48_0+16_1)=n_3$
D1.4	256	11	A7OF	$192_0+64_1=n_4$
Case	1024	–	79U7	$n_1+n_2+n_3+n_4$

As an example, let us examine the testing of a simple combination microcircuit consisting of four two-input AND gates without auxiliary function expansion or case select inhibit inputs. (The total number of inputs n = 8, with each AND gate having k = 2 inputs.) The truth table of this microcircuit is elementary -- the output of each section is the conjunction of two inputs.

In agreement with the general methodology, this microcircuit is tested functionally and parametrically by inputting the signals from the 8 outputs of a counter-driver (cf. figure 2) linearly to all of its 8 inputs.

The sync signal for the analyzer is the counter-driver triggering sync signal. The "start/stop" signal in this case is either taken from the output of the eighth bit of the counter-driver, corresponding to a window of $2^8 = 256$ for measuring the signatures of each output separately, or from the output of the second bit of the counter-multiplexer for measuring the overall signature which corresponds to a sync signal cycle window of $2^{10} = 1024$.

The procedures by which the output binary vectors are formed for each AND gate are presented below.

AND gate No.	i	Output vector formation
1	$i=1$	$2^{8-1-1}\left(\sum_{j=1}^{2} 2_0^{1-(j-1)} + 2_1^{1-(2-1)}\right) = 2^6(2_0^{1-(1-1)} + 2_0^{1-(2-1)} + 2_1^{1-(2-1)}) = 64(2_0^1+2_0^0+2_1^0) = 64(3_0+1_1)$
2	$i=3$	$2^{8-1-3}\left(\sum_{j=1}^{2} 2_0^{3-(j-1)} + 2_1^{3-(2-1)}\right) = 2^4(2_0^{3-(1-1)} + 2_0^{3-(2-1)} + 2_1^{3-(2-1)}) = 16(2_0^3+2_0^2+2_1^2) = 16(12_0+4_1)$
3	$i=5$	$2^{8-1-5}\left(\sum_{j=1}^{2} 2_0^{5-(j-1)} + 2_1^{5-(2-1)}\right) = 2^2(2_0^5+2_0^{5-1}+2_1^4) = 4(48_0+16_1)$
4	$i=7$	$2^{8-1-7}\left(\sum_{j=1}^{2} 2_0^{7-(j-1)} + 2_1^{7-(2-1)}\right) = (2_0^7+2_0^{7-1}+2_1^{7-1}) = 192_0+64_1$

The first AND gate is checked in four cycles, during which its truth table is checked fully (and redundantly). There are 256/16 = 16 check cycles for the second AND gate (15 of which are redundant), 256/64 = 4 (3 redundant) for the third, and 256/256 = 1 for the fourth (none redundant).

The complete vector for the case with a window of 1024 will equal

$$W=64(3_0+1_1)+16(12_0+4_1)+4(48_0+16_1)+192_0+64_1.$$

Table 1 shows the experimentally verified signatures for a K155LI1 microcircuit. The duration of a single test with a sync signal frequency of 2 MHz and a 1024-cycle interval is approximately 1 msec (2·1024·0.5 μsec), i.e., approximately 1,000 tests can be made in one second.

Sequential Logical Microcircuits

The algorithm used to form the input test procedures for sequential microcircuits also includes exhaustive linear trial of input signals. In doing this, the truth table of the circuit is analyzed and the inputs of the microcircuit are distributed among the outputs of the input signal generator, or counter. In this case, the inputs are distributed such that the low-order bits which are switched at high frequency are connected to the sync inputs of the test circuit, and the high-order bits which are switched at the lowest frequency are connected to the mode set, case select, etc., inputs. Although the exhaustive linear sampling principle is retained for sequential circuits, they have some singular features due to the use of memory elements which may result in the presence of certain forbidden states, i.e., the simultaneous application of active signals to certain inputs results in an undefined state at some outputs. An example of this is the "add" and "subtract" sync signal inputs in reversible counters, the "suppress" and "set" of flip-flops or registers, etc. Since the main unit in the input signal generator is a natural binary counter, the states of its individual bits will sometimes coincide, and the signals which result when this happens are unacceptable. Forbidden states are avoided by introducing a binary decoder which provides pulsed signals which are separated in time and which have the same width as the signal from the low-order bit of the generator counter.

The functioning logic of sequential-type microcircuits may in some cases be such that dynamic competition may arise between individual internal elements. For example, if the register number accept strobe signal is in phase with the signal from the input signal generator at the data input, and reception is done using a slice of the sync signal, the synchronous nature of the switching of the counter bits causes the switching moments to lead or lag behind one another. The trailing edge of the sync signal may therefore land in the null state of the following bit if it is switched earlier, and in the ones state if it is switched later (figure 3). Accordingly, either a zero or a one will be received for different cases of the same type. In order to prevent ambiguity, the signal applied to the "receive" sync input must be inverted. Once the initial distribution of the microcircuit inputs among the generator output has been corrected as indicated, the binary output vector of each output is formed separately, like in combination circuits, in the truth table function and distribution of the microcircuit inputs among the outputs of the driver. Correspondence between the truth table output vectors is then analyzed, i.e., analysis is done to see whether all possible switching combinations have been achieved for the outputs of the tested circuit; then the signatures are computed and measured experimentally, the computed and experimental data are compared and entered in the library, and the test chart is produced. If there are any disagreements, the distribution of the inputs must be checked and analysis must be done to see whether there are any forbidden states, whether decoders or other additional elements must be added and whether the signals from the individual generator bits must be inverted.

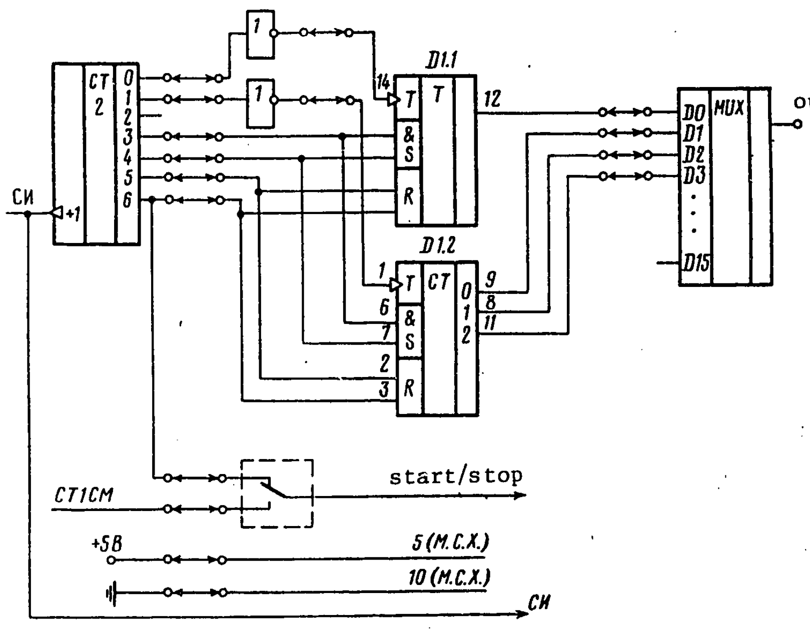

Figure 4. Connection of case of K155IE2 decimal counter

Let us examine the testing of a relatively simple K155IE2 asynchronous binary-decimal counter controlled by cutting off the input sync signal (1 → 0 pulse) and having the following operating modes: counting from 0 to 9 (sync signals at input 1 and input 14), reset (set to 0) (AND ing inputs 2 and 3), set "9" (AND ing inputs 6 and 7). Setting "9" takes precedence over reset and count, and reset takes precedence over counting. The case contains a flip-flop for the low-order bit of the counter (element D1.1) and a 3-bit counter (element D1.2) which counts from 1 to 4 (shifting "4" (100) to the left yields "8" (1000)), and 1 in D1.1 (001) yields 9 (1001) (in order to obtain a four-bit decimal counter the output of D1.1 must be connected to the inverting input of element D1.2, which will produce binary-coded decimal at the circuit outputs) (table 2).

Table 2

Signatures of K155IE2 Microcircuits

Item no.	Element	Output	Window	Signature
1	Г1.1	12	128	8836
2	D1.2	9	128	42AP
3	D1.2	8	128	FUA5
4	D1.2	11	128	1FOP
5	Case	–	512	CU65

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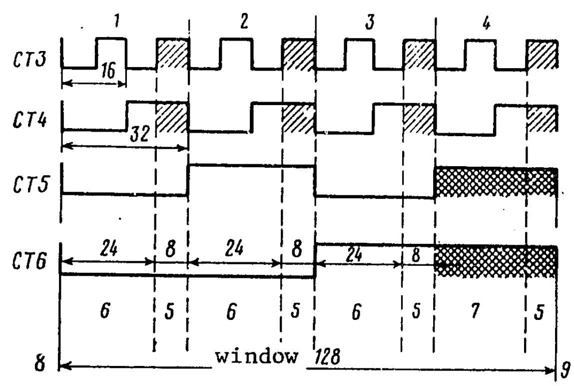
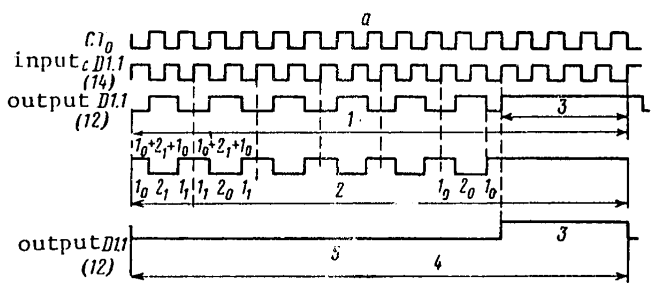


Figure 5. Test regions of K155 E2 microcircuit: 1--first 32 cycles; 2--second 32 cycles; 3--third 32 cycles; 4--fourth 32 cycles; 5--set "9"; 6--count; 7--set "0" (common); 8--start; 9--stop



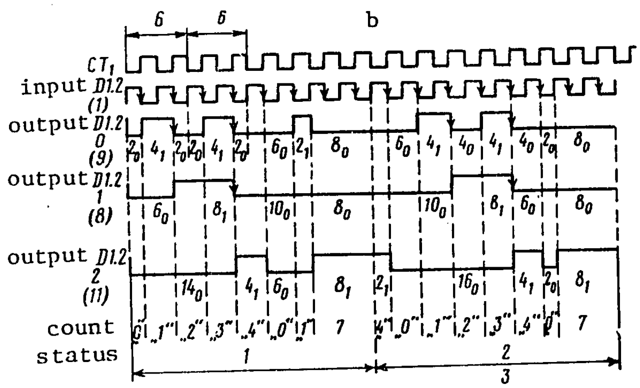


Figure 6. Diagrams of input/output signals during testing of K155IE2 decimal counter: a--for element D1.1; b--for element D1.2; 1--first 32 cycles; 2--second and third 32 cycles; 3--eight cycles - set "1" ("9"); 4--fourth 32 cycles; 5--reset; 6--eight cycles; 7--set "4" ("9")

In agreement with the general methodology, signals from the generator are applied to all six inputs of the microcircuit (figure 4). The signals from generator bits CTO and CT1 are inverted before being applied to the sync signal inputs in order to eliminate the influence of transient processes when the counter switches at times when the sync signals are being cut off. In addition, the third bit (CT2) of the counter is not used in order to lengthen the cycle and make sure that all switching combinations of the circuit are tested. Therefore, the seventh bit (CT6) is the high-order bit of the counter, although only six bits are used. The diagram in figure 4 also indicates the numbers of the contacts of the switch which switches the inputs/outputs of the tested circuit to the outputs of the generator and inputs of the multiplexer, switches the power and common bus, and switches "start/stop" signals to the inputs of the signature analyzer.

In the case in question, the "start/stop" signal is taken from the output of the seventh bit (CT6) of the generator, which corresponds to a window of $2^7 = 128$ for measuring the signatures of each output (without multiplexing), or from the output of the second bit (CT1) of the multiplexer counter to measure the overall signature, which corresponds to a window of $2^7 \cdot 2^2 = 2^9 = 512$. A time diagram of the measurements is shown in figure 5, where the regions of exhaustive trial of all input signals are shown for each element.

A window of 128 is distributed as follows: when the individual values of the last two bits (CT5, CT6) of the generator are the same, a zero-set signal is formed in the last 32 cycles (figure 6). When the individual values of the two preceding bits (CT3, CT4) are the same, a nine-set signal is formed; this signal is narrower (eight cycles) and is generated four times -- at the end of each group of 32 cycles.

During the first three 32-cycle groups, counting is thus permitted only during the first 24 cycles, with "9" being set in the last eight cycles of that group, i.e., the low-order bit is set to "1". The binary output vector of the low-order bit appears as

$$n_1 = \underbrace{6(1_0 + 2_1 + 1_0) + 8_1}_{\text{first 32 cycles}} + \underbrace{2(6(1_1 + 2_0 + 1_1) + 8_1}_{\text{second and third 32 cycles}} + \underbrace{24_0 + 8_1}_{\text{fourth 32 cycles}}.$$

For the remaining bits, respectively,

$$n_2 = 2(2_0+4_1+2_0)+6_0+2_1+8_0+2(6_0+2(4_1+4_0)+2_0+8_0)+32_0;$$
$$\bar{n}_4 = 14_0+4_1+6_0+8_1+2(2_1+16_0+4_1+2_0+8_1)+24_0+8_1.$$

The overall binary vector of the K155IE2 case with a window of 512 will be $n_5 = n_1 + n_2 + n_3 + n_4$. Table 2 shows the corresponding signatures of the K155 case.

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FUNCTIONAL SIGNATURE TESTING OF INTEGRATED CIRCUITS USED IN MAIN STORAGE USING DATA-SHIFTING METHOD ('MARSH' TEST)

Moscow MIKROELEKTRONIKA in Russian Vol 11, No 1, Jan-Feb 82 (manuscript received 21 Nov 80) pp 54-63

[Article by G. Kh. Novik, All-Union Scientific Research Institute of Electromechanics]

[Text] Testing the microcircuits used in main memories is one of the most important problems in modern digital technology. The use of microcircuits in main memory is increasing, and the information capacity of the memory chips themselves is growing as well. While the producers of microelectronic articles have sufficiently powerful, universal and efficient equipment, users (of which there are far more than there are producers) have practically no equipment for functional acceptance testing of LSI memory devices. This reflects on the quality of the industrial articles which they produce in quantity, and, accordingly, on the reliability of these articles and their operating efficiency.

The method used to test integrated memory circuits is based to a great extent on an analogous methodology borrowed from the theory and practice of testing classical magnetic core memory devices with rectangular hysteresis loops. The borrowing of this method fails to take into account a number of specific features inherent in microelectronic solid-state memory elements, and this is reflected in the testing. A memory microcircuit, like any other microcircuit, is characterized by a truth table of some degree of complexity. The states of this table are determined by the values of the signal at the output of the memory chip as a function of different combinations of select enable/inhibit, read/write signals input to the microcircuit. Traditional methods of testing memory circuits consist primarily of testing the value of the output signal only when information is being read (from different addresses, of course) while selection is enabled. It is therefore extremely important to develop a methodology and construct relatively simple equipment for functional testing of memory circuits with respect to the complete truth table, which is of great significance for consumers and developers of math-produced equipment who use memory circuits.

The industrial equipment now available for testing LSI memory devices is extremely cumbersome and expensive, requires highly qualified personnel to operate and is usually ased on the use of computers. These include such familiar devices as the Makrodeyt 104 [1], the Elekon [2] and the "Integral" AIS [automated information system] based on the "Saratov" computer [3], which cost this and hundreds of thousands of rubles since they are designed for both functional testing and direct precision measurement of electrical parameters, which users do not require for functional acceptance testing and which can be replaced with indirect parametric testing. The latter means the creation of "worst-case" conditions for the testing circuits with respect to their inputs and outputs, i.e., conducting their functional tests under full output RC load and driving the inputs at the maximum logical zero level and minimum logical one level of the input signals. The complexity of this equipment, which is due largely to the use of computers, makes it inaccessible to a large group of users, and often limits the size of memory which can be tested, and also increases testing time unacceptably. In particular, the "Integral" equipment based on the "Saratov" minicomputer takes approximately 30 seconds [3] for actual testing of a 64-bit memory (disregarding the time required to record the results) using a data shifting algorithm (the "Marsh" test). Since the time required for the "Marsh" test is approximately proportional to the capacity of LSI memory, 120 and 480 seconds (i.e., eight minutes) and 1920 seconds (32 minutes) are needed to test 256-bit 1K and 4K LSI memories, respectively, while a 16K and 64K LSI memory takes 128 minutes (two hours) and eight hours, respectively, which is, of course, unacceptable. Furthermore, only one of the four states of the LSI truth table is tested; thus, the problem of creating new methods and new mass-produced equipment based on them for direct functional testing (and indirect parametric testing in the indicated sense) becomes obvious and urgent.

The ideology and equipment for functional testing of small-, medium- and especially large-scale integrated circuits [4] which has been developed on the basis of using signature analysis can also be used effectively for testing memory circuits, to which the present material is devoted. This ideology is aimed toward simplifying LSI memory testing equipment significantly by eliminating the use of computers and their programming, reducing LSI memory testing time so that it does not exceed more than fractions of seconds for LSI memory chips regardless of capacity and organization, and increasing test reliability by ensuring that output responses are tested for all of the truth table states of the circuits being tested.

The general assumptions involved in testing integrated circuits by exhaustive linear trial of permitted input effects using signature analysis to record the output responses by compressing binary vectors of arbitrary length to short signatures -- four hexadecimal digits -- is explained in [4]. In accordance with these general assumptions, the basis of the source of the input test sequences which is used in order to implement the "Marsh"-type test is a natural binary counter triggered by a sync signal generator in which defined bits are connected directly to all of the inputs of the tested LSI case, except for the select enable input (RV) and read/write mode control input, to which the counter bit is connected directly or indirectly in the case of the $\overline{\text{WRITE/READ}}$ input, or through an inverter in case of the WRITE/READ input.

The data shifting test ("Marsh" test) belongs to the class of $\alpha 2N$ tests (where N is the memory capacity and α a constant). A defined background ("1" or "0") is first read into all of the addresses in the memory field; then the background data is read from each address one at a time and replaced at each address with its opposite, which remains in the tested locations as subsequent addresses are tested (the test, so to speak, leaves a trail); the background is reversed as the test proceeds (if the background data consisted of ones, it is replaced upon being read out with zeros, shifting from a zero address to the next (N - 1) address against the background of the replaced ones). After all zeros have been written in the memory field as a result of the first half of the test, the field will then be read during the second half of the text, with ones being written in each current location, as if it were shifted from the null address to the subsequent (N - 1) address against the background of the replaced zeros. There should thus be two operations - READ and WRITE - in each current address; the input data should be reversed during the first and second passes through the memory field.

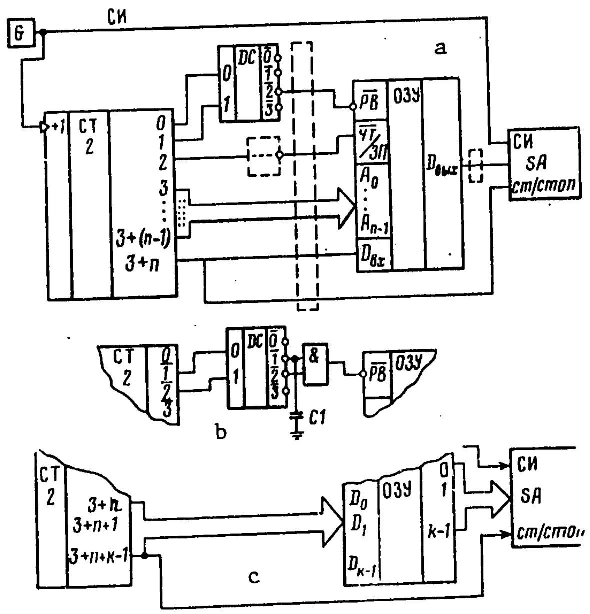

Figure 1. Testing LSI memory using Nx1 MARSH test in READ and WRITE mode (a); in READ - CHANGE - WRITE mode (b); for LSI memory with NxK organization (c).

The circuit in which the input signal source is connected to the inputs of an Nx1(k) LSI memory chip and with n-address lines ($N - 2^n$) (figure 1) implements this MARSH test algorithm completely using simple hardware, since the output responses are registered by a signature analyzer whose data input receives the output signals from the tested LSI memory during each system sync signal cycle without exception. The measurement "window" in the signature analyzer is formed

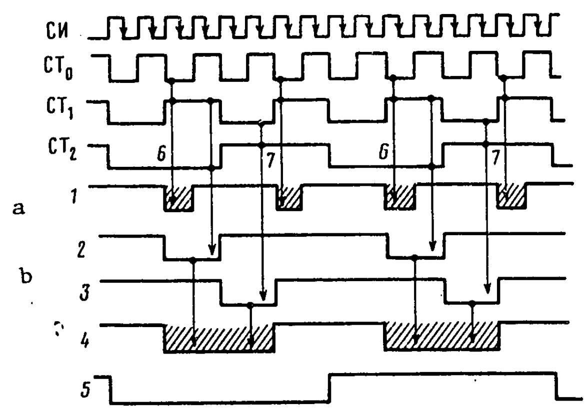

Figure 2. Time diagram of formation of select enable signals (RV) in READ and WRITE mode (a); in READ - CHANGE - WRITE mode (b): 1--$\overline{RV}$ READ and WRITE mode; 2--status $\overline{1}$ of bits ST_1 & ST_2; 3--status of $\overline{2}$ bits ST_1 & ST_2; 4--$\overline{RV}$ READ - CHANGE - WRITE mode; 5--low-order address; 6--read; 7--write

for the START/STOP input by the last bit of the counter-driver which is used; that bit is also used to drive the data input of the tested LSI device, so that the "window" includes the entire cycle during which the data change in the sequence 0 → 1.

The select enable signal $\overline{RV}$ is formed by a 2 → 4 binary decoder, to the two inputs of which a pair of the three low-order bits of the generator ("0" and "1" or "1" and "2") can be applied. The binary decoder produces sequential signals corresponding to the decoded status of two of its inputs: $\overline{0}$, $\overline{1}$, $\overline{2}$, $\overline{3}$. The length of these signals is a multiple of the cycle length (one period) of the sync signals produced by the timing generator in the system. If output bit "0" and "1" from the generator are applied to the inputs of the decoder, the length of the signals at the output of the decoder is one cycle. If counter bits "1" and "2" are applied to the inputs of the decoder, the length of the signals at the outputs of the decoder is two cycles which, as will be shown below, is required for forming different select enable signals $\overline{RV}$. The decoder output signals have active zero value because of the particular hardware used. The signal $\overline{RV}$ is formed differently depending upon mode: READ and WRITE (select enable signal $\overline{RV}$ is separate for the READ instruction and for the WRITE instruction) or READ - CHANGE - WRITE (where the $\overline{RV}$ signal is common for the READ - WRITE instruction cycle). In the READ and WRITE mode, the $\overline{RV}$ signal is the output state "$\overline{2}$" decoded by the decoder when counter bits "0" and "1" are applied to the inputs; in the READ - CHANGE - WRITE mode the $\overline{RV}$ is formed when the two states "$\overline{2}$" and "$\overline{1}$" combined by the two-input AND gate apply counter bits "1" and "2" to the inputs of the decoder (figure 1b), which provides a double width $\overline{RV}$ signal. (In order to prevent "gaps" in the middle of the $\overline{RV}$ signal at state output "1", it is shunted by a small capacitance of 150-200 pF, which eliminates any effect from differences in the length of the processes involved in switching decoder outputs "1" and "2".) This formation of the select enable signal $\overline{RV}$ guarantees that it will be located on the time axis within the address signals (figure 2), since the low-order bit of the address is driven by counterbit "3", while bit "2" drives the READ/WRITE input of the LSI being tested. It is essential for the MARSH test that the READ/WRITE phase be suppressed in the READ/WRITE sequence. Counter bit output "2" has phase of 0-1. Therefore, when the READ command of the memory being tested has an active-low level (with the WRITE instruction having active-high level), the output "2" is connected directly to the $\overline{READ}$/WRITE of the device being tested. When the READ instruction has an active-high level (and the WRITE instruction an active-low level), counter bit "2" is connected to the $\overline{READ}$/WRITE INPUT through an inverting gate.

The address inputs of the tested device are driven by sequential bits of the generator, starting with bit "3" with n-address inputs and ending with bit 3 + (n - 1). The last bit of the 3 + n-counter which is used stimulates the data input, so that a zero will be written during the first half of the text after ones have been read from all of the addresses, and in the second half of the text a one will be written after zeros have been read from all of the addresses. Since the mechanical connection of the case to the driving circuit is not synchronized with the generator, the first driving cycle is not a test; the test begins with the second measurement window, which is irrelevant, since the testing cycle length is small. As figure 1 indicates, n + 3 is the last counter bit used. This means that the total number of test cycles is 2^{n+4}. Consequently, the number of cycles for an LSI memory with capacity of e.g., 4K (N = 4K, n = 12) is 2^{12+4} = 2^{16} = 65K. If the time required to test the LSI device (delay between $\overline{RV}$ signal and output of signal) is τ (ns), the acceptable minimum timing signal length, whose leading edge triggers the generator and whose trailing edge poles the output of the tested LSI memory, must be somewhat greater than that quantity. Allowing for the speed of the generator (approximately 130 ns) and signature analyzer (approximately 110 ns), the duration of the sync pulse is not less than $240 + \tau_{sel}$, and the period is $2(240 + \tau_{sel})$. Hence, the driving frequency does not exceed $10^6/2\ (240 + \tau_{sel})$. For τ_{sel} = 500 ns, this quantity is 0.6 MHz, and the time required for one test cycle of a 4K LSI memory is $65K\times2(240 + \tau_{sel})$ = $65K\times2(240 + 500) \simeq$ 1 second.

Table 1 presents data on the number of cycles and the cycle time for a series of LSI memory devices during testing using the present method, as well as data for R-bit LSI memories with N addresses and K bits (with 2^{n+k+3} cycles in this case, where $n = \log_2 N$). The signatures for some chips have been calculated theoretically and verified experimentally.

The principle used to test multibit LSI memories using this method is fully analogous to the testing principles explained above for single-bit LSI, with the added factor that the K data inputs of the tested LSI are obviously not driven by the last (n + 3) bit of the generator, but rather by a group of bits (cf. figure 1c): 3 + n, 3 + n + 1, ..., 3 + n + (k - 1) = n + k + 2; therefore, the total number of cycles in a complete testing program will be 2^{n+k+3}, and the start/stop input of the signature analyzer is controlled by the last bit used (n + k + 3). Obviously, the output response will have some redundancy, which is not of any particular significance using the signature method. As table 1 indicates, the testing times are short, not exceeding fractions of a second.

One important matter is the analysis of the formation of the binary output vectors during testing, keeping in mind that the state of the outputs, i.e., the components of the output binary vector, are recorded by the signature analyzer at the cutoff of each sync pulse, so that testing is ensured in all states of the truth table of the LSI being tested. The current address duration, as determined by driver counter bit "3", is equal to half the switching period ($1/2x2^4$), i.e., eight cycles. Therefore, for single-bit LSI it is sufficient to examine the formation of the output binary vector for eight current address cycles during the first half of the test, when $D_{in} = 0$, and in the second half of the test when $D_{in} = 1$. The summary output vectors are easily obtained by multiplying the eight-cycle group vectors by the number of groups, which is N/8. Since the truth tables are different for different types of LSI, it is useful to examine the question of the formation of binary output vectors using specific examples, for which we have selected K564RU2 (256x1 bit) single-bit LSI and K155RU2 (16x4) multibit LSI. Let us consider the example of the formation of the binary output vector for a K564RU2 LSI for which n = 8, k = 1 (the second output is inverse). The measurement window is 2^{12} = 4096 cycles. The time diagrams are shown in figures 3 and 4. The possible states of the outputs of this circuit are shown in table 2, the data in which provide the basis for table 3, which records the states of the output in the eight-cycle programs during the first (during the first 2048 cycles in the case in question) and in the second half of the interval (during the second 2048 cycles in the case in question), for the READ and WRITE mode; table 4 presents the analogous information for the READ - CHANGE - WRITE mode.

Table 1

Type of LSI	Capacity bits	N	h	n	τ_{sel} nsec	2^{n+k+3} test cycles	Time required for test cycle 2^{n+k+3} τ_{cycle} msec	Cycle length µsec/ stimulus frequency MHz	Signature
К155РУ2	64	16	4	4	60	2048	1,2	0,6/1,66	QO*H*5
К185РУ2	64	64	1	6	70	1024	0,7	0,62/1,6	
К155РУ5	256	256	1	8	70	4096	2,8	0,62/1,6	*CE*46
(К) 185РУ4	256	256	1	8	200	4096	3,6	0,88/1,1	
185РУ5	1К	1К	1	10	250	16К	16	1,0/1,0	
134РУ6	1К	1К	1	10	500	16К	24	1,5/0,7	1586
К541РУ1	4К	4К	1	12	180	65К	55	0,9/1,15	
К541РУ2	4К	1К	4	10	200	130К	120	0,88/1,1	
К500РУ145	64	16	4	4	10	2048	1	0,4/2	
К500РУ148	64	64	1	6	15	1024	0,5	0,5/2	
К500РУ410 413	256	256	1	8	40	2048	1,1	0,56/1,7	
К500415	1К	1К	1	10	30	16К	8,8	0,54/1,85	
К564РУ2	256	256	1	8	450	2048	2,8	1,4/0,7	*CH5F*
К537РУ1	1К	1К	1	10	800	16К	32	2,1/0,45	*UHC7*
505РУ6	1К	1К	1	10	650	16К	30	1,8/0,6	
К565РУ2	1К	1К	1	10	450	16К	23	1,4/0,7	82*CC*
К527РУ3	1К	1К	1	10	650	16К	320	2,1/0,45	82*CC*
К552РУ1	16К	16К	1	14	450	260К	370	1,4/0,7	
К507РУ1А	1К	1К	1	10	600	16К	27	1,7/0,6	
К565РУ1	4К	4К	1	12	200	65К	60	0,88/1,1	
К565РУ3	16К	16К	1	14	200	260К	230	0,88/1,1	*A*190
К565РУ(5)	64К	64К	1	16	200	1М	1000	0,88/1,1	*SE*53

$\tau_{cycle} = 2(130+110+\tau_{sel}) = 2(240+\tau_{sel})$

$f_{stim} = 1/\tau_{cycle}$

Table 2

$\overline{\text{READ}}$/WRITE	$\overline{\text{RV}}$	Mode	outputs Output	$\overline{\text{Output}}$
0	0	Read	Data	$\overline{\text{Data}}$
0	1	Inhibit Read	1(Z)	1(Z)
1	0	Write	1(Z)	1(Z)
1	1	Inhibit Write	1(Z)	1(Z)

The corresponding binary output vectors from the outputs of a K565RU2 LSI are as follows: for the READ and WRITE mode -- out. (13): $2048_1 + 2048\ (2_1 + 1_0 + 5_1)$, $\overline{\text{out}}$. (14): $2048\ (2_1 + 1_0 + 5_1) + 2048_1$; the signatures of these vectors are CH83 and H73U, respectively. The overall binary output vector is formed by arranging these vectors sequentially, and equals $2048_1 + 4096\ (2_1 + 1_0 + 5_1) + 2048_1$; its signature is CH5F.

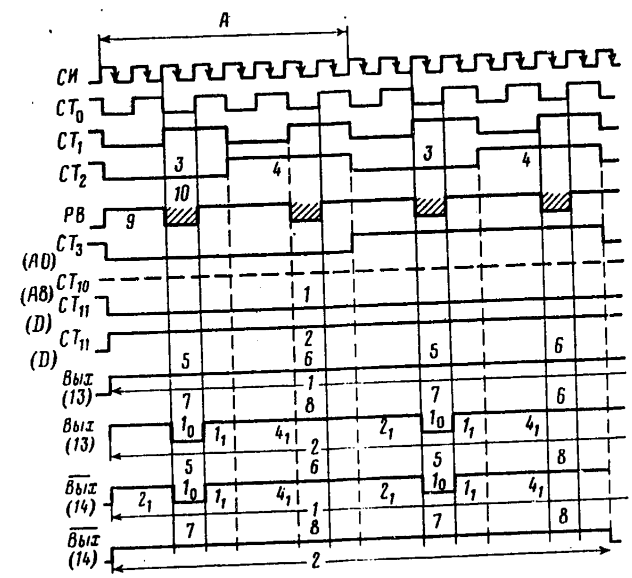

Figure 3. Time diagrams of input/output signals for functional testing of K564RU2 and K561RU2 memories in READ and WRITE mode using MARSH test; A -- eight cycles (current address); 1--first 2048 cycles; 2--second 2048 cycles; 3--read; 4--write; 5--read "1"; 6--write "0"; 7--read "0"; 8--write "1"; 9--inhibit; 10--enable

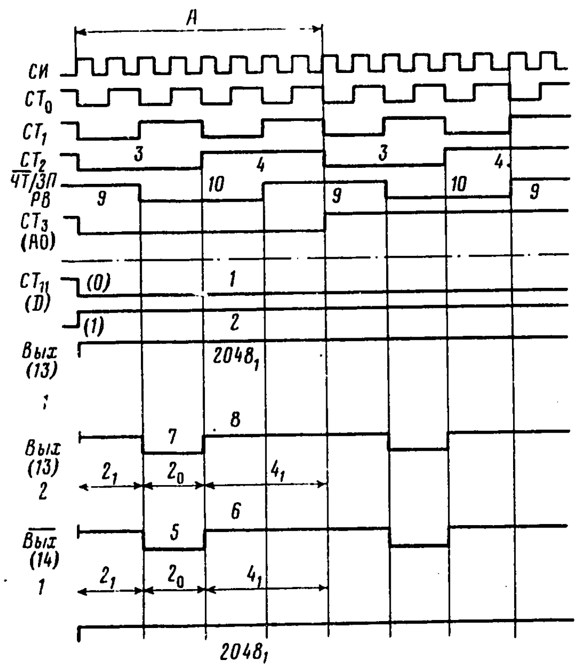

Figure 4. Time diagrams of input/output signals in functional testing of 564RU2, 561RU2 memory circuits in READ - CHANGE - WRITE mode using MARSH test (designations as in figure 3)

Table 3

Operation	Read				Write				Binary output vector
Cycle No.	1	2	3	4	5	6	7	8	
Mode	Inhibit		Read	Inhibit	Read		Write	Inhibit	
Out	1		Data		1		1	1	
($\overline{out}$)	(1)		Data	(1)	(1)		(1)	(1)	
Read 1/ write 0	1 (1)	1 (1)	1 (0)	1 1	1 1	1 1	1 1	1 1	8_1 $2_1+1_0+5_1$
Read 0/ Write 1	1 1	1 1	0 1	1 1	1 1	1 1	1 1	1 1	$2_1+1_0+5_1$ 8_1

Table 4

Operation	Read				Write				Binary output vector
Cycle No.	1	2	3	4	5	6	7	8	
Mode	Inhibit		Read		Write		Inhibit		
Out	1	1	Read Data		1	1	1	1	
($\overline{out}$)	1	1	Data		1	1	1	1	
Read 1/ Write 0	1 (1)	1 (1)	1 (0)	1 (0)	1 (1)	1 (1)	1 (1)	1 (1)	8_1 $2_1+2_0+4_1$
Read 0/ Write 1	1 (1)	1 (1)	0 (1)	0 (1)	1 (1)	1 (1)	1 (1)	1 (1)	$2_1+2_0+4_1$ 8_1

Formation of the binary output vectors for a multi-bit LSI memory is examined for the READ and WRITE mode using the example of a K155RU2 microcircuit ($N = 16$, $n = 4$, $k = 4$) with a $2^{3+4+4} = 2^{11} = 2048$ window connected in accordance with figure 1c and having the truth table in table 5.

The data in table 5 provide the basis for table 6, which contains the states of the outputs in the eight-event cycles in the first half (during the first 1024 cycles) and in the second half (the second 1024 cycles) of the interval for the READ and WRITE mode. The time diagram corresponding to this mode is shown in figure 5.

There is some redundancy in formation of the binary output vectors, since the switching periods of the four bits of the counter which drive the data inputs of the LSI memory are not multiples of powers of 2. Therefore, the read 1/write 0 test for the high-order bit D_3 occurs during the first 128 cycles of an exhaustive sampling of 16 addresses, with 8 cycles each. Since there is no input to D_3 during the remaining 896 of the 1024 cycles (the output of bit 10 remains 0), the zeros written in the first 128 cycles will be read, and zeros will be written to all of the addresses. As can be seen from table 6 and the explanatory time diagrams of the stimulation of input of the various bits of the K155RU2 LSI and the distribution of the modes READ 1/WRITE 0, READ 0/WRITE 1, READ 0/WRITE 0, READ 1/WRITE 1 (figure 6), the binary output vector of output D_3 during the first half of the interval will be $16\,(2_1 + 1_0 + 5_1) + 896_1$. For the second half of the interval, the READ 0/WRITE 1 test will occur during the first 16 cycles, while the READ 1/WRITE 0 test will occur during the remaining 896 cycles. The corresponding vector is (cf. table 6) $16(4_1 + 4_0) + 112(2_1 + 1_0 + 1_1 + 4_0)$. The input of bit D_2 is switched half as often as the input of bit D_3; therefore, during the first 128 cycles the READ 1/WRITE 0 test mode will occur, and the READ 0/WRITE 0 mode will occur in the following 384 cycles, after which the value at the input will be 1, which corresponds to the READ 0/WRITE 1 mode. The first half of the interval is repeated during the second 1024 cycles of the interval.

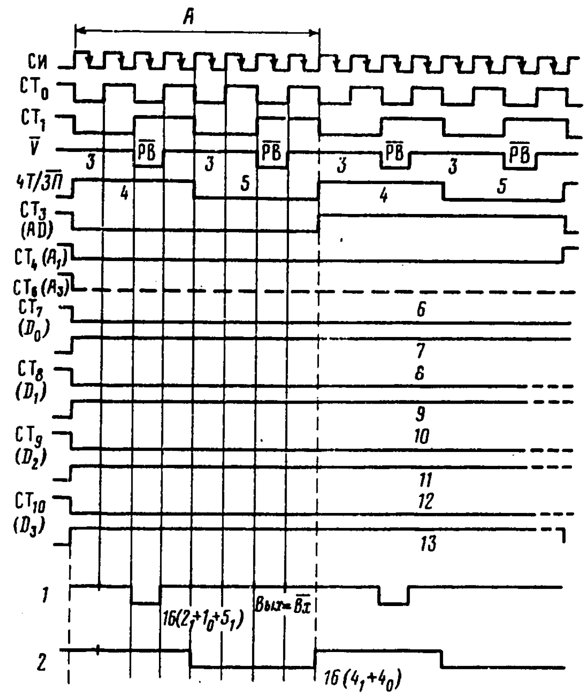

Figure 5. Time diagrams of functional testing of K155RU2 memory circuit in READ and WRITE mode using MARSH test: A -- eight cycles (current address), 1--output "0", first 128 cycles; 2--output "0", second 128 cycles; 3--inhibit; 4--read; 5--write; 6--first, and all odd, 128 cycles; 7--second, and all even, 128 cycles; 8--first, and all odd, 256 cycles; 9--second, and all even, 256 cycles; 10--first and third 512 cycles; 11--second and fourth 512 cycles; 12--first 1024 cycles; 13--second 1024 cycles

The READ 1/WRITE 0, READ 0/WRITE 1, READ 1/WRITE 1 cycles will be repeated four times for bit D_1 (table 6 and figure 6), and the cycle READ 1/WRITE 0, READ 0/WRITE 1 will be repeated eight times for bit D_0. The binary output vectors (and their signatures) of the output of a K155RU2 LSI memory, formed according to table 6 and figure 6, appear as:

Output D_0: $8(16(2_1+1_0+5_1)+16(4_1+4_0))$ (signature 009A)

Output D_1: $4(16(2_1+1_0+5_1)+128_1+16(4_1+4_0)+$
$+16(2_1+1_0+1_1+4_0))$ (signature 6C3U)

Output D_2: $2(16(2_1+1_0+5_1)+384_1+16(4_1+4_0)+$
$+48(2_1+1_0+1_1+4_0))$ (signature 1096)

Output D_3: $16(2_1+1_0+5_1)+896_1+16(4_1+4_0)+$
$+112(2_1+1_0+1_1+4_0))$ (signature 9UP5)

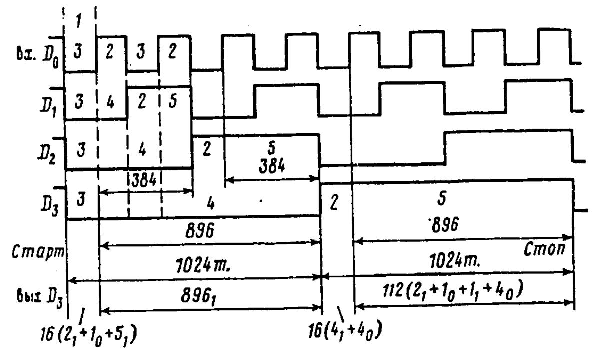

Figure 6. Time diagrams of stimulation of inputs of various bits of K155RU2 memory circuits and distribution of modes read 1/write 0, read 0/write 1, read 0/write 0, read 1/write 1: 1--16 addresses -- 1028 cycles; 2--read 0/write 1; 3--read 1/write 0; 4--read 0/write 0; 5--read 1/write 1

Table 5

$\overline{RV}$	READ/$\overline{WRITE}$	Mode	Output
0	0	Write	$\overline{D}_{in}$
0	1	Read	Data
1	0	Inhibit	D_{in}
1	1	No operation	1

Table 6

Operation	Read				Write				Binary output vector
Cycle No.	1	2	3	4	5	6	7	8	
Mode	Inhibit		Read	Inhibit	Inhibit		Write	Inhibit	
Output	1	1	Data	1	$\overline{D}_{in}$		$\overline{D}_{in}$	$\overline{D}_{in}$	
Read 1/Write 0	1	1	0	1	1	1	1	1	$2_1+1_0+5_1$
Read 0/Write 1	1	1	1	1	0	0	0	0	4_1+4_0
Read 0/Write 0	1	1	1	1	1	1	1	1	8_1
Read 1/Write 1	1	1	0	1	0	0	0	0	$2_1+1_0+1_0+4_0$

When the overall signature of the chip is recorded by multiplexing the output vectors, its overall output vector is analogous to a series of these vectors arranged one after the other, and the overall signature of the chip for an interval of 2048x4 = 8192 is 00H5.

This functional testing method for LSI memories using the "data shift against inverted background" (MARSH test) is general, and can be implemented using simple equipment, allowing bulk users to use it for acceptance testing of LSI memory devices. It can also be used as the basis for more complex LSI memory tests.

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UDC: 681.325.3

HIGH-SPEED MICROPOWER ANALOG-DITIGAL CONVERTER

Moscow PRIBORY I TEKHNIKA EKSPERIMENTA in Russian No 1, Jan-Feb 82 (manuscript submitted 27 Feb 80) pp 117-119

[Article by Ye. A. Kolombet and B. K. Fedorov]

[Text] This article describes the 10-bit bit-weighting analog-digital converter with throughput capacity of 1 mbps (10 bits per 10 μsec); input voltage range 0-10 V, power consumption <100 mW.

Bit-weighting analog-digital converters generally have a complicated control circuit, require many high-precision elements and adjustment circuits and consume a lot of power (3-5 W), and are consequently not usable in autonomous systems with limited power supply output. Thanks to the use of modern MOS LSI and new circuit treatments, it has been possible to reduce power consumption in the bit-weighting analog-digital converter we have developed to 100 mW, while retaining sufficiently high speed.

The slowest section of the bit-weighting analog-digital converter (figure 1) is the digital-analog converter which generates the feedback signal. The output signal of most modern digital-analog converters is a current signal. In order to increase the speed of converters using such digital-analog converters it is necessary to arrange current feedback in bit-weighting analog-digital converters, i.e., to add together at the input of the voltage comparator the current equivalent I_{in} of the input voltage and the output current I_d (feedback current) of the digital-analog converter. Current I_d is added to the output current of the input analog signal sample-and-hold device.

The output voltage from the sample-and-hold device is converted to current I_{in} by internal resistor R_{os} in the digital-analog converter used. The minimum rise time of the current I_d in each cycle can be obtained with a minimal (10-100 ohms) equivalent load impedance R_ℓ of the digital-analog converter, while the required N-bit resolution in the bit-weighting analog-digital converter can only be obtained as long as $R_\ell \geq U_p 2^{N+1}/I_e \geq 2.5 \geq K\Omega$ (with $N \geq 8$, standard digital-analog current $I_e \approx 1$ mA and the usual ambiguous zone for modern comparators of $U_p = \pm 5$ mV). The impedance R_ℓ must thus have a nonlinear volt-ampere characteristic:

$$U_\Sigma = U_p \text{ for } I_r \geq I_e/2^{N+1} \text{ (i.e., } R_\ell = 0);$$
$$|U_\Sigma| < U_p \text{ for } -I_e/2^{N+1} \leq I_r < I_e/2^{N+1}$$
$$\text{(i.e. } R_\ell > U_p 2^{N+1}/I_e);$$
$$U_\Sigma = -U_p \text{ for } I_r < -I_e/2^{N+1} \text{ (i.e. } R_\ell = 0).$$

Here U_Σ is the voltage fluctuation at the point at which I_{in} and I_d are added, and $I_p = I_{in} - I_d$. This is achieved in this analog-digital converter by using a new active voltage limiter structure.

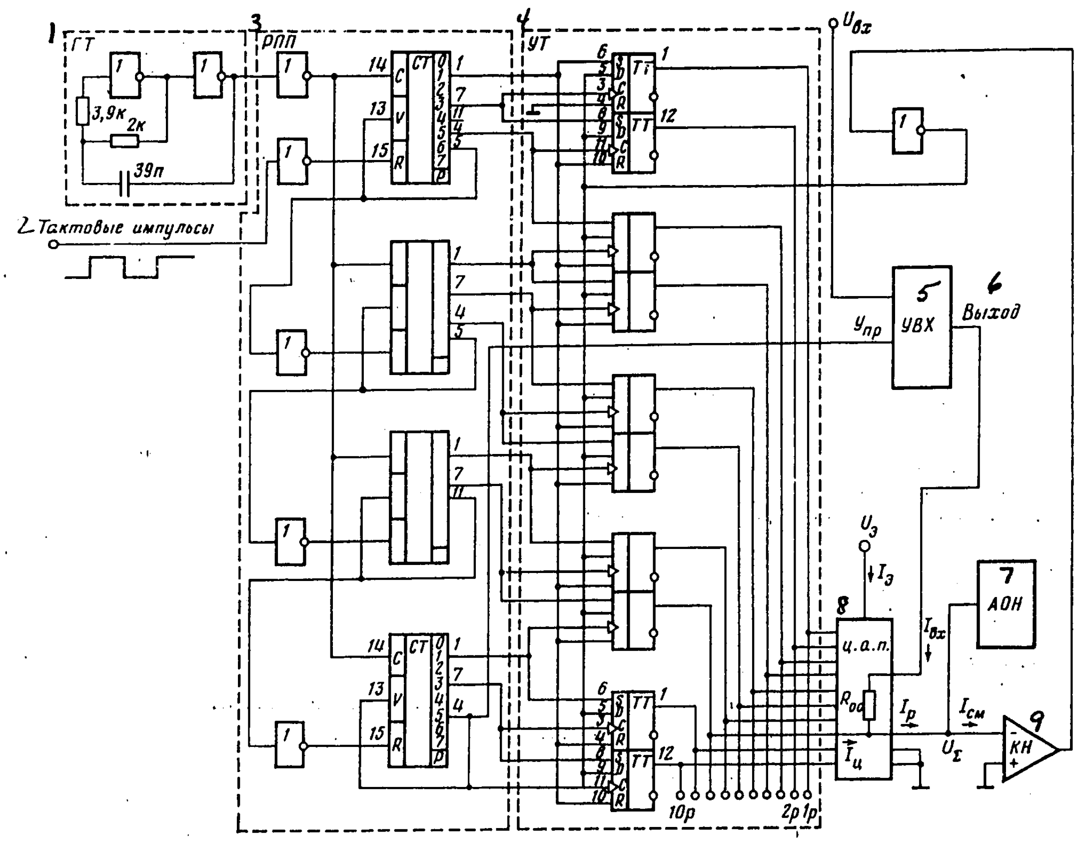

Figure 1. Functional diagram of bit-weighting analog-digital converter. Counters - 564IYe9, flip-flops - 564TM2, inverters - 564LN2, digital-analog converter - 572PA1A, voltage comparator - 521SA3, 1, timing generator; 2, timing pulses; 3, sequential approximation register; 4, control flip-flops; 5, sample-and-hold circuit; 6, output; 7, active voltage limiter; 8, digital-analog converter; 9, voltage comparator.

The structure of this digital device (figure 1), which contains a sequential approximation register, automatically triggered variable timing generator and control flip-flops, is sufficiently understandable. We point out only that complete conversion to an N-bit word requires 2 N cycles of the timing generator, which results from an operating pecularity of the 564IYe9 LSI (the output pulses of these LSI may overlap in time; therefore, only half of their outputs are used in order to avoid incorrect operation).

Let us examine the active voltage limiter and sample-and-hold devices (figures 2 and 3), which to a great extent determine the parameters of the entire device, in more detail. The maximum delay introduced by the digital-analog converter in the present arrangement is obtained when $I_p=I_e/2^N$, and amounts to $t_{dd}\approx U_\Sigma 2^N C_\Sigma / I_e$, where N is the resolution of the analog-digital converter; U_Σ is the voltage amplitude at the point at which I_{in} and I_d are added; I_e is the standard current of the digital-analog converter; C_Σ is the parasitic capacitance operating at the summation point. As this expression shows, the only possible way to reduce the delay t_{dd} is to limit $U_{\Sigma max}$ at its minimum level with a maximum difference current I_p. In addition, when the current $I_p=I_e 2^{-N}$ is minimum it is necessary to satisfy the condition $U_{\Sigma min}<2^{-(N+1)}IR_\ell$, in order to obtain a conversion error of half the least-significant bit. The required mode current $I_1>I_e/4$ and the values of the resistors needed to ensure the required $U_{\Sigma max}$ and $U_{\Sigma min}$ are calculated for this active voltage limiter by the following expressions:

$$U_{\Sigma max}=\phi_T \ln[4(I_1-I_e/4)/I_e]-(I_1-I_e/4)R_1<U_{\Sigma g};$$
$$U_{\Sigma min}=\phi_T \ln(I_1 2^{N+1}/I_e)-I_1R_1 \geqslant U_{pmin},$$

where U_{pmin} is the minimum threshold voltage of the voltage comparator; $U_{\Sigma g}$ is the maximum acceptable voltage at the output of the digital-analog converter.

Bit-weighting analog-digital converters are known to be characterized by methodical error equal to half the least significant bit due to the fact that the ideal gain of the analog-digital converter and digital-analog converter do not match. In order to eliminate this error, an additional direct current is applied through resistor R_k (figure 2) to the summation point:

$$I_k=\frac{U_{eb}}{R_k}=\frac{I_e}{2^{N+1}}+I_{sm},$$

where I_{sm} is the input current of the voltage comparator.

In contrast to other sample-and-hold devices, the present one (figure 3) consumes current from the power supply only during the sampling time (≈500 nsec). In the hold mode T_{1-4} is closed, there is no current in the differential stage and while the bit-weighting analog-digital converter is operating (≈10 μsec), direct current $U_{in}R_{os}$ is consumed from the power supply. It is not difficult to determine that the sample-and-hold device consumes maximum power only when $U_{in}=E^+_p/2$, and amounts to $P=(E^+_p)^2/4R_{os}$. The innovation in this circuit is the use of transistor T_{2-3}, which compensates for the charge current of memory capacitor C_3 with the base

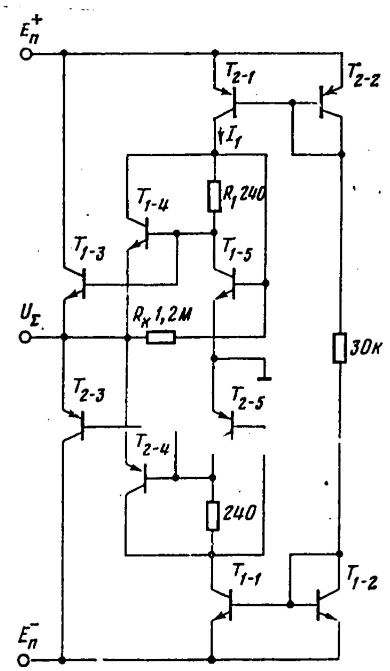

Figure 2. Schematic diagram of voltage level limiter. T_1=198NT1, T_2=198NT5.

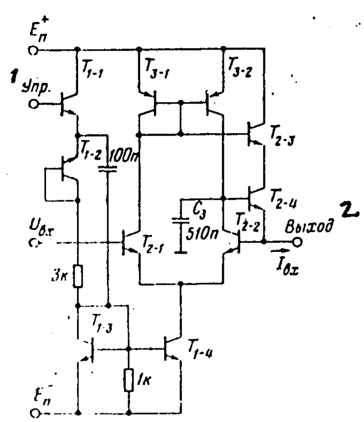

Figure 3. Sample-and-hold device. T_1, T_2 - 198NT1, T_3 - 198NT5, 1, control; 2, output.

current from T_{2-3}. If the base current gain β of transistors T_{2-3} and T_{2-4} is approximately the same, the charge current of memory capacitor C_3 in the hold mode is negligibly small, which made it possible to eliminate the buffer amplifier from the sample-and-hold device and to charge C_3 within 10 μsec using no more than 5 mV.

Tests of the analog-digital converter in the ±50°C temperature range indicated that the conversion time, to within 10 bits, is 10-15 μsec with error equal to half the least significant bit and power consumption of 80-90 mW.

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POWER ENGINEERING

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IMPROVING FUEL UTILIZATION AT NUCLEAR POWERPLANTS USING VVER-440 REACTORS

Moscow ELEKTRICHESKIYE STANTSII in Russian No 12, Dec 81 pp 8-9

[Article by A. A. Matveyev, Yu. I. Savchuk and Ye. I. Ignatenko, engineers, Kola AES]

[Text] Of the many directions in which work is being done to increase the economic efficiency of nuclear powerplants at present, the attempt to increase the extent of nuclear fuel depletion should be emphasized. The reloading of nuclear fuel (replacing spent fuel with fresh) occupies a special place in the organization of an optimal fuel utilization mode. The best alternative, which yields the greatest benefits, is continuous refreshing of fuel-rod assemblies which have reached their design depletion level. Due to singularities of construction [1], the design of the VVER-440 has provisions for 3 partial re-loads during the reactor life-cycle. The reactor operates for approximately a year between reloading.

The average depletion of the unloaded fuel depends upon the number of fuel elements to be unloaded, and increases as the amount decreases (assuming that the elements which have been depleted to the greatest degree are removed from the reactor first).

It is noted in [1] that the present mode of three partial reloadings with a fuel cycle lasting a year makes it possible to achieve a design fuel depletion level of 28,000 MW·day/tU. The fuel depletion in VVER-440 reactors can be increased further if the fuel is reloaded more frequently (than 3 times per run). Then the number of reloaded fuel assemblies must be kept the same during each subsequent recharging of the reactor. In this case, stoppage of the reactor for reloading will not always coincide with the summer lull in power consumption. It is economically profitable to implement this mode when the re-loading downtime does not exceed 7 days. The actual amount of time required for reloading at existing nuclear plants using VVER-440 reactors is significantly longer than this due to the fact that scheduled and preventive maintenance is done at the same time. This makes it impossible to implement the mode in which increased numbers of partial reloadings are used. It becomes possible to arrange a reloading mode with a reduced number of fuel magazines if the reactor is fueled with U234-enriched fuel.

The specific nature of the active-zone formation in the VVER-440 reactor by the fuel magazines requires that the fuel loading be kept symmetrical. The number of working fuel magazines to be replaced with fresh ones must be a multiple of 12, 6 or 3. The number of working supply magazines which is closest to the design number of 102, which we shall use as the initial quantity. Reducing this number by 12 each time, we obtain the following series of values for the number of magazines to be reloaded: 90, 78, 66, 54, etc., such that fuel loading symmetry is maintained.

It must be noted that as the number of fuel magazines decreases, the amount of time each spends in the active zone of the reactor increases. For example, when a reactor is fed with 90 magazines, the length of stay of 46.7% of the fuel magazines in the active zone increases to 4 years; if the number of fuel magazines is reduced to 78, all of the fuel will have a 4-year run time.

The experience of the Kola Nuclear Powerplant, where most of the fuel assemblies can be operated successfully for 4 years, shows that this increase in the operating life of nuclear fuel is fully attainable.

The neutron-physical characteristics of the stationary fuel cycles of the VVER-220 reactor have been obtained (analytically) in order to substantiate the choice of required fuel enrichment when a smaller number of fuel magazines is used [2, 3]. The initial fuel load used is the typical load of a series-produced VVER-440 reactor. The reactor enters the stationary fuel mode only after the ninth reloading. The table shows the length of the fuel cycle as a function of the number and enrichment level of reloaded fuel assemblies when the reactor enters the stationary load.

Figure 1 [not reproduced] shows the length of the stationary fuel cycle of the VVER-440 reactor as a function of the enrichment of the fuel for a fixed number of reloaded fuel magazines. The duration of the stationary fuel cycle with the reactor loaded with 102 working magazines with enrichment of 3.6% comprised 326 effective days. It follows from this that when the reactor charge is reduced to 90 magazines and the same fuel cycle length is realized, the required enrichment of nuclear fuel amounts to 3.9%, and when 78 magazines are used their enrichment should be increased to 4.3%.

The average fuel depletion for the unloaded fuel is increased in the first case to 38,300 MW·day/t the first case, and to 40,300 MW·day/t in the second (figure 2) [not reproduced].

The use of enriched fuel in VVER-440 reactors makes it possible to improve the technical and economic indicators of a nuclear powerplant. Although the cost of the fuel assemblies in these cases increases in proportion to the enrichment, the total cost of the fuel, i.e., the costs over the fuel cycle of the reactor, is reduced. The economic indicators of nuclear powerplants which are changed by charging a VVER-440 reactor with a smaller number of enriched fuel magazines are presented below.

Number of fuel magazines	102	90	78
U235 enrichment of fuel magazines, %	3.6	3.9	4.3
Reduction, %, of land electricity prime cost:	-	1.7	3.1
of its fuel component	-	4.5	7.9
variable portion of fuel component	-	4.7	8.4

Conclusions

1. One way to increase the depletion of nuclear fuel at nuclear powerplants using VVER-440 reactors is to feed the reactor with enriched fuel and simultaneously reduce the number of reloaded magazines.

2. Feeding the reactor with enriched fuel makes it possible to extend the operating cycle of the VVER-440 reactor to 4 years, with a separate fuel cycle length of one year.

3. The implementation of a 4-year run for the VVER-440 reactor makes it possible to reduce the fuel component of the prime cost of electricity by 7.9%, and to reduce the prime cost of electricity produced at the powerplant by 3.1%.

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CSO: 1860/227

UDC: [621.311.25:621.039]:621.182.448-57.004.13

ON ARTICLE BY V. M. SEDOV, P. G. KRUTIKOV AND S. T. ZOLOTUKHIN: 'CHEMICAL-TECHNOLOGICAL MODES DURING START-UP AND INITIAL OPERATING PERIOD OF AES USING RBMK REACTOR'[1]

Moscow ELEKTRICHESKIYE STANTSII in Russian No 12, Dec 81 pp 9-10

[Article by G. D. Volgin, candidate of chemical sciences, Leningrad AES]

[Text] It follows from the essence of the material presented in the title article that the author is talking about post-installation flushing of the internal surfaces of the condensate-feed section of a nuclear powerplant using an RBMK reactor. In addition, in both the title and the article itself, post-repair pre-startup flushings of the condensate-feed circuit are treated as chemical-technological modes during the startup period, which obviously is not the same thing.

The post-installation flushing of the inside surfaces of the condensate-feed circuit of Units No. 1 and 2 at the Leningrad Nuclear Powerplant imeni V. I. Lenin was done with ammonia monocitrate during chemical flushing and sodium citrate during passivization.

In developing the technology for post-installation flushings of the condensate-feed circuit of Unit No. 3 at the Leningrad Nuclear Powerplant, we studied the experience of the Kursk Nuclear Powerplant in flushing the condensate-feed circuit of Unit No. 2 using water with hydrogen peroxide, considering the results with respect to maintaining the water-chemical mode during subsequent operation of the power unit. As we know, the performance norms for the coolant in Unit No. 2 at the Kursk Plant were achieved earlier than after chemical flushing; no further difficulties in operation of the turbine condensate cleaning installation occurred. Since the amount of hydrogen peroxide actually expended was only 1.5-3 milligrams per square meter of surface area , it was possible to assume that there was no influence of the hydrogen peroxide additives on the results obtained.

Instead of chemical flushing, the inside surfaces of the condensate-feed circuit in power Unit No. 3 at the Leningrad Plant was flushed after installation with non-reagent water. The quality standard for feed water in terms of iron content was achieved in power Unit No. 3 after 40-50 hours of operation at power; the iron-content norms were, for practical purposes, not exceeded in the forced recirculation

1ELEKTRICHESKIYE STANTSII, No. 2, 1981.

circuit during startup and when operating at power. The condensate-feed circuit in power Unit No. 4 was also flushed with with non-reagent technology. The iron content in the water in the forced recirculation circuit met the established norm during startup, gaining power and operating at power; the iron content in the feed water reached the normal value after 50 hours of operation at power. As power Units No. 3 and 4 continued to operate, no significant increase was observed in the coolant iron concentration after stops and starts, while the concentration of iron in the feed water dropped to below 10 micrograms per liter within a few hours after each startup.

A significant positive effect is also achieved with non-reagent water washdown of condensate-feed circuits because this technology is implemented using stock equipment and without a time break between flushing the condensate-feed circuit and starting up the power unit.

We consider the improvement in operating conditions of devices for maintaining the water-chemical mode during startup, savings in supply material (citric acid) and savings in the construction of neutralizer baths to be important facts arguing on behalf of non-reagent water flushing technology for condensate-feed circuits, which consist of the following basic stages:

-post-installation water (cold) flushing of the condensate-feed circuit, discarding the water;

-post-repair water (hot, 70-80°C) closed-circuit flushing.

The article noted correctly that chemical cleaning and passivization using sodium nitrite or ammonia have been borrowed from thermal power engineering for nuclear powerplants using RBMK reactors. The results of starting up recent power units using RBMK-1000 reactors indicate that this should not have been done.

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QUANTUM ELECTRONICS, ELECTRO-OPTICS

OPTOELECTRONICS IN PROCESSING MOTION PICTURE FILM

Moscow OPTOELEKTRONIKA PRI OBRABOTKE KINOFOTOMATERIALOV in Russian 1980 (signed to press 11 Jul 80) pp 2, 189-191

[Foreword, table of contents and annotation from book "Optoelectronics in Processing Motion Picture Film", by Iosif Solomonovich Barbanel', Izdatel'stvo "Iskusstvo", 6000 copies, 191 pages]

[Text] Author's Foreword

The present monograph is devoted to questions of testing and evaluating the polymer base and emulsions of motion picture films and magnetic tapes using coherent and holographic equipment. These problems are solved on two theoretical planes:
1. Determination of requirements for optimal processing of holograms recorded on thin-film carriers allowing for the characteristics of the recording media (photographic materials, thermoplastic material, photothermoplastic materials, etc.).
2. Synthesis of special optoelectronic processing devices used to analyze recording media including photographic emulsions, magnetic tape coatings and film bases, and to analyze the "transfer" characteristics of recording media (characteristic curve, phase relief of medium as function of exposure for phase media, etc.).

All of these devices are divided formally into three basic subclasses: refractometers, photometric devices and microcomposition analyzers; the book is structured to reflect this.

All of the devices considered use holograms to some extent as the basic elements, or holographic methods of basic functioning principles; this made it necessary to include a chapter on optimal processing of actual holograms.

The author is grateful for the work done on the manuscript by Doctor of Technical Sciences E.I. Kripitskiy, by Z.M. Krasnovskiy and A.M. Bekker and, for their assistance in experimental research, to Candidate of Technical Science V.V. Kulikov, and M.B. Ioffe, A.Yu. Shanin and Yu.I. Vdovin.

Table of Contents

Annotation

This monograph is devoted to questions of the application of optoelectronic devices for analyzing and evaluating motion picture films and magnetic tapes using the methods of coherent technology and holography. The principles of holography and

directions in optoelectronics associated with motion picture photography and television are examined. The book describes instruments for physical-chemical analysis which are designed for motion picture films, emulsions and coatings, as well as still, motion-picture and magnetic film bases; also presented are methods and facilities for calculating the optimal modes of photochemical processing of holograms, which are the basic elements used in building these instruments. The book is intended for specialists in the area of motion picture technology, optoelectronics, coherent technology and holography.

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USE OF CHARGE-COUPLED DEVICES IN OPTICAL DATA PROCESSING SYSTEMS

Moscow PRIBORY I TEKHNIKA EKSPERIMENTA in Russian No 1, Jan-Feb 82
(manuscript received 10 Nov 80) pp 98-102

[Article by V. A. Arutyunov, N. A. Yesepkina, B. A. Kotov, Yu. A. Kotov, A. P. Lavrov and I. I. Sayenko, Leningrad Polytechnical Institute]

[Text] The example of an acoustooptical radio signal spectrum analyzer is used to demonstrate the possibility of using new solid state photodetectors based on charge-coupled devices in optical data processing systems. The article describes the construction and operating features of these photodetectors, the characteristics of the linear (unidimensional) CCD-photodetectors which we used which contain 50 32 x 1500 μm^2 light-sensitive elements, as well as the schematic diagram of their control device. The acousto-optical spectrum analyzer investigated had an analysis range of ΔF=40 MHz, frequency resolution ΔF_{min}=100 KHz and provided the capability of parallel spectral analysis of continuous and pulsed signals up to 1 μsec in length.

Optical systems provide high processing speed for large data files in real time. They make parallel analysis of several input signals possible, converting them to the spatial distribution of light intensity in the output focal plane of an optical system. Various photodetectors are used to translate this information to an electrical signal. The current most promising photodetectors are multi-element solid state photodetectors based on charge-coupled devices (CCD) [1]. These have a high quantum output, up to 80%, a wide dynamic range of 60-80 dB, and they use small light sensing elements (tens of micrometers and less) arranged with high geometric precision approaching 0.1 μm.

The present article describes a CCD photodetector and its use in an acoustooptical spectrum analyzer.

CCD photodetector. Multielement CCD photodetectors contain a group of photo-sensitive elements (charge accumulating section) and shift registers (charge transfer section). The photosensitive elements — photodiodes or photocapacitors-- convert light intensity to its proportional electrical charge. The shift registers act as a buffer memory and move the charge distribution obtained serially

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to the output unit. They make it possible to connect CCD to various external devices, including computers, thus making it possible to build hybrid optical-digital data processing systems [2].

The photosensitive elements and shift registers are constructed as an integrated structure based on a silicon chip. CCD photodetectors are produced with both separate [2] and combined charge accumulation and transfer sections [3]. The multielement CCD we used had combined charge accumulation and transfer sections, and consisted of a linear four-phase CCD shift register (figure 1, M_7). The use of transparent polysilicon electrodes made it possible to use this register simultaneously as both a photosensitive structure and a data output device. The elements in the register were spaced 32 μm apart. The light sensitive region of the register was 1.5 mm wide, which made it possible to integrate the light flux for one of the coordinates. The total number of elements in the register was 50. The spectral sensitivity region of the instruments used was 0.4-1 μm, with maximum sensitivity of λ=0.8 μm.

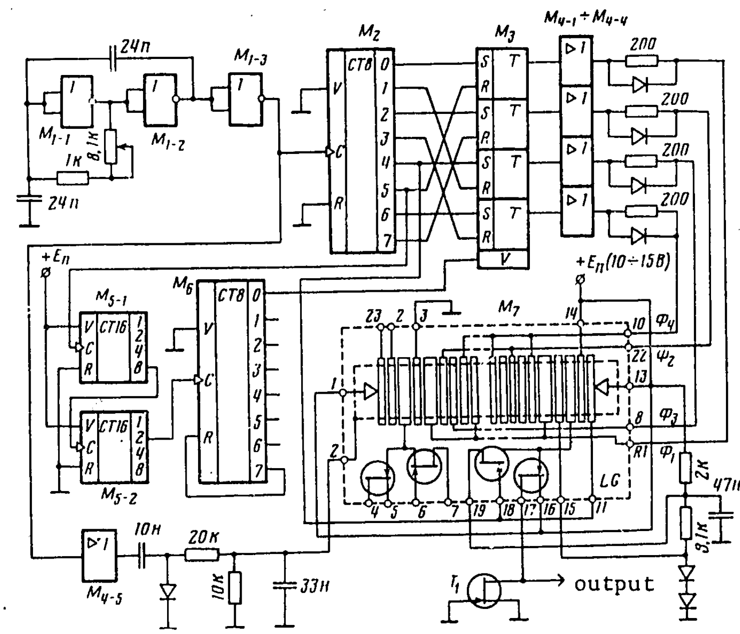

Figure 1. Schematic diagram of CCD photodetector and control devices. M_1 - 564LYe5, M_2, M_6 - 564IYe9, M_3 - 564TR2, M_4 - 564PU4, M_5 - 564IYe10, M_7 - CCD photodetector; T_1 - KP303V; diodes - KD102A.

There are output units at both ends of the CCD register which convert the charge distribution to a proportional output voltage. Data can be output to either output unit, depending upon the operating mode. When necessary, the charge signal can be input electrically to the shift register through one of the output units [1]. This makes it possible to add the electrical and optical data in the CCD photodetector itself, which expands its capabilities.

The charge accumulated in a CCD element is proportional to the illumination and accumulation time. The saturation exposure for the instrument we used was 0.1 lux — sec. The lowest recordable illumination level is determined by the maximum possible accumulation time, which is limited by dark currents. Their value depends upon the power supply conditions and the chip temperature. In the instruments in question the maximum accumulation time at room temperature is several seconds. Figure 2a shows an oscillogram of the output signal which characterizes the dark current level and distribution for the elements of the CCD photodetector at room temperature with a 10-second accumulation time. The saturation illumination for this accumulation time is 0.01 lux. After the dark current signal has been output from all 50 elements of the PZS strip, a pulse can be seen on the oscillogram from an electrical signal applied to one of the elements which corresponds to one-half the saturation signal.

One of the most important features of this CCD photodetector is the capability of processing charge distributions directly in the output unit, which consists of an electrometric stage with "floating" gate [4]. This expands the capabilities of systems using this type of photodetector. For example, the derivative (figure 2b), extremal value (figure 2c), as well as the signal proportional to the sum of the signals in the individual elements, i.e., the "integral" of the original distribution, can be observed at the same time as the signal proportional to the light flux intensity distribution. In addition to the derivative, figure 2b also shows its corresponding visual distribution obtained by projecting a spot of light on the register. The discrete points on the oscillograms correspond to the signals from the individual elements in the CCD strip.

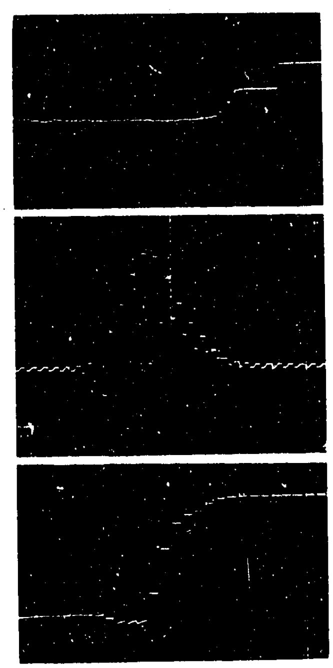

Figure 2. Oscillograms of CCD photodetector output signal: a - dark current distribution for elements after 10-second accumulation and electrical input pulse; b - signal proportional to element difference or derivative of initial distribution; c - signal proportional to extremal value. Vertical scale 1 V/div; number of signals from photodetector elements per division along the horizontal: a - 7.5; b, c - 3.

A controller whose schematic diagram is shown in Figure 1 was developed to control the photodetector. The controller assigns the periodic operating mode of the CCD and produces all of the required service control pulses. It uses series K564(561) integrated circuits. The microcircuits in these series have good power supply agreement with CCD without the use of additional convertors. The range of variation of the CCD control voltages is 0-20 V, while that of the microcircuit supply voltage is 5-16 V; in addition, these circuits consume extremely little power.

The operating period of the controller and CCD photodetector is made up of two intervals: the accumulation interval T_a and data output (read) interval T_o. During the read interval, pulses phase voltages Φ_1-Φ_4 must be applied to the CCD in order to move the charge distribution obtained during the accumulation interval to the output unit; pulses to control the output unit must be applied as well. During the accumulation interval, constant voltages are applied to the CCD instead of pulsed phase voltages, along with the aforementioned output unit control pulses. In connection with this CCD operating algorithm, the device which generates phased voltages Φ_1-Φ_4 and the output unit control pulses (Reset and Output pulses) is a variable 4-phase generator (M_1-M_3 in figure 1) [5]. The generator controls the device which forms the accumulation and read intervals, which consist of M_5 and M_6. Elements M_{4-1}-M_{4-4} are the buffer amplifiers for working into a capacitive load - the CCD register. The data output rate from the CCD in this controller is determined by the frequency of master oscillator M_1. The maximum output frequency is $6 \cdot 10^5$ elements per second, which corresponds to a signal output time from one element of 1.7 μsec. This frequency is limited by the speed of the microcircuits used, and can be raised to $2 \cdot 10^6$ elements per second by using elements with lower inertia.

The CCD output signal is a pulse train. The number of pulses in a sequence is the same as the number of CCD elements, or 50 in our case. In order to obtain the envelope it is necessary to use a "sample and hold" circuit. With control voltage amplitudes of 10 V, the maximum CCD output signal level does not exceed 3 V.

The controller uses a single +(10-15 V) power supply. The operating integrity of the CCD photodetector and controller is retained with supply voltage varying from +6 to +16 V. When E_p=10 V, the power consumption ≤30 mW. The controller is sufficiently simple and compact, and consists of a 100 x 100 mm^2 printed circuit board. Figure 3 shows the appearance of the board holding the control circuit and CCD photodetector.

Acoustooptical spectrum analyzer. The operation of the CCD photodetector in an optical data processing system was investigated on a breadboarded acousto-optical spectrum analyzer. Figure 4 shows the functional diagram of the analyzer, which was built on a standard optical bench. The radiation source was a He+Ne-laser with radiated power of 15 mW. The radio signals were input through an acoustooptical modulator with a fused quartz acoustic conductor operating in the Bragg diffraction mode. The center frequency of the modulator was F_0=130 MHz, with bandwidth of ΔF=40 MHz. The signal propagation time through the acoustic conductor τ_s=10 μsec, which corresponds to frequency resolution of $\Delta F_{min}=1/\tau_s$=100 KHz.

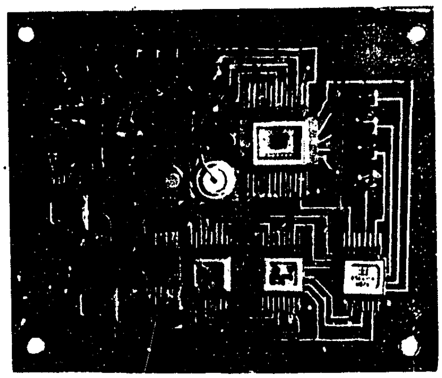

Figure 3. Appearance of PC board with CCD photodetector and controller.

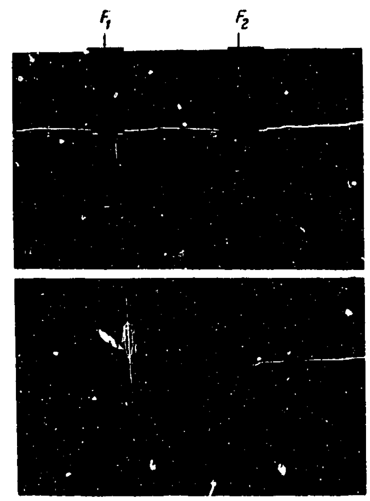

Figure 5. Output signal from spectrum analyzer corresponding to spectra of two radio pulses. F_1=123 MHz, τ_1=10 μsec, F_2=126 MHz, τ_2=3.5 μsec (a) and 1 μsec (b).

The CCD strip was located in the output focal plane of the spectral analyzer, and the signal taken from it was recorded on an S1-76 oscillograph. The following were the parameters of the CCD controller: charge accumulation time in CCD elements T_a=10 msec; signal output time from one element 10 μsec; time to read information from entire strip 0.75 msec.

The operation of the CCD photodetector in the spectrum analyzer was investigated with pulsed input radio signals formed in two independent channels (figure 4). Parallel signal processing is one of the primary advantages of acoustooptical spectrum analyzers.

Figure 4. Functional diagram of acousto-optical radio signal spectrum analyzer. AOM - acoustooptical modulator, L_1, L_2 - collimating lenses, L_3 - integrating lens, 1 - laser, 2 - CCD, 3 - control unit, 4 - recording unit.

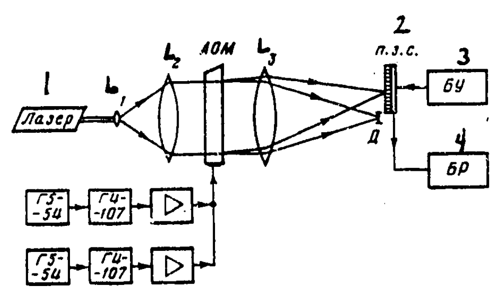

Figure 5 a and b illustrate the operation of the spectrum analyzer. The oscillograms show the output signals of the spectrum analyzer which correspond to the spectra of two radio pulses with different duration and carrier frequency. In order to increase the s/n ratio and to provide visual clarity, the pulse repetition T_p is significantly shorter than the accumulation time T_a ($T_p/T_a \approx 0.05$).

The parameters of the matching optical system were selected so that there were approximately 2 CCD elements per spectrum analyzer resolution element (ΔF_{min}= 100 KHz). It is apparent from Figure 5a and b that the shorter pulses (τ_2=3.5 μsec and τ_2=1 μsec) with spectra of $\Delta F_2 \approx 300$ KHz and $\Delta F_2 \approx 1$ MHz, are recorded by a larger number of CCD elements than a pulse with duration τ_1=10 μsec.

The sufficiently high sensitivity of the photodetector and low dark current level made it possible to record the spectra of single pulses lasting ≥1 μsec. The energy of the optical radiation pulses received by an individual CCD element comprises $\sim 10^{-13}$ J. The laser radiation was pulse modulated during measurement of the spectra of single short pulses, which made it possible to reduce the noise level. The modulation period was synchronized with the time of arrival of the radio pulses and the read period of the signal from the CCD strip.

We used an analogous CCD photodetector as an output device in an integral-optical spectrum analyzer. Our work with linear CCD photodetectors demonstrated their simplicity and convenience for use in aligning and adjusting the optical system in the spectrum analyzer, and for recording the output signal.

Linear CCD photodetectors with 500-800 elements have now been developed [6] whose controllers are essentially the same as those examined above. The use of these photodetectors will make it possible to improve significantly the parameters of optical processing systems as a whole, and in particular to increase the number of channels in spectrum analyzers, and simplify processing of wideband signals. CCD photodetectors can be used in spectrum analyzers as well as other optical processing systems, e.g., acoustooptical correlators [7].

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NEW ACTIVITIES, MISCELLANEOUS

UDC 621.384.3

APPLICATION OF INFRARED TECHNOLOGY IN THE NATIONAL ECONOMY

Leningrad PRIMENENIYE INFRAKRASNOY TEKHNIKI V NARODNOM KHOZYAYSTVE in Russian 1981 (signed to press 27 Jul 81) pp 2-5, 263-264

[Annotation, foreword, table and table of contents from book "Application of Infrared Technology in the National Economy", by Isidor Borisovich Levitin (deceased), Energoizdat, 8000 copies, 264 pages]

[Text] Annotation

This book generalizes and systematizes domestic and foreign experience in the application of modern infrared technology in industry, agriculture, science, medicine, etc. The book presents the results of numerous investigations and developments, describes methods for analyzing radiating devices and radiation modes, and contains a description of various technical devices.

The book is intended for engineering and technical workers who use infrared technology, and may be useful to students in institutes of higher education.

[This book was reviewed by M.G. Tsokurenko.]

Foreword

Deep roots connect one of the branches of modern light technology -- infrared technology -- with the similar ultraviolet technology. Infrared technology uses the same physical bases, concepts, terminology, a number of relationships, etc., although of course, infrared technology also has its own specific characteristics which promote its extremely broad area of application for both peaceful and military purposes.

The present book touches exclusively upon peaceful uses of infrared technology in the economy, although by no means all of them (which would require a much larger book). Nonetheless, the most important aspects of these applications, albeit with insufficient completeness, are presented here, often in an attempt to allow the reader to become acquainted with the principles of designing and analyzing infrared devices. In particular, the book introduces a method for analyzing IR heating devices developed by N.N. Yermolinskiy which has not been fully published before and which is of undisputed interest regardless of the analytical methods developed by other authors which are in use. N.N. Yermolinskiy's method is closer to familiar methods in light technology, is distinguished by its simplicity and provides accuracy sufficient for practice.

Table P-1, borrowed from R. Hudson's familiar monograph [167] gives an idea of the variety of areas of application of IR technology for peaceful purposes -- in production, construction, agriculture, science, medicine, etc. It should be noted that the areas of application of IR technology are continuously expanding, as a result of which no review can pretend to sufficient completeness of information in this sense.

For the reader interested in supplementing information regarding various areas of the use of IR technology, our first recommendation is a regular familiarization with the abstract journals of the All Union Institute of Scientific and Technical Information ("ELEKTROTEKHNIKA I ENERGETIKA", "FIZIKA", "BIOLOGIYA", "ISSLEDOVANIYE KOSMICHESKOGO PROSTRANSTVA" etc.).

Table P-1

Area of application, purpose	Industry and transportation	Medicine and biology	Scientific research
Active systems	Infrared heating and drying. Beam heating. Infrared soldering and welding. Guarding plant and storage areas. Aircraft landing. Registering through transportation. Estimating relative speed of transportation facilities. Preventing motor vehicle collisions.	Beam thermal therapy. Determining distance from obstacles (for the blind)	Space communications. Landscape illumination for night motion picture and still photography. Investigation of mechanism of communication between animals. Studying noctural animal life
Searching, tracking and range measurement	Detecting forest fires. Guiding fire-control rockets. Fire detection in aircraft tanks. Prevention of fuel explosions	Automatic guide for the blind	Space navigation and spaceflight control from the earth. Vertical sensors. Satellite detection. Orientation of optical (astronomical) instruments. Investigation of optical structure of horizon

Area of application, purpose	Industry and transportation	Medicine and biology	Scientific research
Radiometry	Non-contact measurement of temperature of industrial facilities (cutting tools, rolled metal, brake linings, etc.). Integrity testing of electrotechnical equipment. Non-contact dimension measurement. Technological process control. Determination of railroad journal box overheating.	Noncontact skin temperature measurement. Investigation of temperature perception. Early diagnosis of cancer. Monitoring wound healing without removal of dressings. Remote biosensors.	Measurement of the temperature of the moon, planets and stars. Remote determination of weather conditions. Measurement of earth's heat balance. Investigation of heat transfer in plants. Forensic examination.
Spectral radiometry	Detection of air turbulence. Chemical analysis of organic compounds. Analysis of gases. Detection of oil in water. Finding pipeline leaks.	Detection and prevention of air pollution. Determining CO_2 content in blood and exhaled air.	Determining composition of the atmosphere of the earth and other planets. Monitoring traces of life on other planets.
Obtaining thermal image	Non-destructive testing of articles. Testing effectiveness of sheet insulation. Testing optical materials.	Early cancer diagnosis. Early diagnosis of pre-infarct condition. Placental localization. Determination of optimal amputation point. Investigation of effectiveness of polar clothing.	Prospecting for earth's resources. Forest fire detection from satellites in aircraft. Investigation of heat flow. Volcano study. Detection and investigation of pollution of bodies of water. Detection of fissures in icebergs. Iceberg surveys.
Utilization of reflected beam flux	Industrial supervision and accident prevention. Observation of photographic film during pro-	Measurement of diameter of the pupil of the eye. Examination of the eye when cataracts	Determining nature of surface of moon and planets. Identification

Area of application, purpose	Industry and transportation	Medicine and biology	Scientific research
	duction. Nocturnal movie and television imagery. Determination of types of trees in mixed forests.	present. Investigation of obstructed and varicose veins. Monitoring eye movements. Monitoring wound healing process. Studying nocturnal animal life.	of points in archeology, portraiture, etc. Palientology investigations. Investigation of documents. Analysis of water quality. Detection of plant disease.

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