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CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 13/82)

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USSR REPORT

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 13/82)

CONTENTS

HARDWARE

UDC 681.327.6:681.84.083.82

STATE OF THE ART AND PROSPECTS FOR USE OF MAGNETORESISTIVE AND INTEGRATED HEADS

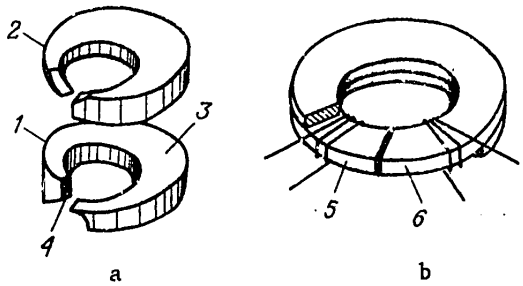
Moscow IZMERENIYA, KONTROL', AVTOMATIZATSIYA in Russian No 6, Nov-Dec 81 pp 34-42

[Article by Yu. L. Bogorodskiy, candidate of engineering science, and Ye. F. Korolev, engineer]

[Excerpts] Because of the application of magnetic heads using the design in question and the progressive technology for manufacturing them, which provides high precision in executing the profile of the magnetic heads, a very small gap (about 0.1 - 0.2 micrometer) between the magnetic head and the recording medium has been obtained. This is especially important for a relatively thin medium, the thickness of which is comparable to the gap value [33]. Using integrated technology enables achieving unity of the technological base in the mass production of both recording media and magnetic heads. In the process, even in vacuum deposition equipment series produced by domestic industry [34], obtaining up to a hundred or more integrated heads on one substrate in one processing cycle is attainable.

In addition to a high degree of integration and suitability to manufacture of magnetic heads, integrated technology enables creating heads with very high reliability and very small weight and dimensions. One should not think however that integrated technology in the immediate future will exclude heads with solid mass cores from application. Preference for application of a particular technology will be determined for a long time by the various economic factors, taking design innovations into account of course. The fact is, in particular, that the chief difficulty in manufacturing solid mass cores--obtaining effective gaps--can be overcome by various methods. The most progressive of them is changing to helical designs that permit excluding the operation of cutting the gap in the core [35-37]. Examples of heads with helical articulations of half-cores are shown in fig. 10.

The head in fig. 10a consists of two C-shaped cores 1 and 2. Core 1, made of magnetically soft material, has helical surface 3 that fully matches the lower surface of core 2. Face surface 4 of core 1 has a nonmagnetic film of silicon oxide or glass. Its thickness is made equal to the head gap size. When the upper section is placed on the lower and they are rotated toward each other, the face parts of the cores are joined



a b

Fig. 10

tightly together, as a result of which a ring magnetic circuit is formed. The cores can be metallic or ferrite. The head in fig. 10b consists of two flat plates 5 and 6 which have the shape of an opened ring. The rings are curved in a helical curve. Compared to previous designs, the advantage of this one is that head dimensions in width are not at all restricted and can be made quite small. Such a head, while keeping the advantage of a ring solid mass magnetic circuit, approximates the integrated in its properties.

Area of Application of Integrated Heads. Since magnetic recording has now entered into essentially all spheres of human activity and its characteristics are starting to noticeably affect the rates of scientific and technical progress, it is expected that the demand for integrated heads will increase. The clearest examples of the use of the technology of recording on a magnetic medium are the uses of studio audio and video magnetic tape recorders in radio and television, astronomy and astrophysics, space technology and aviation, computer technology, defectoscopy, automation and remote control, measuring technology, etc. [1, 38-40]. The rapid development of electronic computers, automated control systems and data banks caused an insistent need for development and improvement of storage equipment in the form of disk, drum and tape units. In these devices, magnetic heads are major components, along with the electronics, media and moving mechanisms.

Since these systems operate with digital information, pulse recording methods, requiring the use of pulse magnetic heads, are used in the storage units. Under the conditions of mass production of them, integrated technology is the most preferred, for the manufacture of the basic elements of large computers is very consistent with thin-film technology. In the process, because of the rapid wear of integrated heads when there is contact with the recording medium, they are applied mainly in units of heads of the floating type, which ensures noncontact recording.

Integrated technology permits organizing mass output of heads with such high characteristics that this has an immediate effect on the overall characteristics of the equipment in which they are used [29, 41]. Thus, for example, the use of integrated heads in disk storage units led to a 2.5-fold reduction in disk diameters and also a reduction in costs for storing the information coming into the units [42]. Media with narrower magnetic tracks, as well as the combined design of a magnetic head and integrated amplifier for reproduction permit in this case eliminating a large share of the noise and adjustments.

Extensive possibilities have been opened in measuring technology in connection with the application of integrated magnetoresistive heads as highly sensitive probes for research of magnetic fields. Here they are competitive with Hall sensors. Also expected is the use of magnetoresistive heads in devices for numeric program control of metal-cutting tools, where low-sensitive heads substantially simplify the structure of the control units.

* * *

Many foreign corporations and firms are now beginning to seriously consider magnetoresistive heads and especially their integrated forms. The capital investment in research to improve the new type of sensors and develop more progressive manufacturing technology for them is steadily growing. A large number of patents have appeared for magnetoresistive heads and new technology for deposition and magnetic electroplating. Considerable advances are expected in the technology of recording analog information by digital methods based on using integrated heads, metallized tapes and integrated amplification technology.

Introducing thin-film technology into the production of magnetic heads is yielding the following advantages:
the frequency response of the "recording-reproduction" path is being improved because the heads are made in the form of a laminated structure of films with magnetic orientation, which provides good flux linkage between the winding and operating gap,
longitudinal recording density is being increased because of the improvement in the shape (geometry) of the head magnetic field,
lateral recording density with precise bounds between magnetic tracks is being increased,
high head reliability and durability are being achieved because of the structural integrity, standardized manufacturing technology and application of new materials,
high suitability to manufacture is being achieved which provides for deposition of hundreds and thousands of heads in one cycle, and
the cost of the products is declining under the conditions of mass automated head production.

Also, the magnetoresistive effect combined with integrated technology makes it possible to substantially reduce the size and weight of storage devices while keeping their high reliability. All these considerations demand a serious attitude toward the development of the new important direction in storage technology and the performance of profound scientific research investigations.

BIBLIOGRAPHY

30. USSR Patent 580577, "Method of Manufacturing Integrated Magnetic Heads," Tikhonov, A. A.; Filatov, I. N.; Khaletskiy, M. B. and Khamayeva, T. Ye., published in B. I. [Bulletin of Inventions], No 42, 1977.

31. USSR Patent 302747, "Method of Manufacturing Units of Magnetic Heads," Timofeyev, B. B.; Taranukha, A. I. and Khishchuk, Yu. A., published in B. I., No 15, 1971.

32. USSR Patent 691920, "Method of Manufacturing Integrated Magnetic Heads," Ryzhkova, I. A.; Spirina, I. A. and Khodzhayev, V. D., published in B. I., No 38, 1979.

33. Korolev, Ye. F., "Analysis of Process of Magnetic Recording on Relatively Thin Medium by (Prysock) Method," ELEKTRICHESTVO, No 9, 1980, pp 66-69.

34. Danilin, B. S., "Vakuumnaya tekhnika v proizvodstve integral'nykh skhem" [Vacuum Technology in Integrated Circuit Production], Moscow, Energiya, 1972, 256 pages.

35. USSR Patent 575680, "Core for Magnetic Head," Bogorodskiy, Yu. L.; Pravikov, N. A. and Kotova, L. G., published in B. I., No 37, 1977.

36. USSR Patent 687463, "Magnetic Head," Paukov, Yu. N.; Bogorodskiy, Yu. L. and Pravikov, N. A., published in B. I., No 35, 1979.

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37. USSR Patent 633065, "Reproducing Magnetic Head," Paukov, Yu. N.; Pravikov, N. A. and Bogorodskiy, Yu. L., published in B. I., No 42, 1978.

38. USSR Patent 621128, "Signal Correlation Processing Device," Korolev, Ye. F. and Kuznetsov, Yu. P., published in B. I., No 31, 1978.

39. GOST [State Standard] 23044-78, "Inflight Voice Recorder Used in Event of Aviation Accident. Technical Specifications."

40. Korolev, Ye. F., "Methods of Investigating Relative Losses and Measurement of Frequency Response in Magnetic Recording Systems," TEKHNIKA KINO I TELEVIDENIYA, No 2, 1976, pp 37-40.

41. Korolev, Ye. F.; Mukhin, Ye. A. and Zhabin, A. S., "Qualitative Indicators of Video Recording on Magnetic Disk," TEKHNIKA KINO I TELEVIDENIYA, No 3, 1974, pp 68-69.

42. Manuel, T., "Computers and Peripherals," ELEKTRONIKA [ELECTRONICS], Vol 53, No 23 (601), 1980, p 34.

8545
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UDC 538

INTENSITY AMPLIFIERS FOR OPTICAL INSTRUMENTS

Moscow VESTNIK AKADEMII NAUK SSSR in Russian No 2, Feb 82 pp 66-75

[Article by G. G. Petrash, doctor of physical and mathematical sciences]

[Excerpts] The extensive application of amplifiers in optical instruments could lead to revolutionary transformations in instrument optics.

There has been recent intensive research on various methods for recovering the wave front with the aid of nonlinear interactions in various mediums. In some versions of the method it is possible to recover the wave front through amplification. As far as is known by the author of this article, these amplifying methods have still not been used in optical instruments. The difficulty in using them is associated in particular with the fact that extremely high powers are required to effect nonlinear conversions.

The first laser mircoprojector was built in 1972 in the optical laboratory of the USSR Academy of Sciences Institute of Physics imeni P.N Lebedev. The amplifying element of a laser based on copper vapor was used as the amplifier. Measurements showed that the amplifier made it possible to amplify the intensity of light beams carrying the image of a microscopic object by a factor of several hundred to more than 10,000. Maximum amplification is achieved with minimum power for brightening the object. As the strength of the beam increases the amplifier approaches saturation and amplification falls off. Here it was possible to use a considerable part of the energy stored in the amplifying medium. Mean power in the exit beam from the microprojector was only several times less than in a laser with the same amplifier, at 1.5-2.5 W. This power is adequate to obtain an image of a microscopic object on a screen measuring 25 sq. meters. When a microscopic object enlarged by a factor of eight was used, the linear increase on the screen exceeded 10,000. These results lie far beyond the possibilities of normal microprojectors. Here the amplifying element had no marked distortions and the resolution of the instrument was not impaired.

Later other pulsed lasers operating on metal vapors were used as the intensity amplifiers in microprojectors. It turned out that all the amplifiers tested made it possible to obtain significant and efficient amplification (some characteristics are shown in a table). Brightness-intensified images of a microscopic object without marked distortions were obtained with all amplifiers in various spectral fields.

New models of industrial versions of laser microprojectors for use mainly in microelectronics, have now been developed. In these instruments provision has been made for a facility to employ treatment by a laser beam focused on an object in a small spot (down to 1 micrometer) with continuous monitoring of the treatment process on a screen.

Optical systems with intensity amplifiers still constitute a quite new field of optics. It is, therefore, at present difficult to assess their possibilities and problems that may arise in development. Nevertheless, already the great future foreseen for optical systems with intensity amplifiers can be assessed.

There are now high-resolution photographic materials that make it possible to record high-quality images on a small area. The use of these materials can substantially reduce the area of the frame in motion films. This would lead to a sharp drop in demand for cine film and silver, which is in short supply, and would reduce the size of cinematographic equipment. However, given the present projection equipment, it is not possible to do this because the light loads on the film during projection onto a screen are already extremely great. The use of intensity amplifiers could provide a radical solution to this problem.

Definite prospects have also been opened up for developing new systems for projecting television. The use of an intensity amplifier in projection would make it possible to substantially reduce the light load on the information medium, which in this case could be a controlled reflector or diapositive. In principle, in this case, too, the size of the information medium, controlled, for example, by microelectronics, could be reduced to down to 1 micrometer, and adequate illumination on the screened would be obtained by intensity amplifiers of the required sizes.

Yet another possibility that could already be developed relatively simply is to take photomicrographs at a frame speed of 10-20 kHz. For this, all that is required is to scan in time the images received at the amplifier output, since the duration of image reproduction for lasers now in use is 10-30 nanoseconds.

Of course, great opportunities also exist for the development of laser microprojectors. The various versions of microprojectors with intensity amplifiers still need to be worked out: polarized and interference microscopes, stereomicroscopes, systems with phase contrast and so forth. The possibility exists of considerably improving methods for mircotreatment with a laser beam with monitoring on the screen of the microprojector.

Great possibilities for the use of the intensity amplifier are also being opened up for infrared technology. Within the IR spectral range it is easier to obtain sufficiently high amplification, and therefore realization of these amplifiers should be simple. In this spectral range, for example, it is easier to build an amplifier that operates in continuous mode, or an amplifier with a broad amplification band. On the other hand, the visualization of infrared images present great difficulties which would be much easier to overcome if the image were formed by a beam of sufficient power, and here it is possible to used a low-sensitivity visualizer of nonlinear conversions.

Attractive possibilities for using intensity amplifiers exist in holography. The use of the amplifiers in recording of holograms would make it possible to use

low-sensitivity recording mediums or sharply reduce recording time. At the stage of reproduction the amplifiers would make it possible to substantially reduce the light load on the hologram and it would be possible to use holograms with low diffractive efficiency, retaining high intensity at the output thanks to amplification. This could turn out to be especially important for dyanmic holography.

The list of prospects for the development of optical systems with intensity amplifiers, and the problems occurring in their development and extensive spread could, of course, be continued, but what has been said is enough to conclude that these prospects are very interesting and that it is time to start serious work on the broad development of optical systems with intensity amplifiers.

To summarize: intensity amplifiers have already been developed and tested on the basis of a number of pulsed lasers operating on metal vapors. They have turned out to be quite suitable in the development of instruments designed for specific practical applications. With their aid it has already been possible to solve a problem that could not be solved on the basis of traditional optical instruments. The development of these amplifiers has also made it possible to embark on studies of the features of optical systems with intensity amplifiers and to develop their physical bases, and also to develop new instruments for practical applications.

This work, however is still being carried on within a very narrow framework and with little effort, which does not accord with the important prospects being opened up in optics by the use of intensity amplifiers.

9642
CSO: 1863/151

ELEKTRONIKA B3-19M CALCULATOR HANDBOOK

Moscow TEKHNIKA VYCHISLENIY NA MIKROKAL'KULYATORE "ELEKTRONIKA B3-19M" in Russian 1981 (signed to press 2 Dec 81) pp 2, 5-6, 8, 10-13, 166-167

[Annotation, excerpts from chapter 1, and table of contents from book "Doing Calculations on the 'Elektronika B3-19M' Calculator", by Mikhail Ivanovich Petrov, Izdatel'stvo "Finansy i statistika", 15,000 copies, 168 pages]

[Excerpts] The book deals with methods and practice in doing calculations on the "Elektronika B3-19M" calculator. Examples are shown for solving systems of linear and nonlinear equations, numerical function integration and differentiation, and integration of differential equations, and questions of solving problems in economics are considered. Each chapter contains examples for the reader himself to solve; answers are provided.

The book is intended for scientific-engineering and scientific workers, economists and VUZ stduents.

The time taken to carry out arithmetical operations is less than 0.2 sec. Average time for determining functions ln x, lg x, sine a, cos a, tg a, arcsin x, arccos x, and arctg x is less than 2 seconds. Maximum absolute error when using the arithmetic functions is less than unity for the smallest digit of a number. Absolute and relative error occurring in determination of functions calculated by the calculator are indicated in the appropriate sections of the text.

The calculator is powered by four DO,55SU1,1 batteries or from a 220V 50Hz power supply. The batteries provide continuous operation of the calculator for 3 hours, after which they must be recharged from a mains power supply. Maximum power consumption is 0.8 W. Power consumption from an AC power supply, taking battery recharging into account, is less than 7 W.

The calculator is designed to operate within a temperature range of 10-35°C at relative air humidity of 30-80% and a barometric pressure of 760±25 mmHg. Overall dimensions are 166.5 X 86 X 41 mm and the weight is less than 0.4 kg.

The arithmetic-logic device is for arithmetic and logic operations on figures and commands (codes). It is based on an adder and X, Y, and Z registers (K145IK3 and K145IK4 microcircuits).

Figure 1.1 The "Elektronika B3-19M" Calculator

The count control device is used to synchronize and coordinate the operation of all elements in the electronics package during the computing process. Synchronization is effected by passing to the elements of the electronics package controls signals obtained from a TG time-pulse generator (K1GF651 microcircuit). Frequency of the synchronization pulse train is 70±5 kHz.

The data input and output control device distributes data inputted via the keyboard to the appropriate assemblies of the calculator and controls its output on the indicator device. Transistor-based matching elements are used for the combined operation of the indicator and the devices built on microcircuits.

Storage consists of build-up memory (or simply memory) and a ROM. The memory is for holding intermediate results from computation or numbers frequently encountered in a given calculation. Numbers are passed to or retrieved from memory by command given via the keyboard. The ROM stores the programs used to handle figures when finding functions computed by the calculator.

The indicator device enables visual monitoring of inputted numbers and readout of computed results. In the calculator this device is built on the base of type ALS311A LED's and has a 12-digit display.

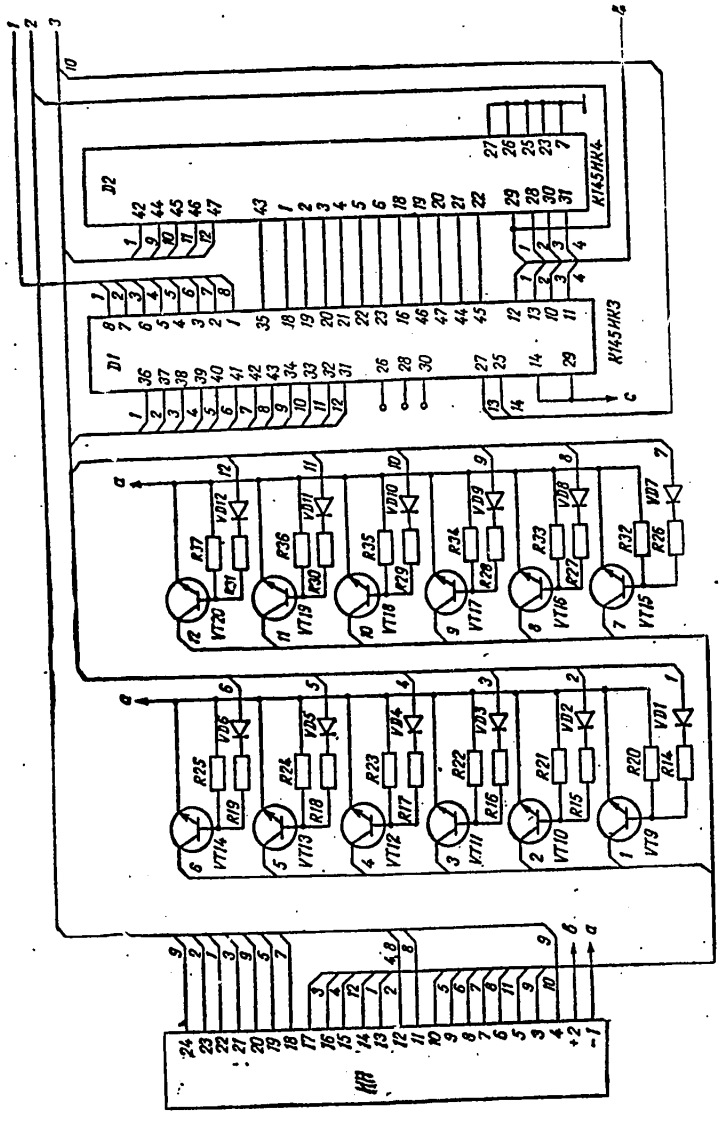

Figure 1.5 Main Circuit Diagram for the "Elektronika B3-19M" Calculator

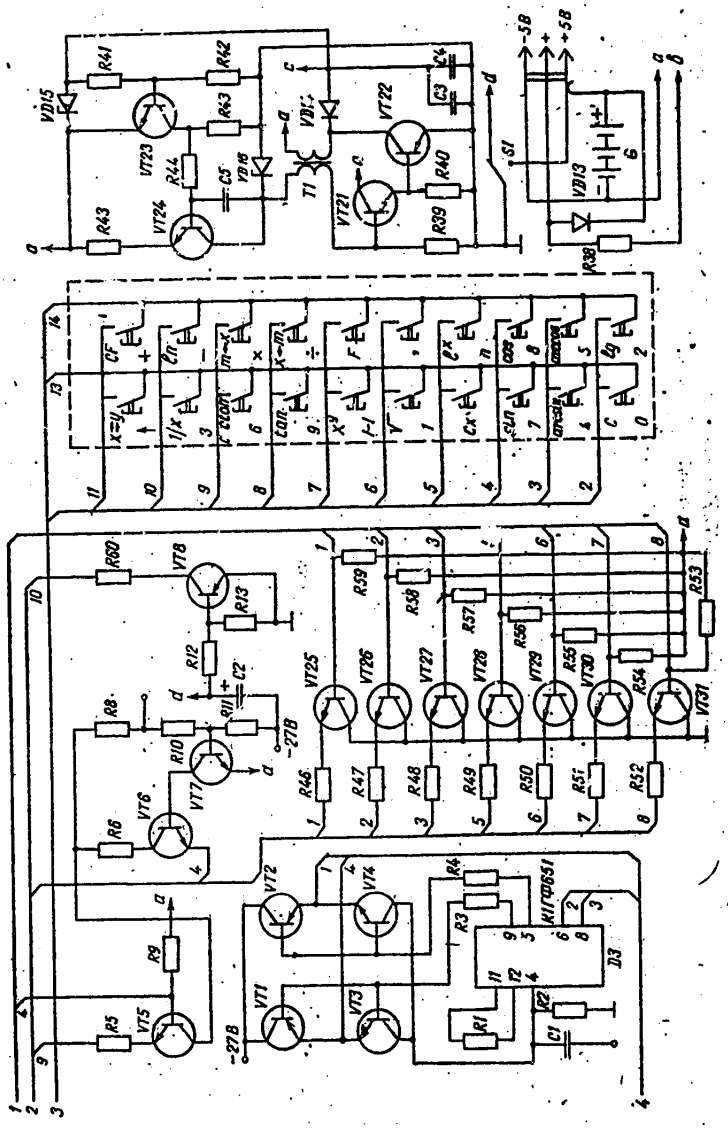

Figure 1.6 Main Circuit Diagram for the "Elektronika B3-19M" Calculator (cont)

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ENHANCED-SPEED MICROPROCESSOR SETS

Moscow MIKROPROTSESSORNYYE KOMPLEKTY POVYSHENNOGO BYSTRODEYSTVIYA in Russian 1981 (signed to press 3 Nov 81) pp 2-4, 165-167

[Annotation, preface, contents & bibliography from book, "Enhanced-Speed Microprocessor Set" by Aleksandr Ivanovich Berezenko, Lev Nikolayevich Koryagin and Artashes Rubenovich Nazar'yan, Massovaya Biblioteka Inzhenera: Elektronika, Izdatel'stvo "Radio i svyaz'", 25,000 copies, 168 pages]

[Text] Microprocessor sets are the elementary basis for the construction of computer hardware and devices of digital radioelectronic apparatus characterized by high reliability, low cost, small dimensions and low power consumption.

It is intended for engineers engaged in the development and application of microprocessors.

Preface

Microprocessor sets are the elementary basis for the construction of computer hardware and devices of digital radioelectronic apparatus characterized by high reliability, low cost, small dimensions and low power consumption.

Thanks to high speed and interference immunity, the possibility of working in a wide range of temperatures and radiation stability, bipolar microprocessor sets based on microprocessor sections made on the technological circuitry base of transistor-transistor logic with Schottky diodes have obtained very widespread use by apparatus developers. The book presented to the reader has also been devoted to this class of microprocessor sets.

Microprocessor sets assure flexibility of planning, both from the point of view of apparatus solutions to satisfy the set productivity of systems and from the point of view of realizing the necessary set of instructions. It is necessary that developer be well acquainted with all features of the structural and functional organization of large-scale integrated circuit microprocessor sets. Only in that case will he be able to realize the potentials of microprocessor sets.

Microprocessor sets contain a broad gamut of processor, interface and storage large-scale integrated circuits for the construction of equipment for various purposes and with various productivity, 2-, 4-, and 8-digit processor sections, 8-, 12-and 16-digit

multipliers, 2-, 3- and 4- general purpose address registers, arithmetic expanders, large-scale integrated circuits for organization of interrupters, control of the store of microprograms, electrically programmable storage devices with capacities of 1, 4 and 16K bits, associative storage units, buffer registers, main-line amplifiers and commutators and large-scale integrated circuits for the organization of synchronous and asynchronous exchange between processors and peripherals.

Transistor-transistor logic with Schottky diodes microprocessor sets consist of large-scale integrated circuits of series K589, KR1802 and KR1804. In view of the limited volume in the book only those of series K589 and methods of constructing apparatus on the basis of them have been examined in detail. It must be noted especially that large-scale integrated circuits of different series are interchangeable, and this permits achieving better characteristics in speed, productivity, dimensions and power consumption in different apparatus.

The book consists of seven chapters. Chapter 1 presents basic information about the selection of the composition and structural organization of large-scale integrated-circuit microprocessor sets. Chapters 2 - 5 are devoted to description of series K589 large-scale integrated circuits and questions of their application. By chapters this material is arranged in the following manner: in chapter 2 is a description of the functioning of the K589 series large-scale integrated circuit and its circuitry; in chapter 3 is a calculation of the time of synchronization cycles for several standard cases of its realization; in chapter 4 the designing of central processors is examined, the realization of apparatus and microcrogram parts is shown, the development of microcprograms by means of a "manual" assembler is shown, and examples are presented of the execution of microprograms for addition, subtraction, multiplication and division, interruptions are analyzed, etc; chapter 5 is devoted to the practical application of series K589 large-scale integrated-circuit microprocessor sets in apparatus micro-computers with a system of mini-computer instructions and a controller for storage on floppy magnetic disks are examined. Large-scale integrated circuits of series KR1802 are briefly described in chapter 6. Chapter 7 is devoted to a description of a system for the automation of microprogramming intended for developers of apparatus based on microprocessor sets.

In presenting the material the authors strove to accent attention to questions which, in spite of their importance, have still not been discussed adequately in the literature accessible to the developers of apparatus based on large-scale integrated-circuit microprocessor sets, or have been discussed insufficiently systematically. Acquaintance with thsee questions mught to contribute to the proper use of microprocessor sets.

The authors are obliged to Doctor of Technical Sciences Professor A. G. Aleksenko and A. V. Kobylinskiy for examining the manuscript and making useful comments.

CONTENTS

BIBLIOGRAPHY

1. Kagan, B. M., and Stashin, V. V. "Mikroprotsessory v tsifrovykh sistemakh" (Microprocessors in Digital Systems). Moscow, Energiya, 1979.

2. Prangishvili, I. V. "Mikroprotsessory i mikro-EVM" (Microporcessors and Micro-Computers). Moscow, Energiya, 1979, 232 pages.

3. Vasenkov, A. A., Vorob'yev, N. M., Dshkhunyan, V. L., et al. "Mikroprotsessornyye BIS i micro-EVM: Postroyeniye i primeneniye" (Microprocessors and Micro-Computers: Construction and Application). A. A. Vasenkov, editor. Moscow, Sovetskoye radio, 1980, 280 pages. Planning integrated microcircuit radio-electronic apparatus).

4. Gal'perin, M. P., Kuzmetsov, V. Ya., Maslennikov, Yu. A., et al. "Mikro-EVM 'Elektronika S5' i ikh primeneniye" (Micro-Computers 'Elektronika S5' and Their Application). V. M. Proleyko, editor. Moscow, Sovetskoye radio, 1980, 160 pages. (Massovaya Biblioteka Inzhenera "Elektronika").

5. Vasenkov, A, A., Konochkin, E. I., Malashevich, B. M., and Shakhnov, V. A. "Terminologiya v tekhnike mikroprotsessornykh integral'nykh skhem i mikro-EVM" (Terminology in the Technology of Microprocessor Integrated Circuits and Micro-Computers). MIKROELEKTRONIKA I POLUPROVODNIKOVYE PRIBORY, 1979, No 4, pp 17-19. A. A. Vasenkov and Ya. A. Fedotov, editors. Moscow, Sovetskoye radio.

6. Shchetenin, Yu. A., and Vorob'yeva, V. V. "Multifunctional Scaling Unit." Ibid, pp 95-1.8.

7. Berezenko, A. I. Koryagin, L. N., and Paramonov, N. N. "Microprocessor Elementary Base of Data Processing Equipment. Structural, Technical Means and Organization of Systems for Automation of Scientific Investigations (Materials of the Tenth All-Union School on Automation of Scientific Iveestigations). Leningrad LIYaF, 1977, pp 59-63.

8. Berezenko, A. I., Koryagin, L. N., Nazar'yan, A. R., and Orlov, B. V. "Microprocessor Set of BIS TTL With Schottky Diodes of Series K589." ELEKTRONNAYA PROMYSHLENNOST', 1978, No 5, pp 20-21.

9. Berezenko, A. I., Berezin, V. I., Kalinin, S. Ye., and Koryagin, L. N. "Micro-Computer Based on a Microprocessor Set of Series K589." Ibid, No 6, pp 49-54.

10. Berezenko, A. I., Koryagin, L. N., and Shchetinin, Yu. I. "Microprocessor Set of Bipolar BIS's." MIKROELEKTRONIKA I POLUPROVODNIKOVYYE PRIBORY, 1977, No 2, pp 80-94. Moscow, Sovetskoye radio.

11. Berezenko, A. I., Kasperovich, A. N., Prokopenko, V. I., Nesterekhin, Yu. B., Koryagin, L. N., and Sluyev, V. A. "Crate Controller CAMAC Based on a Microprocessor Set of BIS's." PRIBORY I SISTEMY UPRAVLENIYA, 1978, No 9, pp 11-14.

12. 1977 Data Catalog of Intel, USA.

13. Nesterov, P. V. "Development and Evaluation of the Architecture of Microprocessors." ZARUBEZHNAYA RADIOELEKTRONIKA, 1977, No 4, pp 32-69.

14. Proleyko, V. M. "Development of Microprocessors, Micro-Computers and Systems Based on Them." ELEKTRONNAYA PROMYSHLENNOST', 1979, No 11-12, pp 3-6.

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STRUCTURAL ORGANIZATION AND COMPOSITION OF MICROPROCESSOR SETS

Moscow MIKROPROTSESSORNYYE KOMPLEKTY POVYSHENNOGO BYSTRODEYSTVIYA in Russian 1981 (signed to press 3 Nov 81) pp 5-15

[Chapter 1 from book "Enhanced-Speed Microprocessor Set" by Aleksandr Ivanovich Berezenko, Lev Nikolayevich Koryagin and Artashes Rubenovich Nazar'yan, Massovaya Biblioteka Inzhenera: Elektronika, Izdatel'stvo "Radio i svyaz'", 25,000 copies, 168 pages]

[Text] 1.1. Classification of Microprocessor Large-scale Integrated Circuits (BIS)

All microprocessor BIS's can be divided into three classes: single-crystal micro-computers, microprocessor sets based on single-crystal microprocessors, microprocessor sets (MPK's) based on processor sections, or sectionalized MPK's (SMPK's).

Single-crystal micro-computers contain a central processor with a fixed structure and system of instructions, a main memory with random access and a mask-type ROM. Due to limited area of the crystal the capacity of the main memory and permanent memory is not more than 2-3 Kbytes, and so the area of their application is programmable controllers, commercial calculators, cash registers, etc. Single-crystal micro-computers are much less expensive than micro-computers made with microprocessor sets.

A microprocessor set based on single-crystal microprocessors includes: a large-scale integrated-circuit microporcessor containing a processor with with a fixed structure and instructions list; a large-scale integrated-circuit ROM (the mask-type or electrically programmable; a large-scale integrated-circuit interface of input-output devices (UVV); a large-scale integrated circuit of controllers, generators, timers, etc. The microprocessor set can include a matrix large-scale integrated circuit for the realization of ordered circuits for control, communications, etc.

The fixed structure of a single-crystal multiprocessor does not permit using microprocessor sets based on them for the construction of powerful computer systems and high-speed data processing equipment. The existing inadequacies of MPK's are the limited possibilities of exchanging information with the external environment, organization of parallel processing and increase of productivity. The capacity of programs of systems constructed on the basis of a single-crystalline MPK can reach 64K bytes, the time of performance of instructions from 2 to 10 microseconds, and the cost is the average between single-crystalline micro-computers and systems with sectionalized MPK's. The area of application is micro-computers, controllers, data transmission apparatus, devices of automation, etc.

Sectionalized MPK's include a minimum number of BIS's, compatible with each other, of different functional purpose (processor, interface, ROM's, main memories, etc), by means of which it is possible to realize structures with different organization and digit capacity, a multiple of 2, 4 and 8. The instructions list is selected by the system developer in accordance with its specific purpose and is realized by the microprogram method by recording in the storage unit microprograms based on the main memory or the electrically programmable ROM's.

The breakdown into sections of the processor and interface parts permitted creating large-scale integrated circuits with different bus organization: combined, separate, two-directional and also with different structural organization to increase the informational capacity horizontally and vertically, which permits realizing modular structures with highly efficient communication between them, including also the conveyer method of processing. The capacity of system programs based on sectionalized microprocessor sets can amount to several hundred kilowatts.

The use of SMPK's is effective in cases where maximum productivity is necessary, that is, in universal and specialized computers realizing various instruction lists in controllers and radio engineering equipment, and also in equipment for real-time signal processing, digital filtration and spectrum analysis. Those areas of application cannot be realized on micro-computers and single crystalline microprocessors, and so questions of the development and improvement of large-scale integrated-circuit sectionalized microprocessor sets are an important direction in the development of microprocessor technology.

Table 1 [TsPE = central processor element]

BIS Series MPK	Technology	Number of BIS types	BIS TsPE capacity, bits	TsPE cycle time, microseconds
K587	KMOP	4	4	2.0
K588	KMOP	3	16	2.0
K582	I^2L	5	4	1.75
K583	I^2L	12	8	1.0
K584	I^2L	4	4	1.0
K537	p-MOP	11	8	10
K589	TTLSh	10	2	0.1
KR1802	TTLSh	15	8	0.15
KR1804	TTLSh	6	4	0.12

Table 1 presents the SMPK's produced industrially. MPK of series K587, K588 include BIS of microprogrammed control devices in which instruction lists of the type NTs are realized for series K587 and K588, and S5 for series K536. The instruction list can be changed by replacing a single photographic pattern in the course of BIS manufacture.

1.2. Principles of Construction of MPK BIS

The following principles have been made the basis of the development of MPK BIS: modular construction of systems on the basis of of MPK BIS and main-line organization of communication between modules; arbitrarily increasable digit capacity; expandable

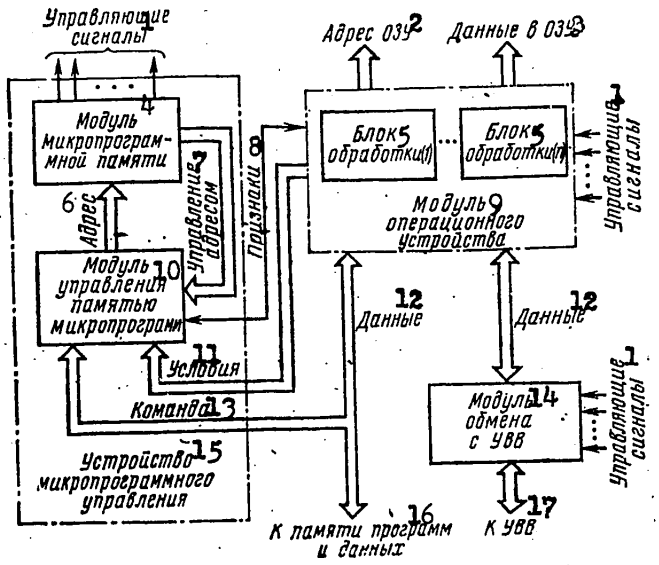

Figure 1. Structural diagram of modular microprocessor

1 - Control signals
2 - Main store address
3 - Data in main store
4 - Microprogram memory module
5 - Processing unit
6 - Address
7 - Address control
8 - Signs
9 - Operating device module
10 - Microprogram memory control module
11 - Conditions
12 - Data
13 - Instruction
14 - Module for exchange with input-output devices
15 - Microprogram control device
16 - to program memory and data
17 - to input-output devices

volume of general-purpose registers (RON); multi-functionality of BIS and their specialization according to basic purpose (processing, control, commutation, interface, memory, etc); functional completeness of MPK; the possibility of constructing on the basis of MPK devices with data processing in series and in parallel; microprogram control with the realization of any known instruction lists under the conditions of the user, and also of arbitrary algorithms on the microprogram level; logical, electrical and constructive compatibility of BIS and a single principle of organization of synchronization in MPK-based systems.

Figure 1 presents a basic structural diagram of a modular microprocessor(MP) with main-line organization of communications between the modulators and microprogram control to realize MPK equipment. The basic MP modules are: a module of operational equipment, a module of control of the store of microprograms, a module of microprogram memory and a module of exchange with input-output devices (UVV). The MPK includes BIS by means of which each each module, depending on the required capacity and speed, can be realized on one, on several BIS of the same kind or on several different BIS.

The operational equipment module is intended for processing addresses and data and includes: units for arithmetic and logical calculations, a memory of general-purpose registers and a local control device. Various alternative constructions of the module are presented on Figure 2. On Figure 2a the arithmetic-logical units (ALU) and RON's are combined into a single BIS, and the number of RON's does not increase. On Fibure 2b the ALU's and RON's are executed in separate BIS's and can can increase independently of one another:: the ALU's in accordance with the digit capacity and the RON's in accordance with the digit capacity and the number of registers. To increase the productivity, additionally introduced into the ALU's and RON's are arithmetic expanders (AR) performing apparatus displacements, multiplication and division (see Figure 2c). The line organization is different for different BIS's: two input information lines, separate output address and data lines (Figure 2d); two-directional data lines (Figure 4e); input and output data lines (single-directional and separate) (Figure 2f).

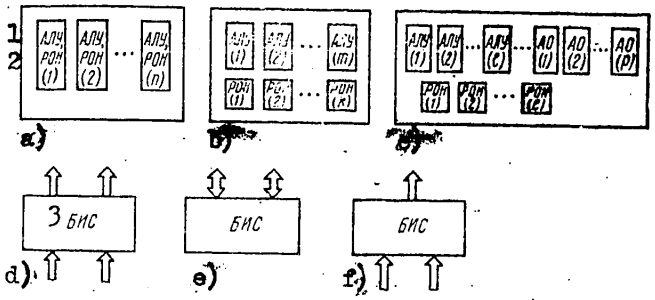

Figure 2. Variants of modular structures.
1 - ALU 2 - RON 3 - BIS

The processing of instruction information during realization according to Figure 2d is done successively with the processing of numerical information. During realization of a module of the operating equipment on a BIS with a structure of lines corresponding to Figure 2e and f, the same units can be used to process the instruction information as for calculation of numerical information, but in that case it is necessary to use a peripheral to store the ROM address.

The module for control of the microprogram memory is intended for reception of an instruction, the calculation of successive addresses for the microgram memory, depending on the signs arriving from the operating equipment, and external and internal interruptions.

The microprogram memory module is intendeded for storage of control information for all MP modules. To realize a module, BIS's of electrically programmable storage devices with a capacity of 1, 4 and 16K bits are included in the MPK. To organize the conveyer principle of microprogram control on the output of the microprocessor memory it is necessary to additionally use registers with with recording on the front, available in the standard series K155.

The module of exchange with input-output devices is intended for the reception and issuance of information, and also for the organization of priority processing during work of the microprocessor with peripherals. To construct the module,

the MPK includes a BIS of priority interruption, interface adapters, multi-regime registers and line formers.

To control the main lines and construct synchronization devices the set includes the BIS of the main-line commutator and the BIS of a multi-functional synchronizing device.

The logical, electrical and constructive compatibility of the MPK BIS is achieved by a single presentation of information with standard levels of signals TTLSh (the input voltage U^0_{in} = 0 - 0.8 V, U^1_{in} = 2.0 - 5.25 V; the output voltage U^0_{out} = 0-0.5 V, U^1_{out} = 2.4 - 5.25 V), the application of a single voltage of a power sourse of 5 V $\pm$5% and plastic casings with a vertical arrangment of the outputs with a spacing of 2.5 mm and 16, 24, 28, 40, 42, 48 and 64 outputs.

All BIS MPK work in the temperature range of -10 to 70°C.

1.3. Composition of MPK's and Characteristics of BIS's

The TTLSh (transistor-transistor logic with Schottky diodes) MPK consists of logical BIS's of series K589, KR1802 and KR1801 and BIS PROM of series K556 (Tables 2 and 3).

To construct the operating device module, into the MPK are introduced two BIS MP of sections, the BIS of an arithmetic expander (AR), four BIS's of multipliers (YM), the BIS of a summator (SM) and a circuit of transfer acceleration (CUP).

The central processor element (TsPE) is a two-digit section with 11 single-address RON's, two two-bit input information lines, an input two-bit line mask, separate two-bit address and data lines, controlled by separate inputs. Arithmetic, logical and shift operations are performed. The line organization corresponds to Figure 2e. Arithmetic, logical and shift operations are performed with the possibility of masking input data. Signs of equality to zero of the result and of overflow are produced.

The arithmetic expander (AR), a 16-place device, performs in one cycle arithmetic, logical and cyclic shifts to the left and right, and also the operation of retrieving the number of the left unitary bit; the line organization corresponds to Figure 2e.

To organize accelerated transfer during increase of BIS TsPE and AU a circuit of accelerated transfer for eight groups is used.

To construct super-operative stores a module of processing and registry of memory in in the control device, in the MPK there are separate BIS's of a 2- 3- and 4-address registry memory. The RON has 16 two-address general-purpose registers with four places each. It increases in the number of registers and in digit capacity, and the line organization corresponds to Figure 2e. The multi-functional matrix of associative registers (MAR) has four registers with eight places each, and the BIS can be re-arranged into eight 4-place registers and perform functions of associative selection. The line organization corresponds to Figure 2e. The information exchange circuit (OI) is a 4-address register with the possibility of organizing on one of them a counter and of comparing its contents with the contents of another register; the line organization corresponds to Figure 2e.

Table 2

Description of BIS	Designation	Number of outputs	Power, WT	Speed, nano-seconds
Central processor element (TsPE)	K589IK02	28	1	70
Microprogram control unit (BMU)	K589IK01	40	1.2	60
Accelerated transfer circuit (SUP)	K589IK03	28	0.6	10
Priority interruption unit (BPP)	K589IK14	24	0.8	80
Multi-regime buffer register (MBR)	K589Ir12	24	0.8	40
Line former (ShF)	K589AP16	16	0.7	20
Line former with inversion (ShFI)	K589AP26	16	0.7	16
Multi-functional synchronizing device (MSU)	K589KhL4	16	0.8	40
Programmable permanent storage unit (PPZU) per 1K bits	K556PT4	16	0.7	70

For the construction of the microprogram control equipment there are BIS's of the microprogram control unit (BMU), an electrically programmable logic matrix (EPLM), a programmable permanent storage device (PPZU) with a capacity of 1, 4 and 16K bits, The BIS BMU and EPLM are intended for the construction of a module for the control of the store of microprograms, and the BIS PPZU for the construction of a module of microprogrammed memory. The BIS EPLM and PPZU can be used also in other modules and devices of the microprocessor system. The BMU contains all the necessary devices for control of the sequence of microinstructions from the microprogram store of 512 words. The BIS includes functions in the control of interruptions on the microprogram level. The BIS assures the storage of signs and conditional and unconditional transitions. The EPLM on 48 logical products realizes eight output functions from 16 input variables. A PPZU with a capacity of 1, 4 and 16K bits have an organization of 256x4, 512x8 and 2048x8 bits respectively.

For organization of interruptions in the MP system, construction of a model for exchange with the input-output devices and also for the realization of circuits for the control of lines between different modules in the MPK there are the following BIS's; a priority interruption unit (BPP), which assures priority processing interruption requests, permitting realization of multi-level interruptions in systems based on MPK's and having the possibility of increasing the number of interruptions; a multi-regime buffer register (MBR)--a universal 8-place register with a built-in selective logic which has an independent trigger for the formation of a request for interruption of the central processor, intended for realization of many types of interface and auxiliary devices, including data registers and registers with strobing; a multi-functional commutator of main lines (MKM), which commutates information with logical processing from any of four directions into the three others. The line organization corresponds to Figure 2e. The programmable adapter of a successive interfact (PAPI) is an 8-place increasable BIS intended for the organization of series and parallel reception and transmission with control of evenness or oddness. The BIS of the interface (I) produces the necessary signals for organization jointly

Table 3

Description of BIS	Description	Number of outputs	Power, WT	Speed, nano-seconds
Arithmetic device (AU)	KR1802VS1	42	1.2	100
Arithmetic expander (AR)	KR1802VR1	42	1.2	100
General-purpose registers (RON)	KR1802IR1	24	1	50
Serial multiplier (UMP)	KR1802VR2	42	1.2	1000
Parallel multiplier (UM8)	...	42	1.2	100
Parallel multiplier (UM12)	...	64	3	110
Parallel multiplier (UM16)	...	64	4	130
Summator (SM)	...	48	1.2	50
Multi-functional matrix of associative registers (MAR)	...	48	1.2	40
Data exchange (OI)	KR1802VV1	42	1.2	50
Interface (I)	KR1802VV2	42	1.2	100
Programmable adapter of successive interface (PAPM)	...	28	1.0	100
Multi-regime commutator of main lines (MKM)	...	48	1.2	50
Programmable permanent storage device (PPZU) for 4K bits	K556PT5	24	0.8	80
Programmable permanent storage device (PPZU) for 16K bits	K556PT6	24	1.0	100
Electrically programmable logical matrix (EPLM)	K556PT1	28	1.0	50
Microprocessor section	KR1804VS1	40	1.2	110
Accelerated transfer circuit	KR1804VR1	16	0.5	10
Control of microinstruction address circuit	KRR1804VU2	20	0.65	95
Circuit for control of following address	KR1804VU3	16	0.4	40
Parallel register	KR1804IR1	16	0.6	12

with the BIS OI of exchange of information over the combined main line with asynchronous and synchronous exchange discipline. The multi-functional synchronizing device (MSU) is intended for the construction of synchronization and control units and performs functions of frequency division with a controllable coefficient of division, the formation of discretely controllable delay of pulses, a controllable packet of pulses and discretely controllable pulse length. The line former (ShF) and line former with inversion (ShFI) contain four formers each to transmit and receive information respectively with and without inversion and are intended for transmission of information over two-directional lines of communication.

Table 4

Area of Application	Speed	Elementary Base
Input-output devices of computers of control and automation	100 ns	TsPE, BMU, SUP, BPP, MBR, Shf, ShFI, MSU, PPZU, (1K0
Digital equipment of telemetry, radio communications, radar and other types	100 ns	TsPe, BMU, SUP, BPP, MBR, ShF, ShFI, MSU, PPZU (1K)
Computers:		
General purpose	1.4 million operations/s	TsPE, BMU, SUP, BPP, MBR, ShF, ShFI, MSU, PPZU (1K);
Special		AU, AR, RON, UMP, OI, I, PPZU (4K), EPLM
SM computers		
Modernization	2 million operations/s	AU, AR, RON, UMP, OI, I, PPZU (4K), EPLM
New models	4 million operations/s	MKM, MAR, UM (8x8), UM (12x12), UM (16x16), SM, PAPI, PPZU (16K)
YeS computers		
Modernization, peripheral computers for computer xystems	4 million operations/s	MKM, MAR, UM (8x8), UM (12x12), UM (16x16), CM, PAPI, PPZU (16K)
Digital processing of signals:	10 million	MKM, MAR, UM (8x8), UM (16x16),
Radar, hydrolocation and other types	operations/s	SM, PAPI, PPZU (16K)

Table 4 presents the principal areas of application of BIS MPK and the speed of the equipment during minimum apparatus expenditures with the application of a limited type of microcircuits is indicated.

2174
CSO: 8144/1086

PROGRAMMABLE 1024- and 4096-BIT PERMANENT STORAGE UNITS (PROM)

Moscow MIKROPROTSESSORNYYE KOMPLEKTY POVYSHENNOGO BYSTRODEYSTVIYA in Russian 1981 (signed to press 3 Nov 81) pp 60-62

[Sections 2.8 and 2.9 from book "Enhanced-Speed Microprocessor Set" by Aleksandr Ivanovich Berezenko, Lev Nikolayevich Koryagin and Artashes Rubenovich Nazar'yan, Massovaya Biblioteka Inzhenera:Elektronika, Izdatel'stvo "Radio i svyaz'", 25,000 copies, 168 pages]

[Text] 2.8 Programmable 1024-Bit Permanent Storage Unit

Description of its functioning. The PPZU (K556RT4) (Figure 27) represents a BIS of the TTL type with Schottky diodes and is made by methods of planar-epitaxial technology. The data in the PPZU are recorded (programmed) by the user by calcining Nichrome crosspieces by a pulse of current once during operation of the circuit. The information is read during feeding of 0 on the two CS inputs. In any other combination of signals on those inputs we have 1 on the PPZU outputs. During reading the address code of the read word is fed to the outputs of address formers A0-A7. From the outputs of the address formers direct and inverse values of the input code are fed to the input and output decoders. The input decoder selects one of 32 lines of the storage matrices containing 32 bits (eight 4-bit words). To read one of the eight words selected by the input decoder, output decoders are used, controlled by three address inputs. From the output decoders the code of the read word is fed through the reading amplifiers to the external load. The outputs of the reading amplifiers made according to a circuit with an open collector. The device for expansion of selection provides the possibility of selecting a circuit when the PPZU is consolidated into large files.

Before programming, 0's are recorded in the microcircuit for all addresses and digits.

2.9. Programmable 4096-Bit Permanent Storage Unit

Description of the work of the PPZU (K556RT5) (Figure 28). The recording of information in the PPZU (programming) is done by the user through calcination of Nichrome crosspieces by a pulse of current one during the time of operation of the circuit.

Information is read during the feeding of the combination 0011 on CS1·CS2·CS3·CS4 respectively. In the presence of all other combinations on the inputs, logical 1

is on all the PPZU outlets. On the address inlets A3-A* is selected one of 64 rows of the matrix. containing 64 cells. The address inputs A0-A2 control the output decoder which which assures the multiplexing of one of the eight bits for each output reading amplifier. The reading amplifiers are made according to a circuit with an open collector. The presence of four inputs of selection expansion of the microcircuit simplifies the decoding in the creation of a large-capacity memory.

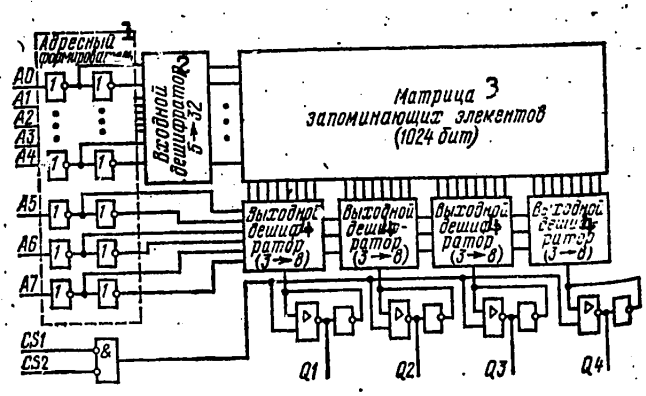

Figure 27. PPZU (K556RT4) structural circuit.
1 - Address former
2 - Input decoder
3 - Storage elements matrix (1024 bits)
4 - Output decoder

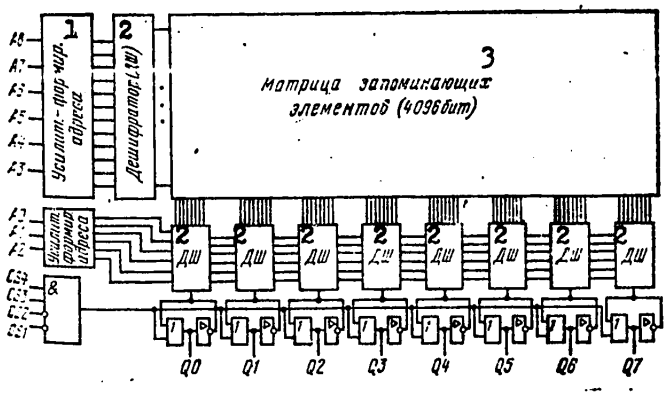

Figure 28. PPZU (K556RT5) structural circuit.
1 - Address amplifier and former
2 - Decoder
3 - Storage elements matrix 4096 bits)

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CSO: 8144/1086

REALIZATION OF COMPUTER HARDWARE ON SERIES K-589 MPK BIS

Moscow MIKROPROTSESSORNYYE KOMPLEKTY POVYSHENNOGO BYSTRODEYSTVIYA in Russian 1981 (signed to press 3 Nov 81) pp 122-132

[Chapter 5 from book "Enhanced-Speed Microprocessor Set" by Aleksandr Ivanovich Berezenko, Lev Nikolayevich Koryagin and Artashes Rubenovich Nazar'yan, Massovaya Biblioteka Inzhenera: Elektronika, Izdatel'stvo "Radio i svyaz'", 25,000 copies, 168 pages]

[Text] With the development of microprocessors and microprocessor sets of large-scale integrated circuits the construction of computer hardware and means of automation has changed substantially. Thus, the application of microprocessor sets of BIS of series K589 on TTL circuits with Schottky diodes, which have broad functional possibilities, makes it possible to effectively solve questions in the creation of micro- and mini-computers for wide use, automated systems for the control of technological processes, computer peripherals, etc.

The present chapter examines the use of MPK BIS of series K589 for the development of micro-computers with simulation of the instructions list of the M-6000 mini-computer and a controller to control the floppy-magnetic disk store.

5.1. Micro-computer Based on the Series K589 BIS MPK

The structure of a processor on a single plate is depicted on Figure 60. The central processor, executed on a series K589 BIS, consists of a matrix of central processor elements (TsPE), a microprogram control unit (BMU) controlling the memory on a PPZU and some additional circuits with a moderate degree of integration. Arranged on the plate is a synchronous pulse generator (GSI) which forms pulses for the TsPE, BMU and other synchronous devices.

The arithmetic-logic device. The TsPE matrix with an accelerated transfer circuit (SUP) realizes arithmetic and logical operations, and also the register memory of the central processor. On the additional integrated circuits of series K155 are gathered the single-digit registers of expansion (RR) and overflow (RP), a trigger forbidding interruption (TrZP) and a "Stop" trigger. On the shift and transfer input of the TsPE matrix, to perform various operations through a 4-input multiplexor can be fed the RR contents, the largest and smallest digits of the data register (AS) and information from the FO output of the BIS BMU. To process eight interruption requests,

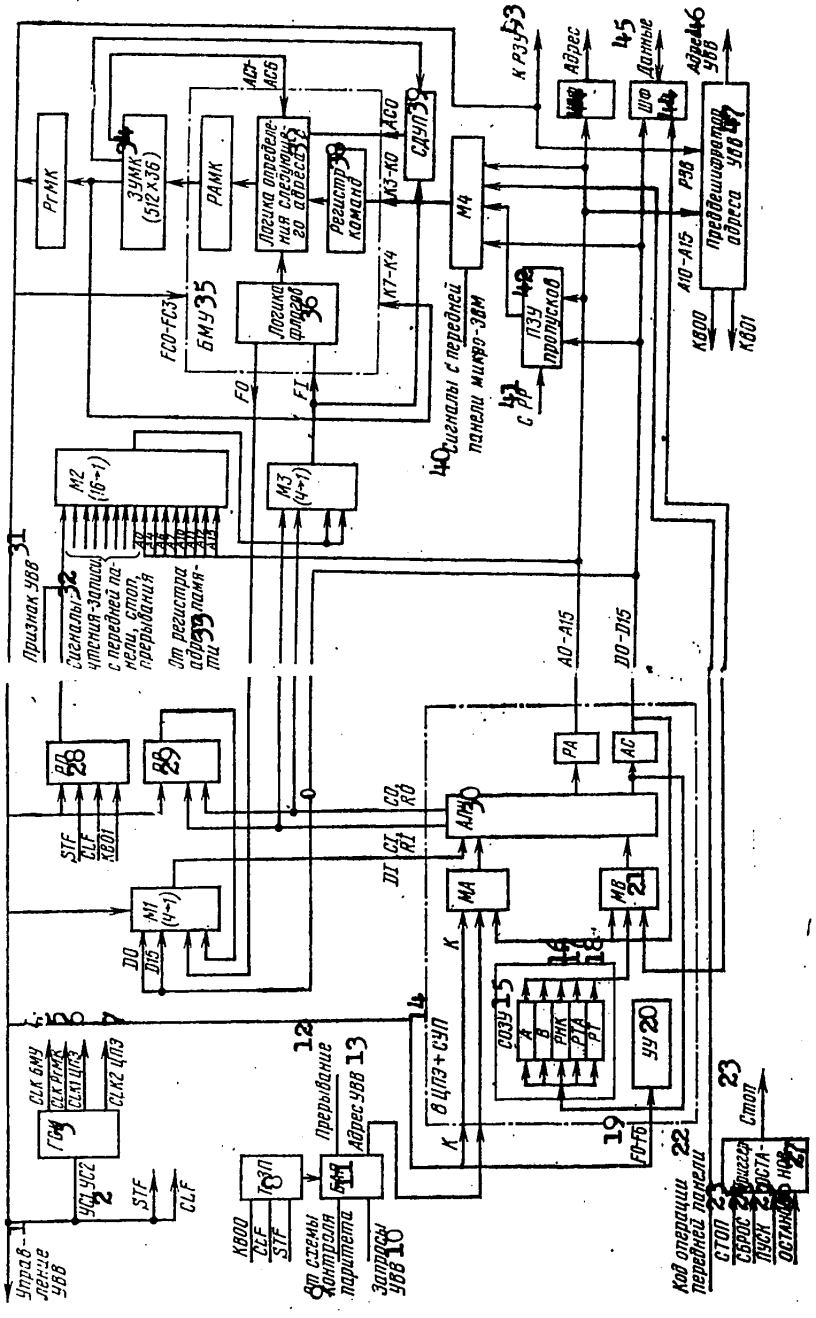

Figure 60. Processor structural circuit.

1 - UVV control
2 - US1, US2
3 - GSI
4 - CIK BMU
5 - CIK PrMK
6 - CIK1 TsPE
7 - CIK2 TsPE
8 - TrZP
9 - From parity monitoring circuit
10 - UVV requests
11 - BAL
12 - Interruption

Figure 60 Continued

13 - UVV address
14 - To TsPE + SUP
15 - SOZU
16 - RNK
17 - RTA
18 - RT
19 - F0 - F6
20 - UU
21 - MV
22 - Front panel operating code
23 - Stop
24 - Inquiry
25 - Start
26 - Halt
27 - Halt trigger
28 - RL
29 - RR
30 - ALU
31 - UVV sign
32 - Reading-recording signals
33 - From memory address register
34 - ZUMK
35 - BMU
36 - Flag logic
37 - Sign for determining following address
38 - Instruction register
39 - SDUP
40 - Requests from microcomputer front panel
41 - From RR
42 - PZU starts
43 - To PZU
44 - Decoder
45 - Data
46 - UVV address
47 - UVV address predecoder

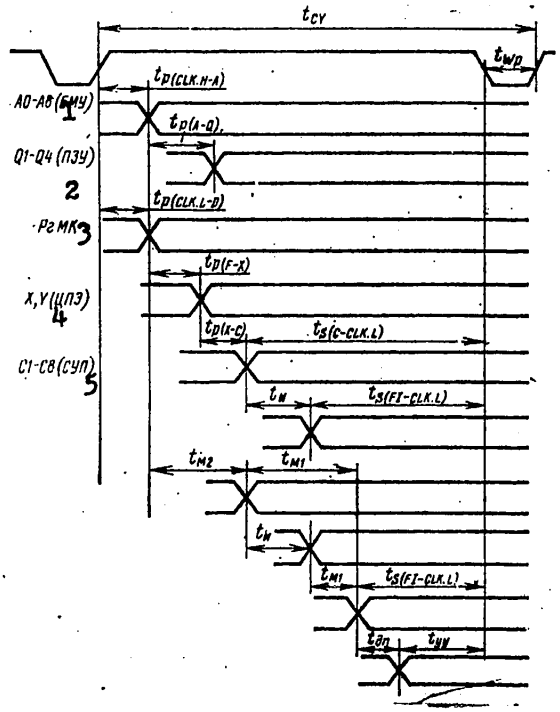

Figure 61. Time dependences for calculating a microinstruction cycle.

1 - (BMU)
2 - (PZU)
3 - RgMK
4 - (TsPE)
5 - (SUP)

on the plate is arranged the BIS of a priority interruption unit (BPP). The input and output data lines are combined into a line former in a single two-directional data line. The address line also emerges from the plate through line formers. To select one of the possible peripherals, on the plate are two K155ID4 circuits, forming the first decoder of the code of selection of the peripheral. All these additional circuits are necessary to realize complete compatibility of programs for the M-6000 computer and the described micro-computer.

To reduce the time required for execution of the register instructions a single PPZU circuit is used (organization 256 x 4) on eight address inputs, to which the instruction positions and signs to be analyzed are attached, and the information outputs serve for determination of the possible omission of the following microinstruction.

The control equipment includes a BIS BMU (K589IK01), a microprogram memory (ZUMK), a conveyer register (RgMK) and several multiplexors (M2-M4). The conveyer register is organized on D-triggers with recording of information on the front (K155IR1 microcircuits). The multiplexors are necessary for expansion of the functional possibilities of the BMU, and also to reduce the number of successively performed microinstructions acccomplishing the given instructions.

To perform conditional transitions on one of the signs not being formed during execution of the following microinstruction a 16-input multiplexor M2 serves. On its input arrive some digits of the microinstruction (for example, A0, A4, A6, etc) signals from the control panel, etc.

Information from that multiplexor can pass through through the 4-input multiplexor M3 to the input of signs and to the AC0 control input. That is done to increase the number of possible conditional transfers in the BMU. The 4-input multiplexor is necessary for passage to the input of the BMU signs of signals arising during execution of the following microinstruction. The multiplexor is included in the circuit because the delay of passage of the signal through the 16-input multiplexor is about 50 ns, and this involves a considerable increase of the cycle of execution of the microinstruction without formulation of the M2 multiplexor.

In all types of instructions of the M6000 mini-computer there [illegible] which determine the execution of several operations, for example digits 1-4 in request instructions, digits 6-7, 8-9, 7-9, and 13-15 in register instructions and digits 7-9 in the input-output instructions group. If it is taken into consideration that the BMU can perform conditional transfers with respect to a group of digits (for example, the BMU, JPX, JPR and JLL transfer functions), it is advisable to feed one of the enumerated group of digits on the K3 - K0 inputs through 8-input multiplexors. This makes it possible to considerably reduce the time required for execution of the instructions. Besides instruction digits onto the inputs K3 - K0 of the BMU through the multiplexors pass signals from the control panel which determine its working conditions during halting of execution of the program, and data from the PZU, necessary for analysis of the passages in the group of register instructions. To save equipment and the microinstruction memory, all transfers by group of digits are made through a four-digit register of instructions of the BMU, and so before the conditional transfer is accomplished for the group of digits using BMU transfer functions such as JPR, JLL, or JRL, it is necessary to record the values of the digits to be analyzed in the BMU instructions register by means of instruction JPX.

It should be noted that there is no special instructions register in the processor. The address instruction code, after it has been read in the accumulating data register (AS) and the memory address register (RA), which are in the TsPE matrix, is remembered according to the JPX instructions BMU instructions register and is stored there in the course of performance of the instruction, and in the RA is the effective address for return to the ROM for the operand.

In the register instructions and the input-output instructions the instruction read from the ROM is remembered in the RA, which is used later as a register of instructions. At the end of the performance of all instructions in the RA a new address is recorded, one which determines the position in the ROM of the following instruction.

Calculation of the cycle of execution of a microinstruction. The time dependences for calculation of the microinstruction cycle are presented on Figure 61. Two synchroseries, obtained from a single generator, serve for the synchronization of all circuits on the processor plate. The microinstruction length is calculated under the worst dynamic characteristics of the microcircuits in the temperature range of 10-70°C and a voltage of 5V±5%. To calculate the cycle for microinstruction execution, several very critical paths of passage of information were considered, among them the paths (and time respectively) of accomplishment of operations in the TsPE and of conditional transfers in the BMU.

At the moment of performance of a microinstruction by the front of the synchropulse, in the microinstructions register (TgMK) from the PZU is recorded a new microinstruction which which in the time $t_{p(CLK.L\cdot D)}$ appears on the PrMK outputs. After its arrival on the TsPE inputs F0 - F6 K0 - K1 in the time $t_{p(F-X)}$ equal to 52 ns, on the TsPE inputs X and Y appear signals for the accelerated transfer circuit which with the delay $t_{p(X-C)}$, equal to 20 ns, issues input transfer signals to all the TsPE circuits.

After the arrival of the input transfers on the TsPE inputs in the time $t_{S(C-CLK.L)}$ = 27 ns a new synchronous pulse t_{WP} with a length of at least 33 ns can be added. In that case the cycle time is

$$t_{CY} = t_{p(CLK.L\cdot D)} + t_{p(F\cdot X)} + t_{p(X\cdot C)} + t_{S(C\cdot CLK.L)} + t_{WP} =$$
$$= 35 + 52 + 20 + 27 + 33 = 167 \text{ нс.}$$

When the transfer signal is used in the logic of BMU signs the signal of the output transfer must go through the MZ multiplexor which gives the delay t_{MZ} - 22 ns, and the following synchronous pulse on the BMU can can be fed during the time of installation of the sign $t_{S(FI-CLK.L)}$ = 15 ns.

In that case the length of the cycle is

$$t_{CY} = t_{P(CLK.L\cdot D)} + t_{P(F\cdot X)} + t_{P(X\cdot C)} + t_{M3} + t_{S(FI\cdot CLK.L)} +$$
$$+ t_{WP} = 35 + 52 + 20 + 22 + 15 + 33 = 177 \text{ нс.}$$

The length of accomplishment of a microinstruction during passage of a signal through a 16-input multiplexor M2 under the condition that on the inputs of that multiplexor the information has been established in advance, is equal to

$$t_{CY}=t_{P\,(CLK.L.D)}+t_{M2}+t_{\text{и}}+t_{M3}+t_{M3}+t_{S\,(FI\text{-}CLK.L)}+t_{\text{ур}},$$

where t_{M2} is the delay of the signal during passage through the 16-input multiplexor, equal to 52 ns; $t_{\text{и}}$ = 22 ns is the information delay in the invertor which serves for transfer into the prescribed cell of the microprogram memory for both the zero and the unit value of the level.

The cycle time is

$$t_{CY}=35+52+22+15+33=179 \text{ нс}.$$

The program control unit has a limited number of possible conditional transfers. To increase the number and types of conditional transfers a circuit of additional conditional transfer was developed which makes it possible to add a transfer sign to the BMU ACO input. The sign for the additional transfer is selected by the multiplexor M2 and through microcircuits which have the delays t_{M3} = 22 ns and t_{DP} = 22 ns respectively and will fall on the input ACO. The time for establishment of information on the AG input t_{yy} = 10 ns.

The cycle time during additional conditional transfer is

$$t_{CY}=t_{P\,(CLK.L\text{-}D)}+t_{M2}+t_{M3}+t_{\text{доп}}+t_{yy}+t_{\text{и}}=$$

$$=35+52+22+22+10+33=174 \text{ нс}.$$

It is evident from the presented calculations that the minimum cycle time which will assure all possible functions of BMU transfers is 179 ns.

The conveyer microinstructions register makes it possible to reduce the cycle time by the time

$$t_{CY}=t_{P\,(CLK.H\text{-}A)}+t_{P\,(A-Q)}-t_{P\,(CLK.L\text{-}D)}=$$

$$=44+70-35=79 \text{ нс},$$

where $t_{p(CLK.H\text{-}\overset{A}{a})}$ is the time of establishment of an address in the BMU.

Used for the construction of a synchropulse generator are a 10 MHz quartz generator and a division circuit which assures a period of synchropulses of 200 ns and and a synchropulse length of 50 ns.

Format of microinstructions. In the construction of a central processor on the basis of series K589 BIS's the minimum number of digits in a microinstruction is 18, of which the seven digits F0 - F6 give the TsPE microinstruction, the four digits FC0 - FC3 control the logic of BMU features and the 7 digits AC0 - AC6 determine the function for the formation of the following microinstruction address. Additional microinstruction digits are required for the construction of a specific processor. The microinstruction format used in the processor emulating the system of M6000 mini-computer instructions uses 36 digits.

Digit 1 gives the value of the mask K.

Digits 2-8 determine the TsPE microinstructions.

Digits 8 and 9 control the multiplexor on the TsPE matrix input.

Digits 11 and 12 control the passage of synchronous pulses into the TsPE, permitting the accomplishment of conditional synchronization. Digit 11 (US1) permits the passage of a synchronous pulse to the six larger digits of the TsPE matrix; digit 12 (US2) to the 10 smaller digits. Thanks to this separation of the synchronous pulses the formation of the zero and following ROM pages during execution of address instructions is simplified. For example, during formation of the following page an instruction is carried out for transfer of the contained instruction number register (RNK) into the address register (RA), but at UC1 = 1 and UC2 = 0 the change of the smaller ten digits of the RA is forbidden, and the value of the largest digits of the RNK are re-recorded in the RA. At UC1 = UC2 = 0 it is possible to verify the content of the registers without changing them or in necessary cases to increase the length of microinstruction execution. Increase of the length of the cycle of performance of microinstructions is necessary in the preparation of the sign of overflow [illegible] of the operation of addition, which is carried out by analysis of the transfer into the largest (sign) digit and the transfer from the largest digit.

Digit 13 allows return to the storage device.

Digit 14 allows in input-output instructions the passage of information and control signals to the interface plates, strobing the decoder of the address of the input-output device (UVV).

Digits 15 and 16 control the work of the allowance and overflow registers, allowing in necessary cases change of its value in accordance with the result of execution of the instruction.

Digit 17 determines the recording or reading of information during reference to the store. This digit also controls the direction of passage of information in input-output instructions.

Digits 18-21 control the multiplexor M2, allowing the passage of signals on one of 16 inputs, and the same digits in input-outpot instructions control the work of peripherals.

Digits 22-24 control multiplexors M3 and M4 during conditional transfers. The control of different multiplexors from single microinstruction digits is possible since operations with conditional transfers according to a single feature and conditional transfers according to an operation code are separated in time.

Digits 25-28 control the logic of signs in the BMU.

Digits 29-35 control the logic of determination of the following microinstruction address in the BMU.

Digit 36 increases the number of possible BMU conditional transfers according to one feature, allowing passage through the circuit of an additional conditional transfer (SDUP) on the BMU ACO input.

Experience in writing microprograms has shown that the use of SDUP facilitates the compilation of an algorithm of microprograms and simplifies the addressing of the control store.

5.2. Controller for a Magnetic Disk Store (NGMD)

A floppy-disk store is intended for the input, storage and output of information and can be used as a peripheral storage device for micro- and mini-computers, assuring the storage of over 512K bytes of information. In the creation of a controller algorithms for the work of NGMD's of the type of "Elektronika GMD-70" were taken as a basis. The microprograms of the controller accomplish the following memory input-output instructions: recording in the buffer memory, reading from the buffer memory, recording of a sector, reading a sector, reading the register of the state and errors and recording of a sector with marking.

Figure 62 shows a controller for magnetic disk stores, made with series K589 BIS microporcessor sets (MPK).

The controller includes the following units: a BMU, four TsPE's, five microprograms, a buffer store, a store regimes former, a data separation unit, a multiplexor, input valves, output valves, an address register, and a buffer store address register. The BMU, TsPE and microprogram store constitute an information processing device. The microinstruction performance cycle selected is 400 ns, which has permitted eliminating the sccelerated transfer circuit.

A multiplexor is used to verify the external input signals. The multiplexor is controlled by a 3-digit selection code which gives on the ACO outlet either the smaller digit of the transfer function code or one of the seven external signals: the buffer store output (VP), the overflow of the buffer store address register (BSP), the the generated synchronous signal (VS), the produced data (VD), the passed synchronous signal (PS), the output of transfer from the smaller digit of the TsPE file (SO), the output of the larger digit of the buffer store address register (A8). The signals VS, VD and PS are produced by the data division unit, read from the floppy magnetic disk.

The microprogram store is made of four programmable permanent storage units (PPZU) organized into a file of 512 words of 32 digits each. The controller microinstruction is divided into the following controlling fields:

-- a field of BMU transfer functions (7 digits);

-- a field of control of the multiplexor output (3 digits);

-- a field of control of decoder inputs (3 digits);

-- a field of control of the multiplexor output (3 digits);

-- a field of control of the logic of signs (4 digits);

-- a field of the mask or data (8 digits).

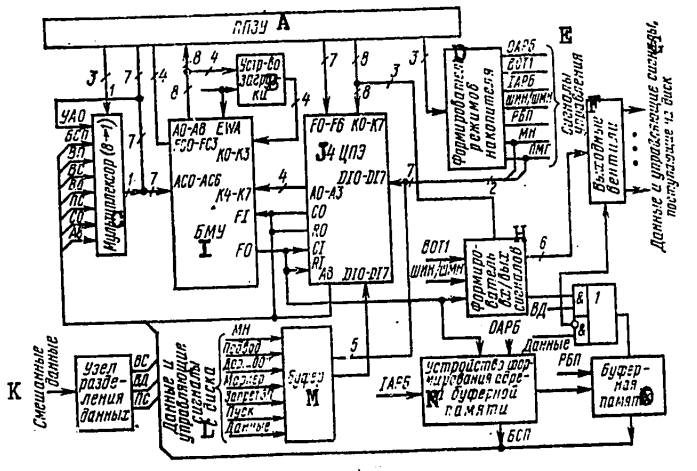

Figure 62. Controller structural circuit.

A - PPZU
B - Loading device
C - Multiplexor
D - Stores regime former
E - Control signals
F - Output valves
G - Data and control signals arriving on disk
H - Input signals former
I - BMU
J - 4 TsPE
K - Mixer data
L - Data and control signals from desk
M - Buffer
N - Buffer store address former
O - Buffer store

2174
CSO: 8144/1086

KR1802 SERIES LARGE-SCALE INTEGRATED CIRCUIT MICROPROCESSOR SET

Moscow MIKROPROTSESSORNYYE KOMPLEKTY POVYSHENNOGO BYSTRODEYSTVIYA in Russian 1981 (signed to press 3 Nov 81) pp 133-157

[Chapter 6 from book "Enhanced-Speed Microprocessor Set" by Aleksandr Ivanovich Berezenko, Lev Nikolayevich Koryagin and Artashes Rubenovich Nazar'yan, Massovaya Biblioteka Inzhenera: Elektronika, Izdatel'stvo "Radio i svyaz'", 25,000 copies, 168 pages]

[Text] 6.1. Arithmetic Device (AU)

The arithmetic device represents an enlargeable section of a data processing device and is intended for performance of the following operations: arithmetic, addition and subtraction in a supplementary code; logical operations of conjunction, disjunction, inversion and additions in modulo 2; arithmetic, logical and cyclic shifts to the right and left per digit. When those operations have been executed one can carry out numerous operations of masking the contents of the register of expansion of individual digits of input data.

According to the result of the operations criteria of equality to zero are prepared and a criterion of overflow (in operations of addition, subtraction and of shift to the left). When several BIS ALU are combined it is possible to produce successive and accelerated transfer, operations of byte processing, a broad set of shift operations, including expanded shifts, that is, shifts of a double-length word together with the expansion register contents without additional external circuits with the production of signs of the result only in selected crystals.

The following devices are included in an arithmetic device (Fig 63): a parallel arithmetic logical device (ALU), a circuit to shift the result of the ALU (SALU), an expansion register (RR), a circuit for the shift and loading of the ALU result into the RR; the circuit for formation of the sign of zero of the result of the operation; registers A and B; output circuits; the arithmetic device operation decoder; the arithmetic device modification decoder.

The digits of the microinstructions F0 - F3 are determined by operation of the ALU with data arriving on its input. Those operations include addition and subtraction of codes and fields, and logical transfers. The digits of microinstructions F4 - F7 determine the operations of ALU modification. Those operations include:

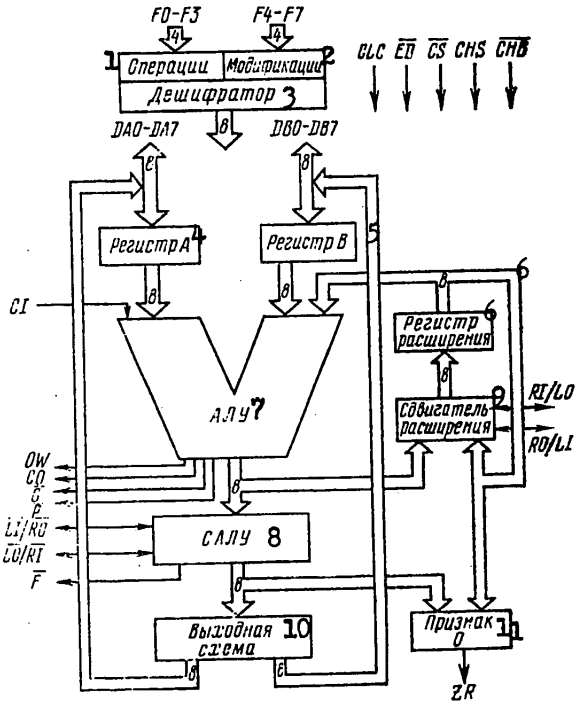

Figure 63. Arithmetic device structural circuit

1 - Operations
2 - Modification
3 - Decoder
4 - Register A
5 - Register B
6 - Expansion register
7 - Arithmetic-logical device (ALU)
8 - SALU
9 - Expansion shifter
10 - Sign

-- selection of operands on the input, that is, operation with register B or the expansion register;

--expansion of the masking operations;

-- different shift operations.

The two-directional lines DA0 - DA7 and DB0 - DB7 with their steady states are intended for the organization of information reception over channels A and B and issuance of the results to those channels at the signal $\overline{ED} \cdot \overline{CS}$. The register of operands A and B serves for buffering information received over channels A and B.

The expansion register is used for storage of the mask used for separation of bits, the storage of one of the operands of the ALU operator and work with the double-length words. The expansion register is effectively used in processors performing operations with a floating point (addition, multiplication and division).

The arithmetic-logical device (ALU) is intended for the performance of arithmetic and logical operations arriving on the ALU inputs.

6.2. Arithmetic Expander (AR)

The BIS AR is intended for the realization on the basis of it of devices accomplishing arithmetic, logical or cyclic shifts, expanded to the left and right, in a single cycle on an arbitrary number of digits, and also retrieval of the number of the left single bit. The AR makes it possible in several cycles to make shifts of information with a digit capacity of more than 16 (for example, 32, 48, etc).

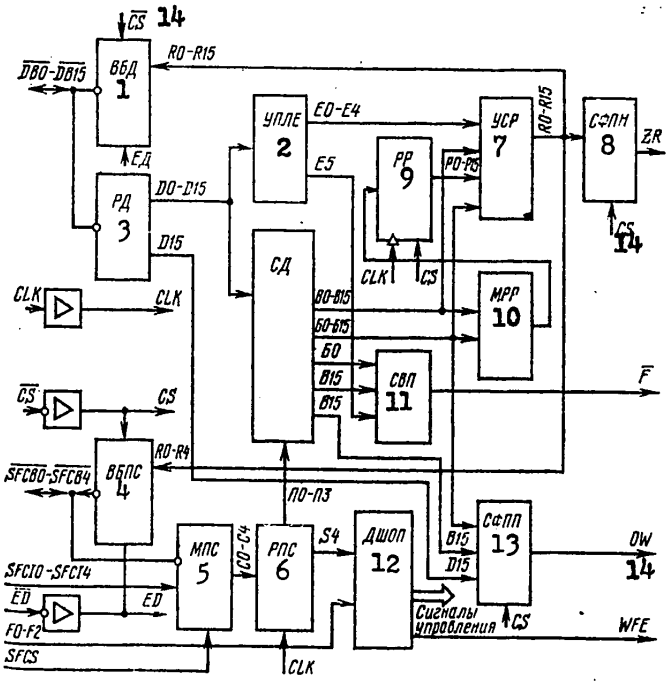

Figure 64. Arithmetic expander structural circuit.

1 - VBD	8 - SFPN
2 - UPLE	9 - RR
3 - RD	10 - MRR
4 - VBLS	11 - SVP
5 - MLS	12 - DShOP
6 - PLS	13 - SFPP
7 - USR	14 - Control signals

The BIS AR (Fig 64) includes the following devices: an information register (RD), an information shifter (SD), an expansion register multiplexor (RR), a left unit retrieval unit (UPLYe), a result splicing unit ((USR), a zero sign formation circuit ((SFPA), a sign issuance circuit (SVP), an overflow sign formation circuit (SFPP), a multiplexor of the parameter shift (MPS), a register of the parameter shift (RPS), an output data buffer (UBD), an output buffer of the parameter shift (VBPS) and a microinstruction operation code decoder (DShOP).

The information register and the RPS serve for the storage of information and the shift parameter at the moment the result is issued, that is, the two-directional main lines are uncoupled. The CD serves for shift of information D, which is determined by the binary code of the shift parameter. P0 - P3. For implementation of arithmetic shifts to the right the circuit has the possibility of multiplying the sign. CD always performs left shifts. Right shifts are obtained through left indirectly on the basis of the part that the right shift is a supplementation of the left. During shift to the right the result is removed with part of the advanced

digits B0 - B15, and the shift parameter P0 - P3 is fed in the supplementary code. In that case the larger digit of the shift paramter S4 is equal to unity.

The expansion register multiplexor passes the advanced (falling out) digits to the RR. During shift to the left this is the information B0 - B15, and during shift to the right, V0 - V15. RR serves for the storage of digits falling out during shifts. The presence of RR permits by macroprograms expanding the digit capacity of the shifted word.

The left unit retrieval unit serves for determination of the digit number of the first unit on the left (starting from the largest digit, 15). The result of the retrieval is issued in a 4-digit code to the USR. In addition, the UPLYe will issue to the SVP the sign of absence of 1 on line E5. The USR serves for formation of the result as a formation of the modification of the shift (logical, cyclic, etc) and represents a multiplexor which assures the operation of logical addition. The USR also issues to the UPLYe the result of retrieval of the left unit on the line R0 - R4.

The output data buffer issues the result of operation R0-R15 to the two-directional main line of information DB0-DB15. The VBPS issues the result of retrieval of the left unit to the two-directional shift parameter SPCB0 - SPCB4.

The shift parameter multiplexor serves for issuance to the RPS of the shift parameter or from the main line SFCB or from the line SFC1 as a function of the control signal of selection of the SFCS parameter. The SFPN issues a signal of equality to zero of all the digits R0 - R15 which arrive from the USR. The SVP issues the last of the dropped out digits during shifts on the sign of absence of 1 in the input information during operations of the retrieval of the left 1. The SFPP forms the sign of overflow during shifts to the left if even one dropped-out digit during arithmetic shift is not equal to the largest digit of the information B0 - B15. In addition, the SFPP issues the sign of input information on line D15 during retrieval of the left 1 and determines the loss of units during logical, expanded and cyclic shifts to the left. The DShOP serves for the formation of control signals corresponding to the code of operation F0 - F2 and the largest digit of the shift parameter S4.

Let us consider the work of the AR during shift operations. When 1 is fed to the CLK information input the information which arrives from the two-directional lines is recorded in the RD. Simultaneously with that the code of shift from the two-directional lines SFCB when 1 is on the SFCS input or from the SFC1 lines when 0 is on the input SFCS is recorded on the RFS. During shift to the right the digit (largest) of the shift S4 code is equal to 0, and the digits P0 - Pe are fed in a direct code. During shift to the right S4 = 1, and the digits P0 - Pe are fed in a supplementary code.

During expanded shift, information B or C is simultaneously issued with the information recorded in the RR. During all shifts information B or C is fed to the RR input. In the presence of the signal CS on the front of the synchronous pulse CLK (transfer from 0 and 1), B or C is recorded on the RR.

In addition, the result of the operation R and O of circuit SFPN is analyzed, the last dropped-out digit (B0 during shift to the left or V15 during shift to to the right) is issued on the output F, and the advanced digits B are analyzed for their simultaneous equality to digit V15 of the SFPP ciccuit.

6.3. General Purpose Registers (RON)

The RON is a two-address general purpose memory which has two 4-digit channels for information reception and issuance. The microcircuit is intended for realization of the SOZU of processors and multi-address OZU's.

The BIS RON structural circuit is presented on Figure 65. The BIS RON consists of a matrix of 16 x 4 bits which contains 16 4-digit registers, two decoders DSh1 and DSh2 to select the necessary register on channels A and B respectively, eight reading amplifiers (US) with three steady states on the output and eight recording amplifiers (UZ).

The reading and recording amplifier of each digit of the BIS RON matrix works on a single digit of the corresponding channel.

Channel selection. By expanding the volume of information of the BIS RON matrix with channels A and B the inputs ECA and ECB are controlled. In the presence of 0 on the ECA and ECB inputs the volume of information with channel A ann B respectivey is expanded.

Control of regimes. The registers RA and RB determine the regime of reading information from the BIS RON matrix to channel A or B. In the presence of 0 on the RA and RB inputs reading from channel A or B respectively is expanded.

The inputs WA and WB determine the regime of recording information on the BIS RON matrix from channels A and B. In the presence of 0 on the input WA the recording of information is allowed from channel A and in that case the reading amplifier output of channel A must be closed (the third state) (on the input Ra in 1). In the presence of 0 on the outputs WA and WB the recording of information is allowed from both channels. During recording from both channels when there is s single address the result is not determined.

The BIS RON matrix register is selected by the decoders Dshl and Dsh2.

6.4. Information Exchange BIS

The information exchange (OI) BIS is a 4-address memory which has four 4-digit registers for information reception and issuance. The BIS OI is intended for use as an SOZU, with the possibility of organizing on one of the registers of a reader with increase of the contents by 1.

Figure 66 presents a structural circuit of the information exchange BIS. The BIS OI consists of the three 4-digit registers RG1, RG2 and RG3 realized on triggers of the "latch" type, a 4-digit double reader (RG0) with the possibility of parallel loading, realized on D-triggers of the MS type with information recording on the front of the signal, four decoders (DSha, DShB, DShC and DShX) for the selection of necessary registers on channels A, B, C and X respectively of the control units, four multiplexors (M0, M1, M2 and M3) for selection of information for recording in the registers, a comparison circuit producing the sign of equality of the content of the RG0 register and that of the RG1 register, and a reception unit--the issuance of information from channels A, B, C and X. The register RG0 can work in the regime of a counter with addition to the contained 1. The BIS OI working regime is

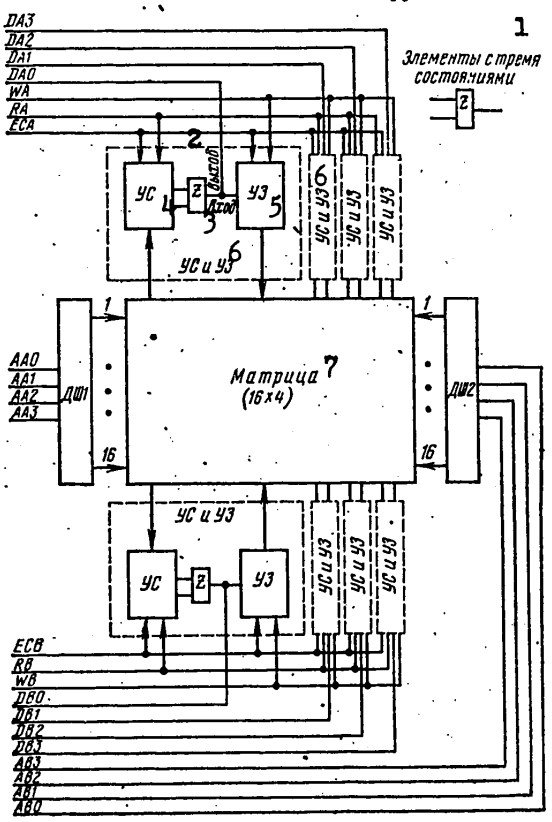

Figure 65. RON structural circuiy.

1 - Elements with three staates
2 - Output
3 - Input
4 - US
5 - UZ
6 - US and UZ
7 - Matrix

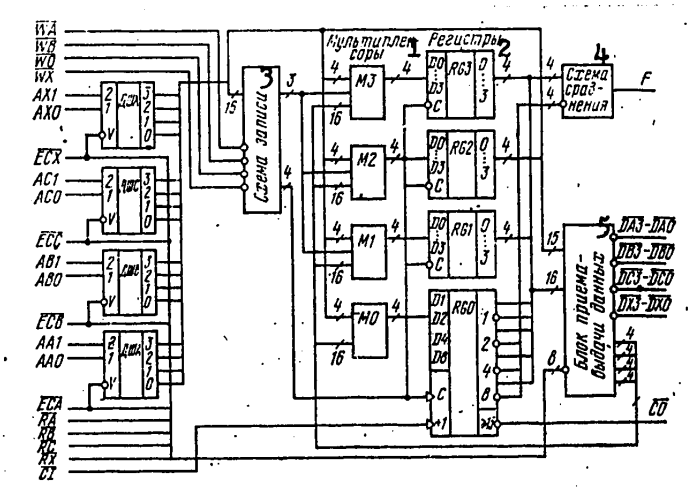

Figure 66. BIS OI structural circuit.

1 - Multiplexors
2 - Resistors
3 - Recording circuit
4 - Comparison circuit
5 - Data reception-issuance unit

synchronized by the feeding of control signals to the inputs of allowed information exchange, the inputs of allowed recording, reading and control of the counting. The working regime on each channel is given independently of the working regime of the other channels.

Channel selection. The inputs ECA, ECB, ECC and ECX are controlled by allowing exchange of information with the channels A, B, C and X. When 0 is present on the inputs ECA, ECB, ECC and ECX, exchange of information of the selected register is allowed with the channels A, B, C and X respectively.

Regime control. The regime of reading or recording can be set only when information exchange is allowed with the selected channel, which is determined by the inputs ECA, ECB, ECC and ECX. The inputs RA, RB, RC and RX determine the regime of reading information from the registers of the BIS OI from the channels A, B, C and X. When 0 is on the input RX, reading of the contents of the selected register of the matrix from channel X is allowed. When 0 is on the inputs RA, RB, RC and RX, reading of the contents of the selected register from channel A, B, C and X is allowed.

Inputs WA, WB, WC and WX determine the the regime of recording information from channels A, B, C and X in selected BIS OI registers. When 0 is on the inputs WA, WB, WC and WX the recording of information from channels A, B, C and X in selected registers is allowed.

In both recording and reading regimes the necessary BIS OI register is selected by the decoders DCA, DCB, DCC and DCX by assigning a binary code to the address inputs. The content of the register RGO is increased when a positive voltage drop on the CI input. For correct performance of the counting operation, during the feeding of the positive front of the signal on the CI input it is not permitted to feed even one of the code address lines determining the register address under the condition of the presence of allowance of exchange and a signal of recording from that line.

It follows from the description of the working regimes that a direct transfer of information can be made from one main line to another through any register except the RGO retister. To do that, the control signals of the main line of the source of information should be so set that it produces a recording of the information from the main line of the source in one of the registers registers, and the control signals of the main line of the receiver of information be set in the condition of reading on the main line-receiver from that regiser in which the recording is made of information from the main line of the source.

The main lines DA, DB, and DC are intended for work on short lines of communication, for example, information lines within a plate; the main line DX can work on long matched lines of communications.

If a recording is made in any of the registers of information one of the main lines and simultaneously with that code on the address lines of main lines determines the same register and recording regime, then in the register is recorded the result of a step-by-step cascaded OR operation with the information on those main lines.

6.5 Interface BIS

The interface BIS is intended for use in single- or multi-processor computer systems as a circuit for the control of information exchange over a combined main line with asynchronous disciplinary exchange. The BIS is oriented toward joint work with the BIS OI, and also can be used with other integrated circuits assuring buffering of the reception and issuance of information.

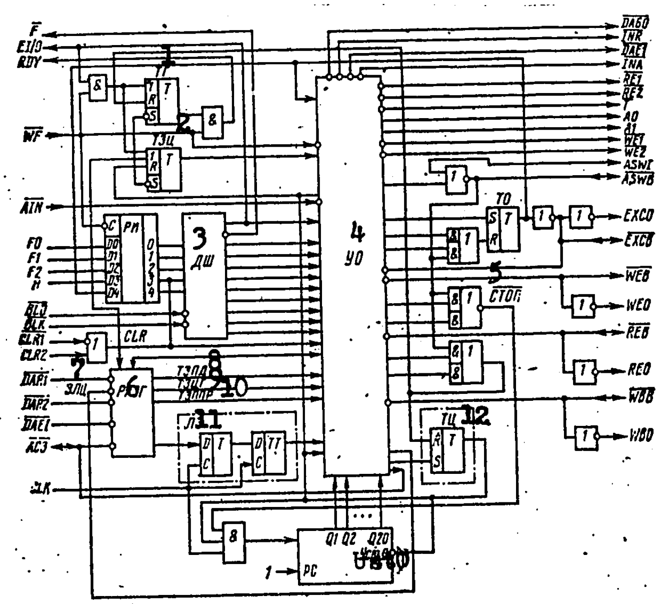

Figure 67. BIS I structural circuit.

1 - TG
2 - TZTs
3 - DSh
4 - UO
5 - STOP
6 - LTs
7 - RKhZG
8 - TZTsG
9 - TZTsG
10 - TZPPR
11 - LZ
12 - TTs
13 - USZO

The BIS interface structural circuit is presented on Figure 67. The principal devices of the structural circuit are: an instructions register (RI), an instructions decoder (DSh), a readiness trigger (TG), a cycle request trigger (TZTs), a digital delay line (LZ), a shift register (RS), an exchange device (UO), an exchange trigger (TO), a cycle trigger (TTs), a main processor trequests storage register (RKhZG).

The 5-digit register of instructions is realized on D-triggers of the "latch" type. The information is recorded in the RI at $\overline{WF}$ = 0 and stored at $\overline{WF}$ = 1. The DSh is a combination circuit which makes a preliminary decoding of the instruction. The

The TG is a trigger which signals regarding conclusion of the BIS I working cycle, the TZTs is set in 1 if in the TTs 0 is set during the recording of a new instruction in RI, LZ serves for the exclusion of "races" in order to have unequivocal reaction of the circuit to all arriving inquiries.

The shift register for the formation of a temporary work diagram of the UO circuit receives and analyzes the input signals, forms temporary diagrams of signals on the outputs of the circuit in accordance with the given instructions. The RKhZR receives and stores inquiries on the main line for the main processor. It consists of three triggers: TZPP, TZTsG and TZPP". When even one of the triggers is set in 1 the installation of the other triggers in 1 is blocked.

6.6. Serial Multiplier

The BIS UMP is intended for the construction of devices for multiplication and division of binary codes and devices for the multiplication of numbers represented in a supplementary code. Operations of multiplication are performed on two 8-digit operands. The obtained result has 16 digits. The operation of division is carried out on a 16-digit code of the dividend and an 8-digit code of the divisor with the result obtained in the form of an 8-digit quotient and an 8-digit remainder.

To obtain devices with large digit capacity (a multiple of 8) several BIS's are used. The presence of a result determining the largest crystal (CHS) and a result of crystal selection (CS) permits during increase conducting operations without introducing additional circuits with the production of definite features of the result.

The reception of initial data and the issuance of the result are done over the same two-directional lines and this makes it possible to economize on the BIS outlets.

The UMP (Figure 68) includes the following devices: registers (R1, R2, R3), multiplexors (M1, M2. M3), a summator (CM), a control unit (UU), an output buffer to issue the result over the main line (VBA), an output buffer to issue the result over the main line (VBB), a circuit to issue the digits being analyzed (SVAR), a circuit to issue signs (SVP), and an instruction register (RI).

The 8-digit RI register serves to receive the multiplier in multiplication operations and and of the smaller word of the dividend during division. In the process of performing those operations the smaller digits of the product and quotient are formed in the R1. The RI register consists of two single-cycle registers R1' and R1". In the single-cycle 8-digit register R2 the multiplicand in operations of multiplication and the divisor in division are stored. The two-cycle 10-digit register R3 serves for recording the largest word of the dividend during division. In the process of multiplication and division the regular partial product and partial remainder respectively are recorded. After the operation is completed the largest digits of the product during multiplication are formed during multiplication and the remainder during division.

The multiplexor M1 assures reception of the operand over the main line and recording of it in R1 during initiation of the operation, and also shift of the contents of R1 by two places to the right (in the direction of the smallest digits) during multiplication and one place to the left (in the direction of the largest digits) during division. M2 assures the feeding on input A of the summator of a direct code of the

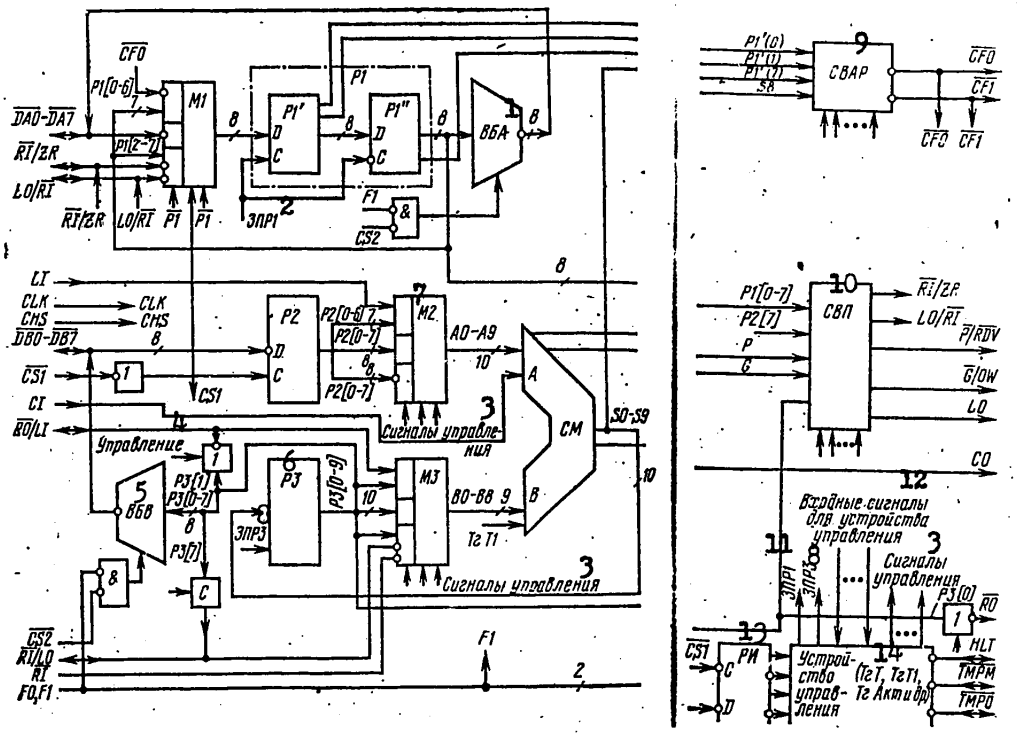

Figure 68. UMP structural circuit.

1 - VBA
2 - ZLR1
3 - Control signals
4 - Control
5 - BVB
6 - PZ
7 - MZ
8 - ZPR3
9 - SVAR
10 - SVL
11 - ZPRL
12 - Controls input signals
13 - R1
14 - TgT, TgT1, Tg

R2 contents with shift of the place to the left *in operations of multiplication), an inverse code of the R2 contents and in yhe process of realizing the algorithms for multiplication and division. Me serves for connection to input B of the summator of the R3 contents with shift of two places to the right (multiplication), with a shift of one place to the left (division) and 0.

The summator is intended for calculation of partial products and correction of the results during multiplication, calculation of successive remainders on the obtaining of successive partial bits during division and recovery of the final remainder. The control device produces in a certain sequence the signals needed for reception of the operands and initiation of the operation, realization of the algorithm of multiplication and division and issuance of the results in codes of the reading operation. The VBA and VBV serve for the issuance to DA and DB of the results from registers R1 and R3 respectively.

The circuits for issuance of the digits to be analyzed serve for issuance of the digits to be analyzed during multiplication and division in the BIS which is active at the given moment, and for reception of the digits to be analyzed by all the remaining circuits. The SVP serves for issuance of displaced digits, different signs of the result and signals of accelerated transfer. The two-digit instruction register reppares the operation code during execution. The operations code is recorded in the RI at $\overline{CSI}$ - 0.

The UMP BIS performs the following operations: multiplication of 8-digit integers presented in a supplementary code, multiplication of 8-digit code, division of codes, loading of the largest word of the dividend and reading of the results.

The first four operations are initiated by the signal CS1 and are given by a 2-digit code determined by signals on the outputs F0 and F1. The performance of those operations is synchronized by the synchronous pulse CLK. Reading of the result was initiated by the signal CS2. In the presence of the corresponding code on the outputs F0 and F1, reading of the contents of registers R1 and R3 is allowed. The results are stored on registers R1 and R3 until unloaded into the UMP BIS by a new operation on CS1, that is, they can be read many times.

6.7. Programmable Adapter of a Serial Interface (PAPI)

The PAPI BIS belongs to the class of programmable peripheral circuits and is functionally oriented toward the execution of parallel-serial and serial-parallel transformations. The functions of the PAPI are programmable and the possibility is envisaged of combining several PAPI BIS to process the transfer of more than 8 bits. The PAPI characteristics combine the possibility of its use for the construction of systems of information transformation on the main line-modular principle. The PAPI is intended for use in systems which direct transformation of parallel-serial information, in particular, disk stores, disciplinary systems, data transmission and reception systems, etc, is necessary.

The principal units of the PAPI structural circuit are: a control unit, an Information reception unit and a data transmission unit.

6.8. 8x8 Multiplier (UM)

The BIS UM is intended for the construction of high-speed multipliers of any digit capacity. The digit capacity of processed words is enhanced by means of additional circuits of summation and multipliers. In that case, to obtain the product of two N-digit words, K^2 UM BIS are necessary, where K is a whole number equal to or greater than N/8. The multiplication time during this is increased by the time of summation of the partial product. A 4-digit summator can be effectively used for the multiplication of multi-digit words (at $K > 2$) and for the summation of partial products (see #6.11).

Figure 69 presents a structural circuit of a multiplier. The microcircuit includes 8-digit registers of the multiplicand and multiplier, a multiplication unit, a 16-digit register of the product and an output buffer cascade. The outputs TCX and TCY permit multiplication on a number with a sign represented by an additional code, on numbers without sign or mixed, both whole and smaller than unity, and obtaining a product in an additional code. For example, for whole numbers the values of the multipliers and product are determined in the following manner:

$$X=(\overline{TCX}-TCX)\cdot X7\cdot 2^7+\sum_{l=0}^{6}X_l\cdot 2^l,$$

$$Y=(\overline{TCY}-TCY)\cdot Y7\cdot 2^7+\sum_{l=0}^{6}Y_l\cdot 2^l,$$

$$P=X\cdot Y=[1-2(TCX\cdot X7\oplus TCY\cdot Y7)]\,P15\cdot 2^{15}+$$
$$+\sum_{l=0}^{14}P_l\cdot 2^l,$$

where the sign O designates summation in modulo 2.

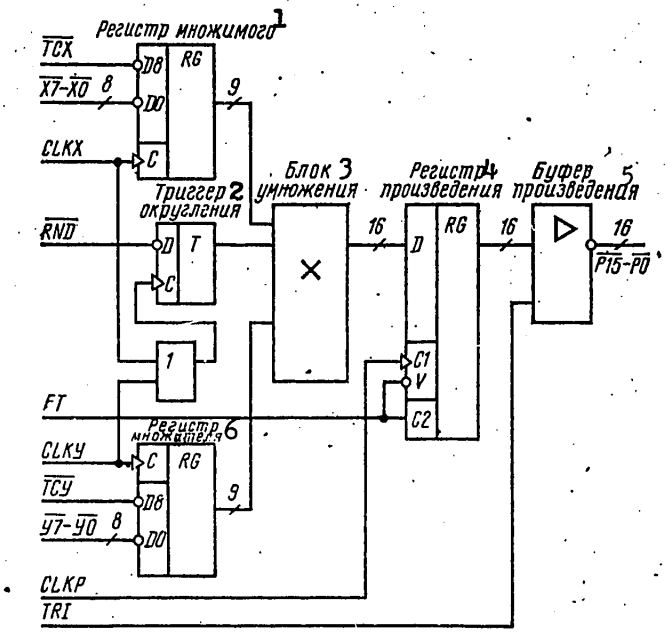

Figure 69. UM 8x8 structural circuit.

1 - Multiplicand register
2 - Rounding trigger
3 - Multiplication unit
4 - Product register
5 - Product
6 - Multiplier register

The sign of the product P15 is considered positive or negative in accordance with the general rule for obtaining the sign of the product as a function of the signs of the factors, in which case if the sign of the product is negative then the product is obtained in an additional code.

The input of rounding RND permits rounding the product by adding unity to the digit P6 of the product. In that case $P_{RND} = P + RND \cdot 2^6$ for whole numbers. Rounding the product is accomplished in the process of multiplication and does not increase the

total multiplication time. During multiplication of numbers smaller than unity the values of the multipliers and product are determined with the formulas:

$$X=(\overline{TCX}-TCX)\cdot X7\cdot 2^{0}+\sum_{i=1}^{7}X_{7-i}\cdot 2^{-i},$$

$$Y=(\overline{TCY}-TCY)\cdot Y7\cdot 2^{0}+\sum_{i=1}^{7}Y_{7-i}2^{-i},$$

$$P=X\cdot Y=[1-2(TCX\cdot X7\oplus TCY\cdot Y7)]\times$$

$$\times P15\cdot 2^{1}+\sum_{i=0}^{14}\cdot P_{14-i}\cdot 2^{-i},\quad P_{окр}=P+RND\cdot 2^{-8}.$$

Inputs CLKX, CLKY and CLKP are controlling and serve for the recording of operands and products in the corresponding registers. Upon the signal TRI, which arrives on the input of control of the buffer output cascade, the product is issued. The presence of a product register permits assuring a conveyer working regime of the multiplier, which can be regarded as a stage of a conveyer system.

The control input FT = 1 blocks the D-trigger of the product register, which becomes potential and the information from the register inputs constantly passes to the outputs (the register as it were is cut off, "transparent').

6.9. 16x16 Multiplier

The 16x16 multiplier represents a high-speed combination device for multiplication of 16-digit operands. Each of the operands can be either a code (a number without a sign) or a number with a sign. In the latter case such an operand is presented in an additional code. The numbers can be both whole numbers and smaller than 1. On the output of the multiplier a product of double precision is prepared--32 digits, which can be rounded of to 16 digits (including the sign digit). During multiplication of numbers in an additional code--during actions on numbers with signs the possibility of attaching a sign of a product to the smallest part of the product is envisaged.

The BIS UM can be used for high-speed processors of digital information processing, which realize the BPF alforithm, digital filtration, etc, and also in specialized and universal digital computers.

The presence of registers of multipliers and product and the control of "transparency" of the latter make possible more flexible use of the multiplier in conveyer systems. The application on the output of the multiplier of buffer circuits,(circuits with three states)permits combining the outputs of several multipliers into a single line of the product (for example, during reduction of the multiplication time of files of numbers by multiplexing).

The structural circuit of the BIS is presented on Figure 70. The device includes a multiplicand register, a multiplier register (register U), a rounding trigger, a multiplication unit, a shifter, a register of the largest and smallest parts of the product, output buffer cascades and the largest and smallest parts of the product.

Registers X and Y are made of D-triggers with a single-cycle input. Recordings are made on them on the front of the signals CLKX and CLKY respectively. Besides 16

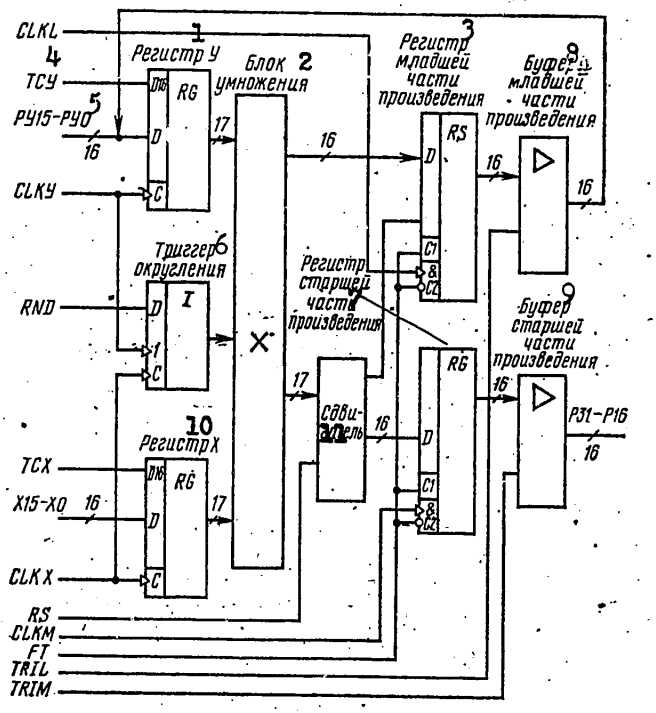

Figure 70. UM 16x16 structural circuit.

1 - Register U
2 - Multiplication unit
3 - Register of smallest part of product
4 - TCU
5 - RU15 - RU0
6 -Rounding trigger
7 - Register of largest part of product
8 - Buffer of smallest part of product
9 - Buffer of largest part of product
10 - Register X
11 - Shifter

digits of the multiplier in the registers X and Y are recorded the signs of the multiplicand and multiplier on the inputs TCX and TCY, which have the values 1 in the case where the given multiplier is a number with a sign and 0 where it is a number without a sign.

On the front of one of the signals CLKY or CYKX in the rounding trigger is recorded the value of the signals on the input RND, on which the rounding to 16 digits is done in the case where RND = 1.

The information is recorded in the register of multipliers and the rounding trigger arrives on the multiplication unit. The multiplication unit represents a combination-logical matrix in which the partial products are formed from the digital multiplication of the multiplicand by the multiplier, are summed and the result is corrected during action on a number with a sign.

The operation of rounding is accomplished simultaneously with summation of partial products by the addition of unity to the largest digit of the discarded part.

During the action on numbers with a sign the possibility is presented of adding the sign of the product of its smallest part. For that, RS must equal 0.

By means of the shifter (SD), which is controlled by the signal RS, the product P is fed in the appropriate format to registers of the smallest amd largest parts of the product.

The recording is made on the front of the signals CLKL and CLKM are blocked, the L-triggers of the registers become potential and the information from the registerinputs gradually passes to the outputs (the registers are transparent).

The output buffer cascades are controlled by the signals TPIL (the smallest part of the product) and TRIM (the largest). The buffer cascades are in an excluded state in which the control signal equals 1.

To reduce the number of used BIS outputs, the digits of the smaller part of the product are applied on the line of multiplier P4 which thus is two-directional.

6.10. 12x12 Multiplier

The 12x12 multiplier represents a high-speed combination device for multiplication of 12-digit operands. The structural circuit and working principle are analogous to the BIS of the 16x16 multiplier. A distinctive feature is that the BIS does not have two-directional outputs.

6.11. SUMMATOR (SM)

The summator is intended for simultaneous addition or subtraction of 4-digit numbers. Expansion of the digital network to any value without additional circuits is allowed. The presence of the outputs P and G permits using the transfer acceleration circuit (155IP4 or R589IK03) to reduce the summation time of multi-digit numbers.

The structural circuit of the summator BIS is presented on Figure 71. The device consists of input registers of operands with common synchronization, a summator, a sum register and an output buffer cascade. The 4-digit components arrive on the inputs DA0-DA3, DB0-DB3, DC0-DC3 and DD0-DD3 and are recorded in the input registers A, B, C and D under the condition that there is a corresponding signal (EDA, EDB, EDC and EDD) of allowance of recording. On inputs OPA, OPB, OPC and OPD are fed the signals of control connected with the signs of operations on numbers (addition or subtraction). The outputs CA0, CB0, CC0 and CD0 are transfer outputs and the inputs CAI, CBI, CCI and CDI are transfer inputs. The result of addition in the form of a 4-digit sum on the signal CLKS is received in the sum register, from which on the control signal CD by output buffer cascades it is issued to peripherals through the outputs DS0-DS3.

The result of the operation is determined with the formula:

$$DS=\pm DA\cdot EDA\pm DB\cdot EDB\pm DC\cdot EDC\pm DD\cdot EDD.$$

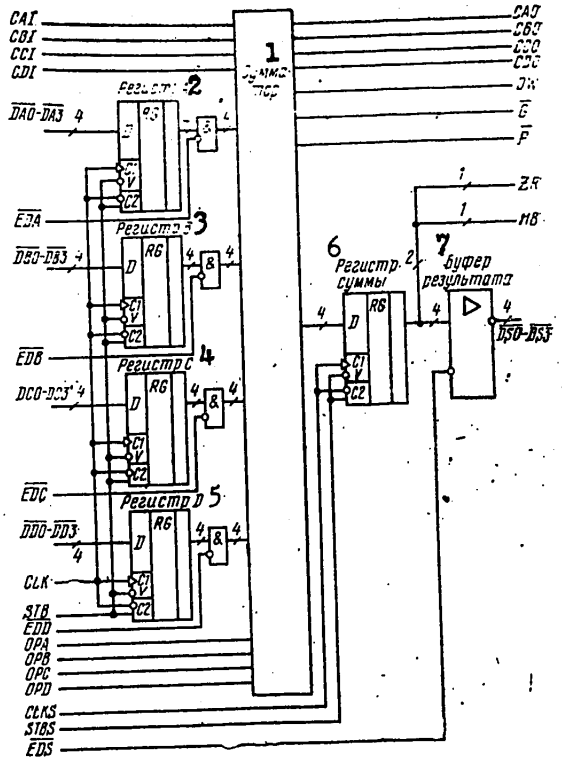

Figure 71. BIS SM structural circuit

1 - Sum
2 - Register A
3 - Register B
4 - Register C
5 - Register D
6 - Sum register
7 - Result buffer

Upon completion of the operations the sign of zero (ZR) and the sign of the result are produced.

6.12. Multifunctional main-line commutator

The multifunctional main-line commutator (MKM) is intended for organization of intramodular and intermodular data transmission main lines with the possibility of parallel logical processing (masking) of transmitted information. The BIS MKM represents a symmetric quadrupole with poles of the main line type. Monitoring circuits test the reliability of input information (monitoring the addition to parity of tetrads). The output information, masked or unmasked, is accompanied by addition to parity (control digit).

Each MKM pole receives or issues information. It is possible to recommutate information from one pole to another or to several poles at one time, the commutation (transfer) being accomplished both without change of the information and with masking of its information arriving on the BIS from other poles. Thanks to the presence of the four internal registers connected to the poles, the MKM can be used also as a register memory. Information stored in the registers can be exchanged. On each register the information (masked or unmasked) can be received from four poles.

In addition, the BIS MKM can be adjusted to perform functions of an element of duplication or masking equipment in systems with great durability.

The BIS MKM consists of the following basic units: function decoders, a register unit, a masking and commutation unit, a unit for monitoring and correction of control digits and a majoritization unit.

6.13. Multifunctional matrix of associative registers

The multifunctional matrix of associative registers (MAR) is intended for use as an ultraoperative memory (general purpose registers, registers of intermediate results, etc), for the organization of an associative memory, with retrieval of a word according to the equality of the interrogation sign and the associative sign of the word, with the possibility of masking the result of comparison, for the realization of special kinds of memory of type (for example, stack), with the possibility of simultaneous access by reading and recording addresses, and also for the construction of a memory with integrated possibilities flowing from the separateness and independence of control of the various MAR working regimes.

The MAR is organized on the (2 + 2)-address principle and is connected with the external environment by four 5-digit (four informational plus one control) two-directional main lines, four lines of indirect addressing of registers of MAR and lines of synchronization and control of the work of the BIS MAR.

The principal working regimes of the BIS MAR are:

1) a regime of superoperative memory with organization of "four + four" registers of four digits each (4 + 4 x 4 digits);

2) a regime of superoperative memory with organization of "four" registers of eight digits each (4 x 8 digits);

3) a regime of associative memory (a field of associative signs);

4) a regime of associative memory (a field of basic memory).

6.14. Programmable logical matrix

The microcircuit represents an electrically programmable logical matrix (PLM), which accomplishes eight output functions of 16 input variables.

The areas of PLM application are: PZU of large capacity; logical units; code converters; peripheral controllers; microprogram control devices; retrieval tables and control automata.

The output functions can have an active level of both 1 and 0.

Logical functions are represented in the PLM in disjunctive normal form (DNF), for example:

$$B1 = A1 \cdot \overline{A3} \cdot \overline{A5} \cdot A10 \cdot A15 \vee A2 \cdot A3 \cdot \overline{A4} \cdot A8 \vee \ldots$$

$$\ldots \vee A6 \cdot A7 \cdot \overline{A16},$$

$$\overline{B2} = A1 \cdot \overline{A3} \cdot \overline{A5} \cdot A10 \cdot A15 \vee A4 \cdot A8 \cdot \overline{A10} \cdot A11 \vee \ldots$$

$$\ldots \vee A1 \cdot A7 \cdot \overline{A12},$$

$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$

$$B8 = A4 \cdot A8 \cdot \overline{A10} \cdot A11 \vee A7 \cdot A12 \cdot \overline{A13} \cdot \overline{A14},$$

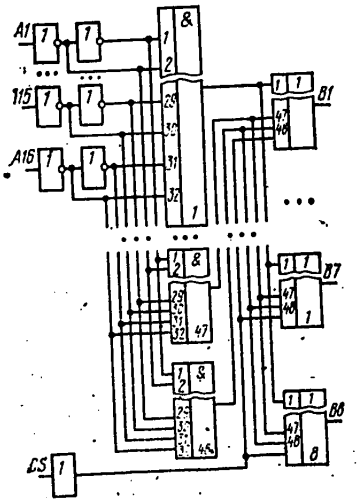

Figure 72. PLM structural circuit.

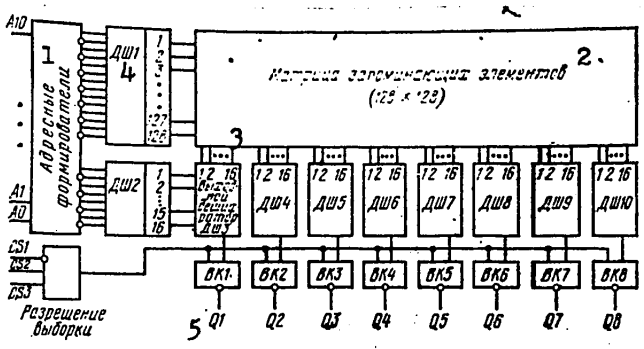

Figure 73. PPZU (2048x8) structural circuit.

1 - Address formers
2 - Memory elements matrix (128 x 128)
3 - Output decoder DSh-3
4 - DSh-1
5 - VK-1

where the output functions B1 and B8 have the active level 1 and B2 has 0. The total number of conjunctions for all functions and in the DNF of each function must not exceed 48. The PLM (Figure 72) consists of two matrices : AND and OR. The AND matrix is constructed on Schottky diodes, and the OR matrix on eight emitter transistors. The presence of a permission input permits increasing the PLM in the number of variables, conjunctions and output functions. The information recorded in the PLM is read when 0 is on the input CS, and when 1 is on that input, 1 is present on all the outputs. All connections in PLM are electrically programmable by lighting Nichrome jumpers in a programming regime.

6.15. Programmable permanent storage unit (PPZU) with organization of 2048x8 digits

The PPZU with electrical recording of information with a capacity of 16K (Figure 73) with the organization of 2048x8-digit words represents a BIS TTL with Schottky diodes and execution by methods of planar-epitaxial technology. In the initial state in unprogrammed circuits in all the memory cells 0 is recorded. The recording of 1 in the appropriate cells (programming) is done by the user by igniting Nichrome jumpers by a pulse of current once during the time of operation of the circuit. Reference to the microcircuit during the reading of information is accomplished by feeding to the access permission inputs CS1, CS2 and CS 3 of code 011 respectively. In the presence of all other combinations of the signal on those inputs all the outputs of the microcircuits are in the state 1. The address code of a read word is fed to the address inputs A0 - A10.

2174
CSO: 8144/1086

CROSS MICROPROGRAMMING SYSTEM FOR BIS MICROPROCESSOR SETS

Moscow MIKROPROTSESSORNYYE KOMPLEKTY POVYSHENNOGO BYSTRODEYSTVIYA in Russian 1981 (signed to press 3 Nov 81) pp 157-184

[Chapter 7 from book "Enhanced-Speed Microprocessor Set" by Aleksandr Ivanovich Berezenko, Lev Nikolayevich Koryagin and Artashes Rubenovich Nazar'yan, Massovaya Biblioteka Inzhenera: Elektronika, Izdatel'stvo "Radio i svyaz'", 25,000 copies, 168 pages]

[Text] The cross system of microprogramming for BIS microprocessor sets (KROSSMPK) is oriented toward work with any micorprocessor sets. The system is intended for the debugging of microprograms and the obtaining of starting data for PPZU programming. The input language is machine-independent and permits describing the controlling fields of a microinstruction and the functional connections existing between fields. The system is realized in the language FORTRAN IV and can be set up on any computer that has a translator from FORTRAN IV and a main memory capacity of at least 256K bytes.

The main function of KROSSMPK is the conversion of microprograms written in the input language INLA into a form suitable for programming various PZU and PPZU equipment. Thsi function is realized in two stages: the assembly of a program in the INLA language and the generation of a file for PZU programming.

7.1. Input Language

The INLA language is a language of free format. The syntactic units can be present in any place of the starting text: the order in which they are encountered, with the exception of some special cases, is arbitrary. Dividers (points and spaces) can be used without limitation and are used to improve legibility of the text. For the same reason a simple symbol is inserted, the point; it can be connected within identifiers. A program in the INLA language can include six phases, which consist of descriptive operators, operators of specification, operators of arrangement and operators of control language. The end of the program is designated by the service word EOF. Each phase has its own name; , the end of a phase, just like the end of operators, is not distinguished by special symbols. A program in the INLA language designated symbolically has the following structure:

PINOUT *AA ... A* INFIL *DD ... D* USFIL *DD ... D*
PROGR *CC ... C* MINOUT *AA ... A* MEMORY *MM ...*
... M EOF.

where A designates control operators, D the description operators, C the specification operators, M the arrangement operators.

Any signs may be used as separators between operators except: [and], PINOUT, INFIL and USFIL--service words designating the names of phases.

7.2. Basic KROSSMPK Modules

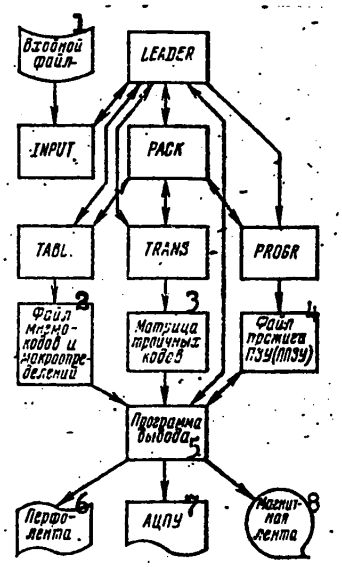

Figure 74. KROSSMPK structural circuit.

1 - Input file
2 - File of mnemocodes and macrodeterminations
3 - Tertiary codes matrix
4 - File of PZU (PPZU) burning
5 - Output programs
6 - Punched tape
7 - Alphanumeric printer ATsPU
8 - Magnetic tape

The KROSSMPK structural circuit is depicted on Figure 74. As is evident from the figure, KROSSMPK breaks down into three basic modules and a number of auxiliary programs. The module TABL is intended for the formation of tables of mnemocodes. The TRANS module is intnded for the translation of initial microprograms into a matrix of tertiary codes. The symbols 0, 1 and X are used to represent the values of the digits of fields (X used to designate indifferent values of the digits of fields). The module PROGR is intended to form a file of the PZU burning.

The INPUT program is intended for the separation from the input file of language units. The program PACK is intended for the packaging of identifiers and numbers

separated by the INPUT program. That program is used by modules of the system for the compact recording of developed information. Output programs assure output to the alphanumeric printer ATsPU, a perforator and magnetic tape of all the necessary informatin. The LEADER program is the mark program of the system and assures distribution of control between the KROSSMPK program and modules.

The starting data and tests of microprograms can be organized on any carrier. In view of the fact that the translation is accomplished in one pass, it is not necessary that the output file be rewindable.

The formed tables of mnemocodes can be recorded on magnetic tape for the special function RECOD. By the same token the stage of creation of tables is separated from the stage of translation of microprograms, which can be used separately. This is convenient, that is, practice shows that the planner changes the introduced designations much more rarely than the microprograms during their debugging. The tables of mnemocodes are connected by means of the function RESTOP.

7.3. Form and Composition of Output Information

During output to a printer the input file is divided into three parts. The first part contains a description of the microprocessor set, the second--microprogram texts, and the third a description of the used PZU (PPZU) crystal and the arrangement of the microinstruction digits by PZU digits. The output to the printer of the MPK description is made in the presence of the control word TEXTF in the operator PRINT.

The description of the PZU (PPZU) crystal and the operators of arrangement are brought out to the printer in the presence of the control word CMEMOR in the operator PRINT.

The file PROGR contains the translated text of the microprogram. The numbers and address of the microinstruction in the file PROGR can be printed in any number system. The file is brought out on the printer by pages (each page contains 60 lines).

The file TABLE containing mnemocode tables is brought out on the printer in the presence of the control word TABLE in the operator PRINT. An example of print-out of the mnemocode table is presented by Figure 75. The table is brought out on the alphanumeric printer by pages. Each page contains 28 lines. In the table headings are presented the names of the fields included in the microprogram. In the first column is the address of the microinstruction in any number system except the binary, and in the second, the marking. Printed in the table are the mnemocodes used in determining the fields in the microprogram. If any field has been determined by direct attachment in a given graph the code of the given field will be presented in the same number system as the address. If any field has been identified as a field of transition, in the corresponding graph, besides the designation of function, the address of transition will be printed. The arguments of functions are not printed in the table.

If there are more than 15 fields in the microinstruction, a transition to the following line occurs. Therefore work with the file TABLE is convenient in the case where the number of fields in the microinstruction is not more than 15.

1	2	3							
* АДРЕС	*МЕТКА	* ПОЛЯ							
*	*								
*	*	*JUMP	:RG	:F	:РЕЖИМ	:УПР	:M	:F1	:F0
: 420	:A210	:JCR(11E)	:R8	:CSR	:1ARB	:BД	:K2	:HCZ	:FF0
: 431	:A207	:JZR(1)	:AC1	:F20	:0	:VA0	:A7H	:000000:	FF1
: 437	:A213	:JCR(119)	:R0	:TZR	:0	:БСП	:K1	:HCZ	:000000:
: 436	:A212	:JCC(EE)	:R9	:F20	:0	:ПС	:V10	:HCZ	:FF1
: 356	:A214	:JZR(4)	:R0	:TZR	:0	:VA0	:K1	:HCZ	:000000:
: 4	:A261	:JZF(72)	:R0	:F10	:0	:VA0	:FBH	:HCZ	:FF0
: 167	:A372	:JCR(72)	:R0	:F10	:0	:VA0	:FBH	:HCZ	:FF0
: 162	:A262	:JFL(E2)	:R7	:INR	:0ARB	:VA0	:K2	:HCZ	:FF1
: 342	:A266	:JCR(EC)	:R0	:F10	:0	:VA0	:FBH	:HCZ	:FF0
: 354	:A268	:JCC(10C)	:AC1	:CSR	:0	:VA0	:K2	:HCZ	:FF0
: 343	:A267	:JCR(EC)	:AC1	:CSR	:0	:A8	:K2	:HCZ	:FF0
: 355	:A269	:JZR(1)	:AC1	:F20	:0	:VA0	:0FH	:000000:	FF1
: 163	:A263	:JCR(76)	:R0	:TZR	:0	:A8	:K1	:HCZ	:000000:
: 170	:A264	:JCC(108)	:R0	:TZR	:0	:VA0	:K1	:HCZ	:000000:
: 171	:A265	:JZR(1)	:AC1	:F20	:0	:VA0	:87H	:000000:	FF1
: 376	:A215	:JCR(FD)	:T1	:F20	:0	:VA0	:CH	:HCZ	:FF1

Figure 75. Example of print-out of mnemocodes table.

1 - Address 2 - Marking 3 - Fields

The cross-reference dictionary is brought out to the printer during feeding of the control word CROSSD in the operator PRINT. An example of print-out of a cross-reference dictionary is shown by Figure 76. Starting with the sixth position is printed a marker which can occupy six positions. From the 23rd to 17th positions in brackets is presented the microinstruction address where the marking has been determined, are printed the microinstruction addresses equalized on the right margin, where the given marking is used. Twenty addresses can be printed on each line. Then a transition to the following line occurs. If there is no explicit reference to any marking the communication is printed; the marking is not used in the microprogram.

To print the microprogram memory distribution circuit the control word IMAGE must be present in the operator PRINT. An example of the print-out is presented on Figure 77. On the first line are printed the addresses of the columns and in the first column the addresses of the lines in a 16-digit numeration system. If the maximum address in the microprograms is larger than 511 the distribution circuit is printed on two pages. One page contains 16 columns and 32 lines.

The following formation is printed in each cell of the circuit:

Line 1: transition code; line 2: first (if the transition is conventional) possible transition address; line 3: mark of the given cell; line 4: number of transitions into a given cell.

```
A452          (  71)   74
A413          (  72)  200
A436          (  73)   57   75
A450          (  74)   30
A451          (  75)   27
A454          (  76)   69
A361          (  77)   68
A389          (  78)   67
METKAA390  НЕ ИСПОЛЬЗУЕТСЯ В МИКРОПРОГРАММЕ 1
METKAA395  НЕ ИСПОЛЬЗУЕТСЯ В МИКРОПРОГРАММЕ
A457          (  82)   95
A399          (  83)   80  211
A400          (  84)   83
A394          (  86)   99
A458          (  87)   82
A459          (  90)   93   94
METKAA466  НЕ ИСПОЛЬЗУЕТСЯ В МИКРОПРОГРАММЕ
METKAA396  НЕ ИСПОЛЬЗУЕТСЯ В МИКРОПРОГРАММЕ
A461          (  93)   90
A456          (  94)   87
A455          (  95)   92
A384          (  96)   70
A368          (  97)  241
A385          (  98)   96
A386          (  99)  100
A393          ( 100)  106  107
METKAA355  НЕ ИСПОЛЬЗУЕТСЯ В МИКРОПРОГРАММЕ
```

Figure 76. Example of read-out of cross-reference dictionary.

1 - Not used in the micro-instruction.

```
      * JFL  * JFL  * JCR  * JCC  * JCR
      * C2H  * D3H  * DAH  * 53H  * D0H
 0DH* A432 * A403 * A4E6 * A407 * A401
      * 2    * 1    * 1    * 1    * 2
      ------------------------------------
      * JCC  * JZR  * JCR  * JCR  * JCC
      * 170H * 4H   * ECH  * ECH  * R4H
 0EH* A242 * A243 * A266 * A267 * A270
      * 3    * 1    * 1    * 1    * 2
      ------------------------------------
      * JZR  * JCC  * JCR  * JCR  * J7R
      * 1H   * 61H  * F3H  * F1H  * 4H
 0EH* A244 * A367 * A366 * A365 * A223
      * 1    * 1    * 1    * 2    * 1
      ------------------------------------
      * JCR  * JCR  * JZR  * JZR  * J7R
      * 10EH * 104H * DH   * DH   * 1H
 1DH* A201 * A202 * A805 * A806 * A199
      * 1    * 1    * 1    * 1    * 1
```

Figure 77. Example of read-out of microprogram memory distribution.

```
*****************************************************
*       *   *   *   *   *   *   *   *   *   *   *   *
*       *   *   *   *   *   *   *   *   *   *   *   *
*       *   *   *   *   P   *   *   *   *   *   *   *
*       *   J   *   *   E   *   *   *   *   *   *   *
*       *   U   *   *   *   Ж   *   V   *   *   *   *   *
*       *   M   *   R   *   *   И   *   П   *   *   *   F   F
*       *   P   *   G   *   F   *   M   *   P   *   M   *   1   0
*****************************************************
*       *   0   *   0   *   0   *   0   *   0   *   0   *   0   0
*       *   1   *   2   *   3   *   4   *   5   *   6   *   7   8
*****************************************************
1   2   *0000000 0011 111 111 112 22222222 23 33*
*АДРЕС*METKA *1234567 8901 234 567 890 12345678 90 12*
*****************************************************
*674Q *A95   *0111000 0000 101 000 011 00000000 11 00*
*675Q *A72   *0111110 1101 110 010 000 00100000 10 11*
*676Q *A73   *0111111 0000 000 000 000 11111111 11 00*
*677Q *A74   *0000111 1100 100 000 000 11111111 11 00*
*700Q *A54   *1011011 1001 010 000 000 10000000 11 11*
*701Q *A189  *0111001 1101 001 000 000 11010100 00 00*
*702Q *A28   *0110110 0001 010 000 000 11101111 11 11*
*703Q *A29   *0101101 1101 010 000 000 11110111 00 11*
*704Q *A17   *0011101 0100 100 000 000 11111111 01 00*
```

Figure 78. Example of read-out of tertiary codes matrix.

1 - Address
2 - Markint

The tertiary codes matrix is printed on the alphanumeric printer in the presence of the control word BINARY in the operator PRINT. An example of the print-out is presented by Figure 78. That table is printed in accordance with the GOST's for technical documentation.

In the table heading are printed the names of the fields, their numbers and the numbers of the microinstruction digits. In the first column are the addresses of microinstructions in any number system given in BINARY except the binary. In the second column the address marking is presented.

The file for burning the PZU (PPZU) is brought out on the printer in the presence of the control word ROMBIT in the operator PRINT. The file ROMBIT is brought out in the alphanumeric printer in accordance with the GOST's for technical documentation.

The file for burning the PZU is brought out on punched tape.

7.4. Setting Up KROSSMPK On a Computer

The KROSSMPK can be set up on any computer having a translator from FORTRAN IV and a capacity of the main memory of at least 256K bytes. To set up KROSSMPK on a computer as external information carriers magnetic tape is required for recording the mnemocodes tables and tertiary code matrices. On the same magnetic tape a library of object modules of the system can be recorded. To bring out on punched tape the file for burning the PZU the systems subprogram PTAPE, recorded on a magnetic drum, is required.

Forty zones are required for the storage of a library of object modules on magnetic tapes. For recording on tapes the intermediate results of translation, about 40 zones are required. During work the KROSSMPK occupies 160K bytes of main memory. The translation time of 512 microinstructions is 12 minutes. The system is used in the work of 55 tracts. The MPK description and the microprogram tests can be represented on punched cards or on a file of an interactive system.

To create a new library of initial modules, one must use magnetic tape containing a library of initial modules of the system, which also is recorded on magnetic tape.

2174
CSO: 8144/1086

HYBRID COMPUTERS

UDC 681.3

ABSTRACTS OF ARTICLES IN COLLECTION 'HYBRID COMPUTER DESIGN'

Leningrad IZVESTIYA LENINGRADSKOGO ORDENA LENINA ELEKTROTEKHNICHESKOGO INSTITUTA IMENI V. I. UL'YANOVA (LENINA): PROYEKTIROVANIYE GIBRIDNYKH VYCHISLITEL'NYKH USTROYSTV in Russian No 262, 1979 (signed to press 29 Dec 79) pp 2, 93-98

[Annotation and abstracts from collection of articles, "Transactions of the Leningrad Institute of Electrical Engineering imeni V. I. Ul'Yanov (Lenin), Order of Lenin: Hybrid Computer Design", edited by Prof. Ye. P. Ugryumov, 300 copies, 98 pages]

[Text] Given in the articles published in this collection are the results of theoretical and experimental research obtained in hybrid computer design.

UDC 681.31

HYBRID COMPUTING DEVICE FOR IMPLEMENTATION OF FAST FOURIER TRANSFORM

[Abstract of article by A. V. Alekseyev and V. V. Alekseyev]

[Text] Discussed in the article is the problem of organizing a hybrid computing device that implements the algorithm for a fast Fourier transform. Recommendations are made in it on selecting the structure and algorithm for device functioning as a function of requirements imposed. Figs. 4, bibl. of 7 titles.

UDC 681.325.5

ERRORS IN COMPUTATION OF FUNCTIONS BY 'DIGIT BY DIGIT' METHOD

[Abstract of article by V. D. Baykov and N. V. Kornilov]

[Text] Given in the article are results of an experimental test of the relations between accuracy in computation of elementary functions by the "digit by digit" method and processor word length. Figs. 3, bibl. of 3 titles.

UDC 62-507.681.3

STABILITY OF TRANSIENT PROCESS IN NET PROCESSOR

[Abstract of article by V. V. Doyenin and V. P. Solov'yev]

[Text] Discussed is a computer system containing a TsVM [digital computer] and net processor (SP) with fixed structure designed to solve partial differential equations by the net method. A problem associated with developing this system is that of selecting a net processor structure that ensures a stable transient process. An analysis is made in the article of the stability of a net processor built by using operational amplifiers. Figs. 2, bibl. of 4 titles.

UDC 681.325.33:519.65

APPLICATION OF PARABOLIC SPLINES IN FUNCTIONAL CONVERSION PROBLEM

[Abstract of article by A. A. Dokuchayev, V. A. Zentsov and S. F. Svin'in]

[Text] Suggested is a possible approach to design of digital-oriented functional converters based on the principle of piecewise-quadratic approximation, in which each section of the parabolic spline is represented by using piecewise-cosntant or piecewise-linear basic functions. The relation between quadratic functions and triangular basic functions is established. A new system of orthogonal basic functions is introduced. Figs. 2, tables 2, bibl. of 2 titles.

UDC 681.31

APPROACH TO IMPLEMENTATION OF COMPUTATION PROCESS OF DYNAMIC SYSTEM IDENTIFICATION

[Abstract of article by V. G. Yegorov]

[Text] Considered is a possible approach to organizing the computational process of identification. Identification of a dynamic system is effected by the method of stochastic approximation by hybrid facilities oriented to digital control computer. Bibl. of 3 titles.

UDC 681.325.53

ARRAY COMPUTING DEVICES FOR CONVERSION OF NUMBERS FROM ONE NUMBER SYSTEM TO ANOTHER

[Abstract of article by L. A. Zaykova]

[Text] Array computers for number conversion. Analysis of data rate of these devices has shown that operation execution rate in them increases threefold compared to known array devices and 15-fold compared to similar devices with shift registers. Figs. 2, bibl. of 1 title.

UDC 681.3.023:681.325.0

OPERATIONAL AUTOMATON STRUCTURAL OPTIMIZATION BY INFORMATION CRITERION

[Abstract of article by A. L. Ivanov]

[Text] Discussed in the article is a method for optimizing the structure of an operational automaton implemented with shift registers. The operational automaton is covered by a set of interchangeable structurally redundant functional modules. A technique is given for determining the optimal number of interchangeable functional modules. Figs. 7, bibl. of 4 titles.

UDC 681.34

PROGRAM SIMULATION OF ALGORITHMS FOR COMPILATION OF SCHEDULES OF OPERATION OF HYBRID COMPUTING SYSTEMS

[Abstract of article by V. N. Knyazev and A. V. Kraynikov]

[Text] Several heuristic algorithms are suggested for compiling operating schedules of hybrid computing systems. Results are given for program simulation to obtain statistical assessments of efficiency of the proposed algorithms. Figs. 2, bibl. of 4 titles.

UDC 681.51:519.712

AUTOMATON APPROACH TO DESIGN OF DEVICES ORIENTED TO EXECUTION OF ANALYTIC CONVERSIONS

[Abstract of article by E. Stempen' and O. G. Kokayev]

[Text] Discussed in the work are problems associated with design of devices oriented to execution of analytic conversions (AP). A converter with stack memory and initial automaton are used to formally describe a translator that translates descriptions of algorithms for analytic conversions from the input to an intermediate language, Polish inverse notation. The structural implementation of the control unit for this translator is suggested. Figs. 1, bibl. of 4 titles.

UDC 681.327:534.78

QUASIANALOG UNIT FOR PREPROCESSOR PROCESSING OF SPEECH SIGNAL

[Abstract of article by V. P. Korovatskiy and S. A. Myglan]

[Text] Structure is given for a speech signal preprocessor implemented on the base of series produced digital and analog equipment. Technical data are given relative to functional capabilities of this unit applicable to solving a broad range of problems in recognizing and identifying speech signals. Figs. 1, bibl. of 5.

UDC 681.34:62-503.55

PROGRAM CONTROL OF EQUIPMENT IN AN ANALOG-DIGITAL DATA PROCESSING SYSTEM

[Abstract of article by S. M. Krylov]

[Text] Considered in the article are the structure, schemtaic implementation and capabilities of a simple processor for program control of equipment in an analog-digital system for acquisition, processing and conversion of data for multipurpose function. Results obtained with prototype are given. Figs. 2, bibl. of 6 titles.

UDC 519.2:621.3

EFFECT OF REMAINDER TREND ON ERROR IN EVALUATING CORRELATION FUNCTION

[Abstract of article by D. D. Nedosekin and F. V. Yan]

[Text] Analytic expressions are derived for displacement and dispersion of evaluation of correlation function of random process containing remainder trend. Bibl. 2.

UDC 681.351

EXPERIMENTAL RESEARCH OF MULTIPLICATIVE ALGORITHM FOR DETERMINING NORMED CORRELATION FUNCTION

[Abstract of article by V. K. Shmidt and M. I. Nemchenko]

[Text] Discussed in the article is the effect of size of digitizer and duration of implementation of random process on mean-square error of computation of normed correlation function of multiplicative algorithm. Figs. 4, bibl. of 4 titles.

UDC 681.325

DIFFERENCE-ITERATION METHOD OF FOURIER TRANSFORM IMPLEMENTATION

[Abstract of article by A. M. Oranskiy, B. V. Nemytov and M. S. Lozovik]

[Text] Discussed in the article are the various methods for implementing Fourier transform. Comparative analysis by speed is made of them. A new modification is given for the difference-iteration algorithm for fast Fourier transform that speeds up solving the problem. Bibl. of 5 titles.

UDC 621.317.087.92

APPLICATION OF FUNCTIONAL CONVERTERS IN CIRCUITS FOR METERING INSULATION RESISTANCE OF DIRECT CURRENT NETWORKS

[Abstract of article by V. A. Red'kin and Ye. P. Ugryumov]

[Text] Classified are known methods of automatic checking of insulation resistance of direct-current circuits at operating voltage. A new structure is suggested for a transducer containing a functional converter that reproduces the hyperbolic relationship. Figs. 4, bibl. of 6 titles.

UDC 681.335.8

COMPLEX-SHAPE SIGNAL GENERATION BASED ON PIECEWISE-LINEAR INTERPOLATION

[Abstract of article by S. Yu. Rzheutskaya]

[Text] Methods are discussed for generating time functions based on piecewise-linear interpolation of reproduced functional relationships. Suggested is a structure of a device that permits performing computation of each value of a function in one step of a summing operation. Figs. 1, bibl. of 2 titles.

UDC 681.3.06

ANALOG-DIGITAL DEVICE FOR DETERMINING MACh

[Abstract of article by A. A. Smagin, G. Ye. Konyukhov, V. V. Prokof'yev and A. V. Gofman]

[Text] Discussed in the article is the organization of a calculator of the aerodynamic parameter to determine the Mach number. The device includes the tabular method for realization of the function of two variables. Analyzed in detail is interpolation of the function by planes and equipment costs are estimated for a PZU [read-only memory] to store values of the function at nodal points, as well as of correcting functions. Structural scheme of the calculator is given and algorithm for its operation is suggested. Figs. 1, bibl. of 2 titles.

UDC 681.327.17

STORAGE SIZE SELECTION FOR DISCRETE OBJECT DIAGNOSING HARDWARE

[Abstract of article by V. P. Kalyavin and S. N. Nikiforov]

[Text] Discussed in the article is the problem of determining storage size for facilities for locating defects in discrete objects with many outputs. To this end, the known diagnostic methods are divided into two groups: combinational and sequential. Based on features of information processing in the process of locating defects, analytic expressions are derived for determining storage size in checking serviceability and locating single and multiple defects. Comparative analysis of expressions derived is made. Factors of relations of combinational and sequential diagnostic methods are plotted. Figs. 1, tables 1, and bibl. of 2.

UDC 621.372.63.001

ON POSSIBILITY OF USING ACTIVE RC CIRCUITS TO SOLVE PARTIAL DIFFERENTIAL EQUATIONS

[Abstract of article by A. V. Bondarenko]

[Text] Discussed in the article is the problem of implementing nets designed to solve partial differential equations by using active RC circuits built on the basis of gyrator circuits. A new gyrator circuit is suggested that is implemented by using voltage amplifiers with finite amplification factors. Figs. 3, bibl. 4.

8545
CSO: 1863/83

UDC 681.31

HYBRID COMPUTING DEVICE FOR IMPLEMENTATION OF FAST FOURIER TRANSFORM

Leningrad IZVESTIYA LENINGRADSKOGO ORDENA LENINA ELEKTROTEKHNICHESKOGO INSTITUTA IMENI V. I. UL'YANOVA (LENINA): PROYEKTIROVANIYE GIBRIDNYKH VYCHISLITEL'NYKH USTROYSTV in Russian No 262, 1979 (signed to press 29 Dec 79) pp 3-7

[Article by A. V. Alekseyev and V. V. Alekseyev]

[Text] Used most often and extensively to evaluate the frequency properties of a random process is the method of calculating the spectral density by a Fourier transform (PF) with subsequent smoothing [1]:

$$G_{xy}(f)=\lim_{M}M\left[S_x(f)S_y(f)\right], \quad (1)$$

where.. $S_x(f)=\int_0^T \xi(t)e^{j\omega t}dt$

or in discrete form: $S_x(f)=\frac{2}{N}\sum_{i=0}^{N-1}(\Delta t\, i)W^{fi}$, (2)

where $W^{\kappa}=e^{j\frac{2\pi}{N}\kappa}$.

This method was used widely after Cooley and Tukey, American mathematicians, invented the algorithm for the fast Fourier transform [FFT] in 1965 [2]. FFT algorithms were invented for application and make use of the specific nature of TsVM [digital computers] (binary representation of information). This article is aimed at examining the possibilities of implementing an FFT by the facilities of a GVU [hybrid computing device] with discrete-controlled parameters [3].

Let us consider the FFT algorithm shown in fig. 1 [4, 5].

This algorithm has the following main advantages:
--input and output data are arranged in natural order;
--natural sequence of indexes of weight factors within each tier;
--symmetry of relationships within each tier; and
--identity of relationships between tiers.

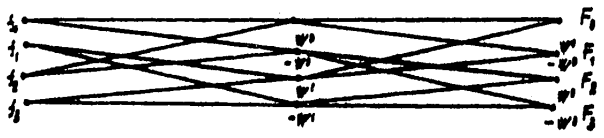

Fig. 1.

They all make it possible to more simply organize the calculation process. The nodes of the graph-scheme for the algorithm can be divided into two types:
--nodes at which addition of two complex numbers occurs:

$$[Re(f_i)+\Im_m(f_i)]+[Re(f_j)+\Im_m(f_j)]; \qquad (3)$$

--and nodes at which two operations of multiplication with subsequent addition are performed:

$$[Re(f_i)+\Im m(f_i)]\cdot W^K+[Re(f_j)+\Im m(f_j)]\cdot(-W^K).$$

This algorithm can be implemented as a hybrid cellular array [6] (fig. 2).

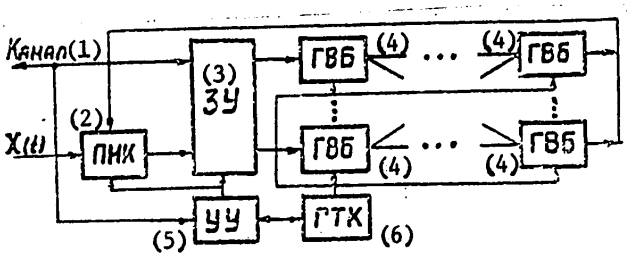

Fig. 2.

Key:
1. channel
2. PNK -- voltage-to-digital converter
3. ZU -- storage unit
4. GVB -- hybrid computing unit
5. UU -- control unit
6. GTK -- trigonometric factor generator

The role of each node in the graph-scheme of fig. 1 is performed by a hybrid computing unit (GVB).

The device operates as follows:
after the control unit (UU) receives the control information, it tunes the structure to the needed dimension of analysis; in the process, there occurs coding in the voltage-to-digital converter (PNK) and storage by the storage unit (ZU) of the data subject to processing, as well as generation of the necessary matrix of trigonometric factors (W^K) by the trigonometric factor generator (GTK). After completion of the preparatory period in the response time at the output of the device, the Fourier factor values are set that after coding in the voltage-to-digital converter can be output upon request to an external device.

The advantages of this computer are:
--minimal calculation time achieved by maximal parallelism of the process of processing the input data; and
--the capability of multidimensional analysis.

However, organization of calculation by the FFT algorithm for an input series of N terms will require N $\log_2 N$ GVB [hybrid computing units], which when $N>2^5$ results in high costs for equipment and is therefore not always implementable. Usually, all digital processors implement by hardware or algorithm one or more "butterflies" (four nodes of the graph-scheme of the FFT algorithm linked directly to each other), which in the process of calculation cover the entire algorithm, organizing the logic in the appropriate way [7]. It is convenient to also use this approach in designing the hybrid device, since it will allow substantial reduction of the equipment used.

Let us consider the organization of a hybrid processor with shift registers as storage units ZU1, ZU2, ZU5 and ZU6 (diagram of it is shown in fig. 3).

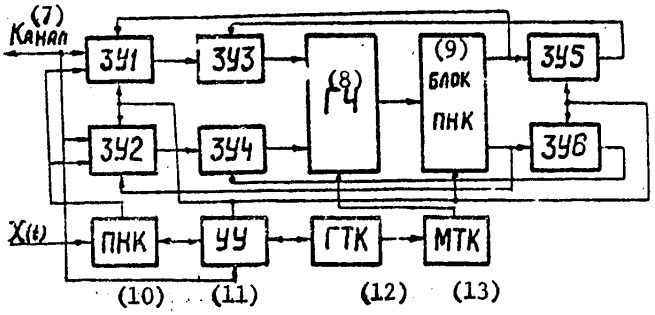

Fig. 3.

Key:
1-6. ZU1 - ZU6 -- storage unit 1 -6
7. channel
8. GCh -- hybrid section
9. PNK -- voltage-to-digital converters
10. PNK -- voltage-to-digital converter
11. UU -- control unit
12. GTK -- trigonometric factor generator
13. MTK -- trigonometric factor matrix

The device operates as follows.

First, the two storage units ZU1 and ZU2 are filled with information to be processed; the first half goes into ZU1, the second to ZU2. Then sequential processing of the primary information starts. Depending on the number of hardware implemented "butterflies" (GVB [hybrid computing units]) in the hybrid section (GCh), the UU [control unit] fills up storage units ZU3 and ZU4, which are linked directly to the hybrid computing units, while the trigonometric factor generator (GTK) fills up the trigonometric factor matrix (MTK), also linked to the GVB [hybrid computing units]. Upon completion of these operations, the voltage-to-digital converters (PNK) code the results obtained which are then stored by the control unit in units ZU5 and ZU6. Then this process is repeated until all the information in storage units ZU1 and ZU2 is processed and there are no values corresponding to first tier values stored in units ZU5 and ZU6. For the computation run in the second tier, the calculation process is similarly organized, except that ZU5 and ZU6 are used to store the initial information and processing results are stored in ZU1 and ZU2.

That is how the values in all tiers are calculated. The control unit takes the final result from either ZU1 and ZU2 or ZU5 and ZU6 depending on the value of the initial access.

In designing a hybrid processor, a number of problems occur that are associated with selecting the width of the quantities involved in the calculation process [7], the number of voltage-to-digital converters for converting intermediate analog signals to digital form and the number of hybrid computing units (GVB). The solution to these problems has a considerable effect on calculation accuracy and time.

For the structure in question, analysis of the relation between FFT algorithm computation time and the number of "butterflies" (GVB) implemented and the number of PNK [voltage-to-digital converters=VDC] used in processing information was performed (fig. 4). The analysis was made for the case when the initial array contained 512 numbers, and the pulse generator frequency was 1 MHz.

Key:
1. execution time, microseconds
2. number of butterflies
3. 4 VDC's
4. 8 VDC's
5. 8 VDC's (16 VDC's)
6. 8 VDC's
7. 16 VDC's
8. 32 VDC's

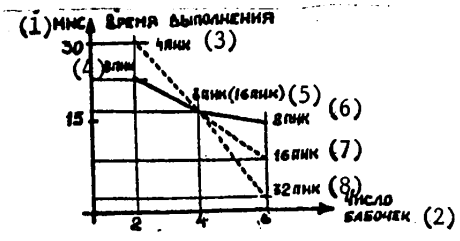

Fig. 4.

The most interesting case is the structure of a computer containing four "butterflies" implemented by hardware. In this case, the capability of making computations in parallel allows having the number of voltage-to-digital converters without changing information processing time, i.e. processing the analog signals at the output of the hybrid section (GCh) not within one step, but two. Parallel computation occurs because while the VDC's are processing the computation results from one half of the hybrid computing units, the initial registers are being filled and computation is performed in the other. The hybrid processor structure using four VDC's and implementing four "butterflies" by hardware was deemed acceptable. If computation time must be reduced, hardware must be increased in accordance with fig. 4.

BIBLIOGRAPHY

1. Gribanov, Yu. I. and Mal'kov, V. L., "Spektral'nyy analiz sluchaynykh protsessov" [Spectral Analysis of Random Processes], Moscow, "Energiya", 1974.

2. Cooley, J. W. and Tukey, J. W., "An Algorithm for the Machine Calculation of Complex Fourier Series," MATH. COMPUTER, Vol 19, 1965.

3. Smolov, V. B. and Chernyavskiy, Ye. A., "Gibridnyye vychislitel'nyye ustroystva s diskretno-upravlyayemymi parametrami" [Hybrid Computing Devices with Discrete-Controlled Parameters], Moscow, "Mashinostroyeniye", 1977.

4. Gold, B. and (Ryder, I.), "Digital Processing of Signals," Moscow, "Sov. radio", 1973.

5. (Rabiner, L.) and Gold, B., "Theory and Application of Digital Processing of Signals," Moscow, "Mir", 1978.

6. Alekseyev, V. V. and Nedosekin, D. D., "Printsipy postroyeniya gibridnogo protsessora BPF na osnove odnorodnoy struktury. Doklad" [Principles of Design of Hybrid Fast Fourier Transform Processor Based on a Cellular Structure. A Report], Kiev, "Naukova dumka", 1976.

7. Domoratskiy, A. N.; Ivanov, L. N. and Yurlov, Yu. I., "Mnogotselevoy statisticheskiy analiz sluchaynykh signalov" [Multipurpose Statistical Analysis of Random Signals], Novosibirsk, "Nauka", 1975.

8545
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ARRAY COMPUTING DEVICES FOR CONVERSION OF NUMBERS FROM ONE NUMBER SYSTEM TO ANOTHER

Leningrad IZVESTIYA LENINGRADSKOGO ORDENA LENINA ELEKTROTEKHNICHESKOGO INSTITUTA IMENI V. I. UL'YANOVA (LENINA): PROYEKTIROVANIYE GIBRIDNYKH VYCHISLITEL'NYKH USTROYSTV in Russian No 262, 1979 (signed to press 29 Dec 79) pp 24-28

[Article by L. A. Zaykova]

[Text] The problem of achieving maximum speed in executing various operations is a major problem for developers of hybrid computing complexes. Array computing devices (MVU) allow with a specified element base achieving maximum speed in executing various arithmetic operations. It is advantageous to expand the class of problems implementable by using array computing devices. To this end, let us consider the problems of designing array computing devices to convert numbers from one number system to another.

The algorithms for conversion of numbers [1] that can be expressed by using iteration formulas are well known:

1. Conversion of an integer decimal number A into binary. The number A in the binary number system will be represented in the form of $A = a_m \cdot a_{m-1} \ldots a_0$, which means:

$$A = a_m \cdot 2^m + a_{m-1} \cdot 2^{m-1} + \ldots + a_1 \cdot 2^1 + a_0,$$

where $a_0 < 2$ is the remainder from dividing the number A by 2. To obtain the other remainders, which are digits of the number A in the binary number system, the iteration formula has the form:

$$A_i = \frac{A_{i-1} - a_{i-1}}{2}, \quad \text{remainder } a_i,\ A_0 = A, \quad i = 1, 2, \ldots, m = 1, \tag{1}$$

where A_{i-1} is the integer part of the quotient obtained in the (i-1) step.

2. Conversion of a fractional decimal number B into binary. The number B, represented in the binary number system as $B = b_1 b_2 \ldots b_m$, can be notated:

$$B = b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \ldots + b_{m-1} \cdot 2^{-(m-1)} + b_m \cdot 2^{-m}.$$

From which the iteration formula for conversion equals:

$$b_i = 2B_{i-1} - B_i, \quad i = 1, 2, \ldots, m, \quad B = B_0, \tag{2}$$

where b_i is the i-th digit of the binary number equal to the integer part of the decimal number, and B_{i-1} is the fractional part of the decimal number in the (i-1) step.

3. Conversion of an integer binary number A to decimal. The binary number $A = a_m \ldots a_1 a_0$ can be represented as $A = (\ldots((a_m \cdot 2 + a_{m-1}) \cdot 2 + \ldots + a_2) 2 + a_1) \cdot 2 + a_0$. The iteration formula for finding the decimal number is defined as

$$A_{m-i} = A_{m-i+1} \cdot 2 + a_{m-1} \qquad \begin{matrix} i=1, 2, 3 \ldots m-1 \\ A_m = a_m \end{matrix} \tag{3}$$

The result of the operation is the decimal number $A = A_i$.

4. Conversion of a fractional binary number into decimal. The binary number $B = b_1 b_2 \ldots b_m$ can be notated in the form of:

$$B = ((\ldots(b_m \div 2 + b_{m-1}) \div 2 + \ldots + b_2) \div 2 + b_1) \div 2.$$

The iteration formula for finding the decimal number has the form:

$$B_{m-1} = B_{m-i+1} \div 2 + b_{m-i} \qquad \begin{matrix} i = 1, 2, \ldots, m-1 \\ B_m = b_m \end{matrix} \tag{4}$$

The result of the operation is the decimal number $B = B_1 \div 2$.

It can be seen from an analysis of the formulas (1-4) that the conversion operations can easily be implemented by using two types of array computing devices since the operations for converting an integer decimal number to binary and a fractional number to decimal are identical in methods of implementation. Also similar are the operations for converting a fractional decimal number to binary and an integer binary number to decimal.

Fig. 1. shows an array computing device for converting an integer decimal number to binary and a fractional dinary number to decimal. The device consists of rows of basic cells, each containing a one-digit adder and gate, while each tetrad of basic cells contains a control bus.

The device operates the following way. In converting an integer decimal number to binary, the binary-coded number A enters inputs A_1-A_8 of the one-digit adders of the basic cells of the corresponding tetrads. The two's complement binary code of the number 3 enters the second inputs of the adders in all tetrads. A shift of the tetrads one bit to the right, which corresponds to the operation of dividing the contents of the tetrads by 2, is performed by the corresponding internal array connections. In the shift, if a one is moved into a given tetrad, then performed in it is the operation of adding the number at the tetrad input to the two's complement code of the number 3, which corresponds to correction of the division operation [1]. But if a zero is moved in, by using the gates, the number entering the tetrad input is sent to the tetrad output.

The operation result, an integer binary number, is generated at outputs a_m-a_0.

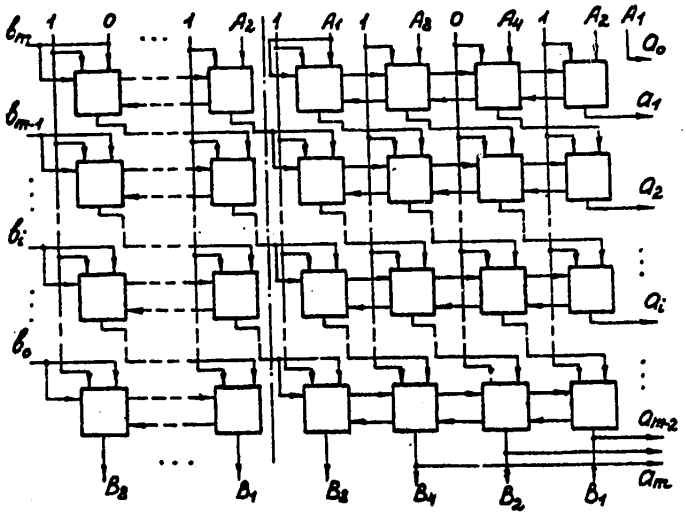

Fig. 1.

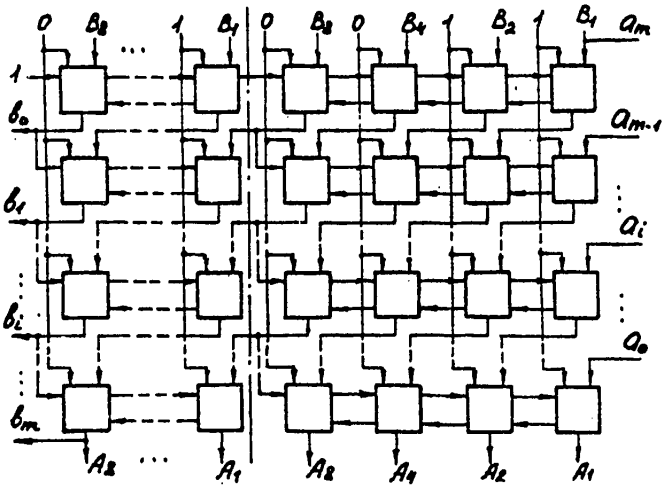

Fig. 2.

In converting a fractional binary number to decimal, it enters inputs b_0-b_m.

The operations performed in the device are similar to the foregoing. The operation results, tetrads of the binary-coded fractional decimal number, are generated at outputs B_1-B_8 of the device.

Fig. 2 shows an array computing device for converting a fractional decimal number to binary and an integer binary number to decimal. In its structure, the device is similar to the preceding one, but in this case, the basic cell is an adder-subtracter.

In converting a fractional decimal number, the binary-coded form of the number enters inputs B_1-B_8 of the corresponding tetrads, and the binary code of the number 3 enters the other inputs. In all tetrads in the first row, the source number is converted into code with a surplus 3 to simplify correction of the multiply operation [1]. A shift of all tetrads one position to the left, which is equivalent to the operation of multiplying the contents of the tetrads by 2, is performed by the corresponding internal array connections. The correcting step in the shift to the left consists of subtracting the number 3 in those tetrads from which a one was shifted to the adjacent decimal position. The operation result is generated at outputs b_0-b_m.

In converting an integer binary number to decimal, the number enters inputs a_m-a_0 of the deivce. The operation is performed by the method described above. Tetrads of the binary-coded decimal number are generated at outputs A_1-A_8 of the device.

Results of analysis on the speed of these devices and the known array devices for number conversion have shown that these array computing devices permit about a threefold increase in the speed of the number conversion operation; compared to similar devices with shift registers, there is a 15-fold increase.

The regularity and uniformity of the array computing device structure make them most promising for implementation in the form of large-scale integrated circuits.

BIBLIOGRAPHY

1. Kartsev, M. A., "Arifmetika tsifrovykh mashin" [Arithmetic of Digital Computers], Moscow, "Nauka", 1969.

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QUASIANALOG UNIT FOR PREPROCESSOR PROCESSING OF SPEECH SIGNAL

Leningrad IZVESTIYA LENINGRADSKOGO ORDENA LENINA ELEKTROTEKHNICHESKOGO INSTITUTA IMENI V. I. UL'YANOVA (LENINA): PROYEKTIROVANIYE GIBRIDNYKH VYCHISLITEL'NYKH USTROYSTV in Russian No 262, 1979 (signed to press 29 Dec 79) pp 44-49

[Article by V. P. Korovatskiy and S. A. Myglan]

[Text] The modern applications of speech signal (RS) recognition include:
1) recognition of isolated words in a restricted vocabulary
2) verification of speakers
3) identification of a person
4) diagnostics of defects in conversational speech
5) diagnostics and classification of singing voices
6) diagnostics of the psychophysiological state of a person
7) recognition of sounds of the past.

There are now two alternative approaches to designing recognition systems.

The first approach is based on applying general-purpose computers to organizing digital methods of speech signal processing [1, 2].

The second method is based on constructing specialized devices for preprocessor rigid (nonadaptive) processing of speech signals to reduce their volume and extract informative features and the speech signals are subsequently classified on the same general-purpose computers [3, 4].

The second approach is of particular interest from the viewpoint of the problem of designing autonomous units for recognition of isolated words from a fixed (tuneable) vocabulary, as well as speech-input computer terminals (real-time input of speech). However, two substantial shortcomings inherent to this approach must be pointed out. First, there is a rigid relationship between the structure of the unit for preprocessor processing (RR unit) as well as the composition of its functional assemblies and the qualitative-quantitative composition of the feature space selected subjectively and arbitrarily by the developers. Second, there is the orientation to performing classification by using one processor, for example, one minicomputer. In the process, on one hand, there is a great variety of particularly specialized designs for preprocessors made in the overwhelming majority on the basis of specially developed functional assemblies. And on the other hand, there is an obvious disparity between the linear sequence of the computational process and the capability (necessity) of organizing the spatially separated process

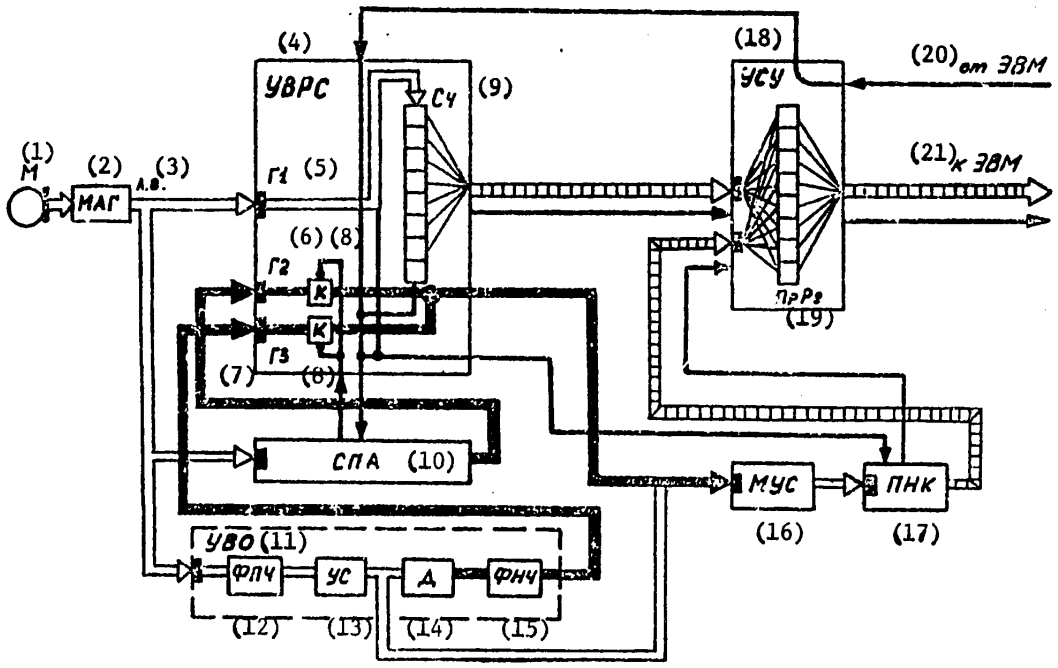

Fig. Speech signal preprocessor

Key:

⟹ denotes circuit for input analog information signal (complete speech signal - PRS)

➡ denotes circuits for analog information signals

⇛ denotes circuits for coded information signals

⟶ denotes circuits for control signals (commands and notifications)

1. M [expansion unknown]
2. MAG - magnetic tape recorder
3. L.V. [expansion unknown]
4. UVRS - speech signal input unit
5. G1 [expansion unknown]
6. G2
7. G3
8. K [expansion unknown]
9. Sch - adder-accumulator
10. SPA - spectrum analyzer
11. UVO - envelope separator
12. FPCh - tuneable frequency filter
13. US - amplifier
14. D - detector
15. FNCh - low-pass filter
16. MUS - scaler
17. PNK - voltage-to-digital converter
18. USU - universal interface
19. PrRg - receiving register
20. from computer
21. to computer

of computations (parallel computational processes). In the process, both these substantial shortcomings are interdependent.

Shown in the drawing is the structure of an RR RS [speech signal preprocessor] which to a considerable extent eliminates the first of the aforementioned shortcomings, and also facilitates to a certain degree eliminating the second one.

Purpose and Basic Technical Characteristics of the Functional Devices in the RR [Preprocessor] Unit (see figure).

1. The speech signal input unit (UVRS) is specialized and makes it possible to effect:
1.1) actual isolation of the speech signal start moment (pulse)
1.2) fictitious isolation of the speech signal end moment (pulse)
1.3) definition of the acoustic pause interval τ_p in the speech signal, and in the process, $\tau_p^{max} = 0.8 \times 2^8 = 0.8 \times 256 = 205$ ms
1.4) count of density of "nulls" of complete speech signal in a constant interval of cyclic time of analysis $\tau_n = 800$ microseconds by using an Sm 8-bit adder-accumulator
1.5) amplitude selection of external sound noise from the equivalent level of voltage at input to the speech signal input unit, 5 mV (-45 dB) to 0.77 V (0 dB) at 10 thresholds
1.6) synchronization of operation of all other functional devices in the RR [preprocessor] unit, except the UVO [envelope separator] and MU [scaler].

2. The low-frequency band spectrum analyzer (SPANCh) is the FSP-80 series produced parallel-type spectrum analyzer and makes it possible to effect:
2.1) instantaneous harmonic analysis of the complete speech signal (PRS) in the band from 1.5 Hz to 22.4 kHz by using 38 third-octave filters with a filter scanning frequency (frame frequency) of 33 Hz and adjacent filter switching time (clock time) of 800 microseconds; in the process, the informative band of actual frequency analysis of the PRS [complete speech signal] selected was 100 Hz - 10 kHz and is covtred by using 21 filters
2.2) synchronization of the start of the PNK [voltage-to-digital converter] every 800 microseconds.

3. The envelope separating device (UVO) is specialized and consists of a tuneable frequency filter (FPCh), amplifier (US), detector (D) and low-pass filter (FNCh).

In the process, the FPCh is an active band-pass filter, the upper f_u and lower f_l cut-off frequencies of which can be independently tuned: the f_l from 0 to 6300 Hz, and the f_u from 700 Hz to ∞. The US [amplifier] provides the needed amount of the detected signal for approximation of the characteristic D in the appropriate form; i.e. with signals in the interval 0.2-1 V, a parabolic approximation (square-law detector), and with signals exceeding 1 V, a linear approximation (linear detector). The detector (D) is made with a half-wave circuit, most suited for the purposes of isolating the frequency of the fundamental tone F_0 by the peak method of analysis of the envelope [5]. The FNCh is an active low-pass filter with three discrete cut-off

values: 15, 30 and 60 Hz. The envelope input unit (UVO) permits effecting isolation of the envelope of the PRS [complete speech signal] with the time constant τ_0=17 ms (low-pass filter cutoff frequency is 60 Hz).

4. The scaler (MUS) provides for matching of the output dynamic bands of the analog signals of the envelope and spectrum readings with the input dynamic band of the PNK [voltage-to-digital converter].

5. The voltage-to-digital converter (PNK) is an F733 series produced converter with a coding cycle of 100 microseconds and 12 information bits in the output code (1 sign bit).

The converter enables coding of the instantaneous amplitudes of the spectrum readings and envelope, as well as the PRS [complete speech signal] from the output of the US [amplifier]. In the process, only the eight high-order bits are used.

6. The universal interface (USU) is designed to connect the output of the quasi-analog unit for preprocessor processing of the RS [speech signal] with any TsVM [digital computer] that has the FS-1500 type photoinput module (the universal interface fully matches the FS-1500 interface).

The main mode of operation of the RR [preprocessor] unit provides for organization of three parallel channels of different-type information on the complete speech signal, namely:

a) channel for input of density of "nulls" in the complete speech signal (channel I)
b) channel for input of amplitude-frequency cutoffs of complete speech signal (channel II)
c) channel for input of envelope of complete speech signal (channel III).

In the process, the input PRS [complete speech signal] with dynamic range up to 40 dB from the line output of the magnetic tape recorder goes simultaneously into the inputs G1 of the UVRS [speech signal input unit], the SPA-NCh [low-frequency band spectrum analyzer] and the UVO [envelope separator]. The threshold device in the speech signal input unit fixes the moment of the beginning of a word by generating the appropriate pulse by which the electronic switch is actuated for polling the comb of band-pass filters in the spectrum analyzer.

Delay in the start of operation of the switch in relation to the moment the actuating pulse originates is no more than 3.2 ms. At each successive moment of switching of the corresponding band-pass resonant filter, the amplitude of the spectrum reading of the latter goes from the spectrum analyzer output to input G2 of the speech signal input unit, and a control pulse is generated by the analyzer and goes to the speech signal input unit. Performed upon this pulse is the output of the code of the density of "nulls" in the complete speech signal, formed within the 800 microsecond time, from the counter in the speech signal input unit to the receiving register PrRg in the USU [universal interface] along with the notification signal "Code Output." By this same control pulse from the spectrum analyzer, the voltage-to-digital converter is actuated and . the digital code of the amplitude of the spectrum reading is generated, which goes from the spectrum analyzer in transit through the appropriate gate to the speech signal input unit to the scaler and voltage-to-digital converter. Then the converter is reactuated to code the amplitude of the complete speech signal envelope, which goes from the

envelope separator output in transit through the appropriate gate to the speech signal input unit to the scaler and converter. The codes of the amplitudes of the spectrum readings and envelope go to the receiving register PrRg in the universal interface alternately in time along with the corresponding notification signals "Code Output" generated by the converter.

Thus, every 800 microseconds, from the receiving register in the interface unit, there go to the computer (digital unit for isolating secondary features and performing classification) in parallel form sequentially one after the other three byte words, namely the code of channels I, II and III respectively along with the corresponding "Code Output" notification signals. When the speech signal ends (fictitious, i.e. with the τ_p^{max}=205 ms delay), the speech signal input unit generates a pulse used to terminate operation of the spectrum analyzer and the entire preprocessor as a whole. The same effect is achieved when the signal "Input Interruption" is received from the digital computer through the universal interface by the speech signal input unit.

In addition to the basic mode discussed, the preprocessor provides two auxiliary modes.

In auxiliary mode I, the complete speech signal is input from the amplifier output directly through the scaler, converter and interface to the computer. In the process, the initial actuation of the converter and interruption of its operation is effected by the detector of the start and end of the speech signal in the speech signal input unit (by the "Input Interruption" signal from the digital computer) respectively.

In this mode, the converter is actuated by a crystal oscillator with a frequency of 10 kHz.

In this case, the source complete speech signal has to be passed through a low-pass filter with a 5-kHz cutoff frequency respectively. Such a filter is organized by tuning the tuneable frequency filter.

Auxiliary mode II is the mode of operating the spectrum analyzer autonomously, achieved by disconnecting the other functional devices in the preprocessor.

In conclusion, it is necessary to note that the principle of the preprocessor with organization of three flows of information on the complete speech signal, implemented in this work on the base of series produced devices of VG [expansion unknown], both analog and digital, with a minimum number of specialized devices in the preprocessor structure, can be considered a prototype in designing autonomous devices for recognition of isolated words in a fixed vocabulary as well as for some of the other tasks listed in the first paragraph of this article.

BIBLIOGRAPHY

1. Somin, N. V., "Package of Application Programs for Speech Signal Research," in "Analiz i raspoznavaniye rechevykh signalov na EVM" [Analysis and Recognition of Speech Signals with Computers], Moscow, VTs AN SSSR [USSR Academy of Sciences Computer Center], 1975, pp 3-19.

2. Rabiner, L. and Gould, B., "Theory and Application of Digital Processing of Signals," Moscow, "Mir", 1978.

3. Donbayev, E. B., "On One Universal Device for Isolation and Input of Speech Features into a Computer," in "Analysis and Recognition of Speech Signals with Computers," Moscow, USSR Academy of Sciences Computer Center, 1975, pp 75-86.

4. Gudonavichus, R. V. et al., "Raspoznavaniye rechevykh signalov po ikh strukturnym svoystvam" [Recognition of Speech Signals by Their Structural Properties], Leningrad, "Energiya", 1977.

5. Sapozhkov, M. A., "Rechevoy signal v kibernetike i svyazi" [The Speech Signal in Cybernetics and Communication], Moscow, "Svyaz'", 1963.

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CSO: 1863/83

UDC 681.34:62-503.55

PROGRAM CONTROL OF EQUIPMENT IN ANALOG-DIGITAL DATA PROCESSING SYSTEM

Leningrad IZVESTIYA LENINGRADSKOGO ORDENA LENINA ELEKTROTEKHNICHESKOGO INSTITUTA IMENI V. I. UL'YANOVA (LENINA): PROYEKTIROVANIYE GIBRIDNYKH VYCHISLITEL'NYKH USTROYSTV in Russian No 262, 1979 (signed to press 29 Dec 79) pp 50-55

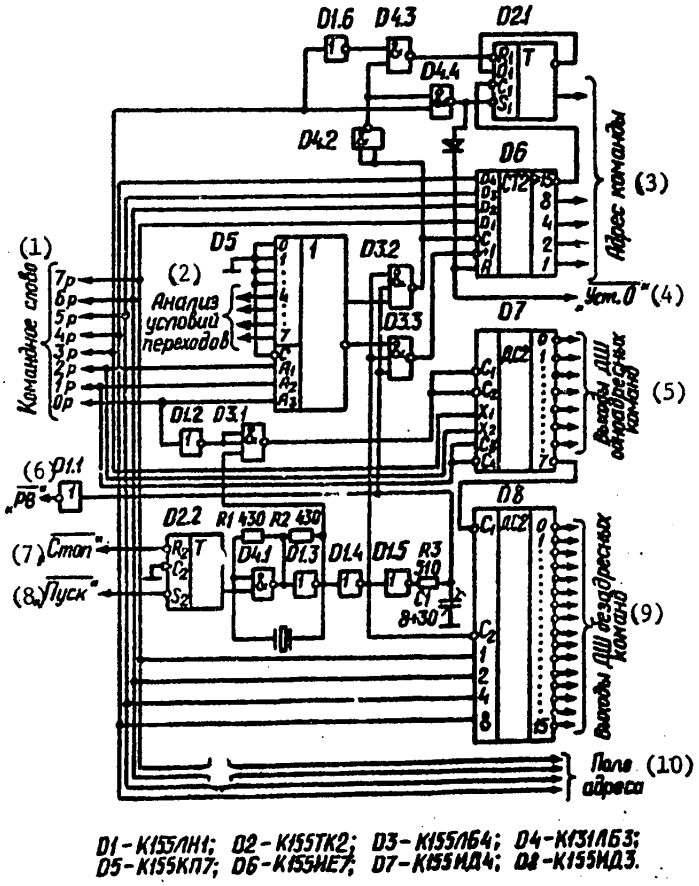
[Article by S. M. Krylov]

[Text] Much attention has been paid recently to problems of developing various systems for acquisition and processing of analog information based on microprocessors [2, 3, 5]. This is due not only to the high degree of integration and potential low price of microprocessor large-scale integrated circuits, but also to the capabilities offered the apparatus developer, namely: execution of various functions on the same equipment (universality) and programmed variation of these functions. At the same time, series digital microprocessors are ill suited to direct interaction with the analog portion of the data acquisition system because of the natural orientation of their instructions to processing digital information. Using such a microprocessor to control analog equipment entails developing special interfaces [1] and, as a rule, is rather inefficient. Therefore, the majority of analog-digital data processing systems are mediocre in interaction between the analog and digital portions, the analog-to-digital [ADC] and digital-to-analog [DAC] converters [3].

The system discussed in this article is one in which the functions of control of elementary analog operations and individual stages of A/D and D/A conversions have been transferred to a special control unit with a very simple structure, a nanoprocessor. One possible schematic implementation, made with standard K155 and K131 series TTL-SIS [transistor-transistor-logic medium scale integrated circuits], is shown in fig. 1.

The nanoprocessor contains a clock pulse generator (D4.1, D1.3), controlled by a start-stop flip-flop (D2.2), a five-bit programmed counter (D2.1, D6), a decoder of one-address operations (D7), a a decoder of addressless operations (D8) and a strobe shaper for the instruction counter (D5, D3.2, D3.3). There are three formats of instructions executed by the nanoprocessor: branch format (format attribute is a "1" in the zero bit of the instruction word), one-address instruction format (attribute is a "0" in the zero bit) and the addressless instruction format (attribute is the code "0111" in bits zero through three inclusive).

A feature of the scheme is the use of a multiplexer (D5) to analyze the conditions (attributes) of branches in branch instructions and generate the appropriate strobe



D1 - K155ЛН1; D2 - K155ТК2; D3 - K155ЛБ4; D4 - K131ЛБ3;
D5 - K155КП7; D6 - K155ИЕ7; D7 - K155ИД4; D8 - K155ИД3.

Fig. 1. Nanoprocessor

D1 - K155LN1 D2 - K155TK2 D3 - K155LB4 D4 - K131LB3 D5 - K155KP7
D6 - K155IYe7 D7 - K155ID4 D8 - K155ID3

Key:
1. instruction word
2. branch condition analysis
3. instruction address
4. "Ust. 0" [zero setting]
5. one-address instruction decoder outputs
6. $\overline{RV}$ - access authorization
7. stop
8. start
9. addressless instruction decoder outputs
10. address field

for the program counter (receiving the branch address or incrementing the counter readings by one). The branch operation code enters address inputs A1-A3 of multiplexer D5, in accordance with which one of the information inputs 4-7 is connected to its output. If the signal at this input equals a logical one, there will be generated at D3.2 a strobe for receiving the address of the branch (bits 3-7 in the instruction word) to the instruction counter D2.1-D6. Otherwise, there will be generated at 3.3 the strobe "add one to instruction counter," and "receiving the branch address" is selected in the adjustment by the regulator of the capacitance of C1.

The nanoprocessor instruction word length adopted is 8 bits, which with the 5-bit program counter permits using as program storage the standard K155 series of microcircuits with an organization of 32 eight-bit words: the K155RYe1, K155RYe3 or four K155RU2 circuits. Synchronization of their operation with the nanoprocessor cycle is effected by the signal "$\overline{RV}$" (access authorization). The nanoprocessor can operate directly with the outputs for readout of these microcircuits.

If required, the instruction word length can easily be extended, for example, to 12 bits, and the capacity of the program counter to 8 (for which a second K155IYe7 four-bit counter is included instead of the the flip-flop D2.1). The free outputs from the operation decoders provide the capability of generating instruction formats in accordance with the structure of an analog-digital system and requirements imposed on it.

Based on a similar processor, a multipurpose prototype system was developed for data acquisition, processing and conversion [6]. A simplified structural diagram of the system is shown in fig. 2. Besides the control nanoprocessor, the system contains storage for 32 eight-bit words, a four-bit TsAP (digital-to-analog converter), a programmable time counter (timer) and a three-decade register for the reading. The analog portion is a type set of elements used for

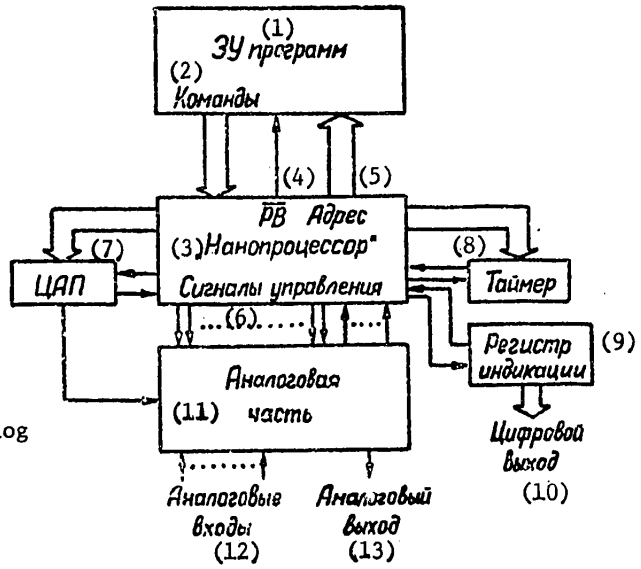


Fig. 2.

Key:
1. program storage
2. instructions
3. nanoprocessor
4. $\overline{RV}$ - access authorization
5. address
6. control signals
7. TsAP = DAC [digital-to-analog converter]
8. timer
9. reading register
10. digital output
11. analog portion
12. analog inputs
13. analog output

data acquisition and conversion [4]: analog multiplexers and demultiplexers, scaling operational amplifiers and analog storage elements.

The instruction system consists of 22 instructions in the three aforementioned formats, and the addressless format is used for individual switchings of the analog circuits in the system, control of the DAC register modes and the reading register (shift of the reading register by one bit or incrementing the register by one); the one-address format is used for loading the DAC register, the timer registers and the register for setting the transfer factor for the scaling operational amplifier. The number written to the appropriate register is placed as an immediate operand in the address field of the one-address format.

Branching instructions execute the unconditional branch operation as well as conditional branches on several features: end of timer operation, overflow of reading register and on the analog signal sign.

To demonstrate the capabilities of the system, a number of programs were written to process and convert data that implement the following functions:
1. "Time Counter." This program reads out time intervals from tens of microseconds to several hours and provides the capability of tying data processing to the real-time scale.
2. "Analog-to-Digital Conversion." This program generates 12-bit conversion code, using one 4-bit DAC, and both the depth of conversion and type (into binary or binary-decimal code) are varied by program facilities.
3. "Heteropolar Pulse Generator." This program generates at the analog output of the system heteropolar pulses, the amplitude of which is programmed, and the positive nad negative pulses can have a different amplitude.
4. "2.5-fold Frequency Increase." This program increases the frequency of repetition of square pulses coming into the system analog input 2.5-fold and outputs them at the analog output with the same amplitude.
5. "Complex Shape Pulse Generator." This program allows synthesizing a signal of essentially any shape by the method of output of a series of voltage levels.
6. "Automatic Frequency Meter." This program meters pulse repetition frequency with automatic selection of the best of four possible ranges.
7. "Direct Current Filter-Detector." This program converts an input signal into direct or pulsating voltage of one polarity; a constant signal passes through the system unchanged, but the higher the frequency of a signal of alternating polarity, the greater the reduction in effective value until the input signal is fully attenuated at the cutoff frequency.
8. "Metering of intervals between pulses of negative polarity, negative and positive polarity, as well as between pulses, the amplitude of which exceeds some threshold."
9. "Oscillating Frequency Generator." This program generates at the analog output signals of varying duty factor and duration. The nature of the variation is specified by program.

The length of any of the programs listed above does not exceed 32 instructions.

Thus, using the simple control unit (the nanoprocessor) in an analog-digital system for data acquisition, processing and conversion permits making fuller use of analog equipment and therefore increasing the flexibility (universality) of the system.

BIBLIOGRAPHY

1. (Weisberger), A., "Application of Microprocessors in Information Acquisition Systems," ELEKTRONIKA, No 18, 1974, p 36.

2. Konikov, A. I.; Piskulov, Ye. A. and Sobkin, B. L., "Analog-Digital LSI Circuits for Expanded Microprocessor Set," ELEKTRONNAYA PROMYSHLENNOST', No 4(58), 1977, p 90.

3. (Mattera), L., "Data Converters for Operation with Microprocessors," ELEKTRONIKA, No 18, 1977, p 22.

4. (Santucci), D., "Data Acquisition Systems," Part 1, ELEKTRONIKA, No 23, 1975, p 34, and Part 2, ELEKTRONIKA, No 24, 1975, p 51.

5. (Hetch), R., "Expanding the Functional Capabilities of a Multimeter when Using a Microprocessor," ELEKTRONIKA, No 19, 1976, p 35.

6. Krylov, S. M., "Specialized Control Microprocessor in Analog Information Processing System," "Sbornik trudov Kuybyshevskogo politekhnicheskogo instituta im. V. V. Kuybysheva" [Collection of Works of Kuybyshev Polytechnical Institute imeni V. V. Kuybyshev], Kuybyshev, 1978.

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APPLICATION OF HYBRID COMPUTER SYSTEM WITH DEVELOPED INTERNAL SOFTWARE TO NUCLEAR POWER PLANT SIMULATOR

Kiev ELEKTRONNOYE MODELIROVANIYE in Russian No 2, Mar-Apr 82 (manuscript received 23 Oct 81) pp 82-85

[Article by Candidate of Technical Sciences Alla Aleksandrovna Bal'va, junior scientific worker, and Doctor of Technical Sciences Viktor Dmitriyevich Samoylov, department head, both of the Institute of Problems of Simulation in Power Engineering, Ukrainian SSR Academy of Sciences, Kiev]

[Text] According to the program for development of nuclear power engineering in the USSR during the past five years, it was planned to put nuclear power plants with a total of 23,000-25,000 MW into operation. The need for safe, reliable and economic operation of nuclear reactors arises with the intensive development of this sector of the national economy.

It is known that the number of accidents at nuclear power plants through the fault of operating personnel comprises from 40 to 80 percent [1]; therefore, highly qualified servicing of the energy units is of primary importance. The problem of operator training is being solved successfully by organization of training centers to train operating personnel of AES equipped with simulators, i.e., with hardware for occupational training of the human operator and designed to form and improve occupational skills and knowledge required to control a man-machine system.

The following types of problems should be solved in simulators:

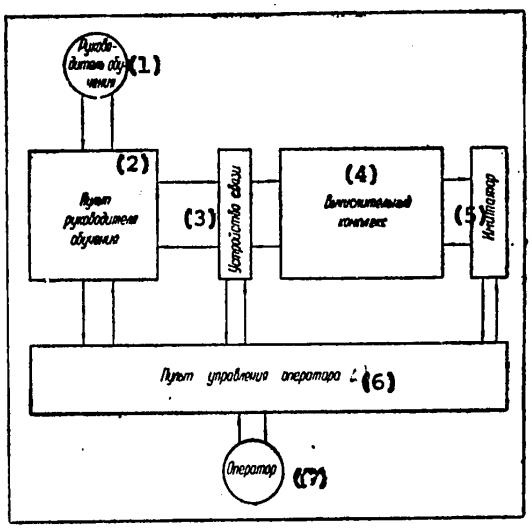
static problems without dynamic feedback (recognition of specific situsituations);

dynamic problems without feedback (evaluation of the correctness and completeness of the response of interlocking and shielding);

dynamic problems with feedback (processing control algorithms under different conditions, estimating the effect of control actions on the dynamics of a process and so on).

The block diagram of a simulator presented in the figure consists of an operator's control console that simulates the console and the unit control panel

of a nuclear power plant, a training supervisor's console designed to control the simulator and also to monitor and supervise the training process, a simulator unit, a computer complex and an integration device.



Key:
1. Training supervisor
2. Training supervisor's console
3. Communications device
4. Computer complex
5. Simulator
6. Operator's control console
7. Operator

The basis of the simulator is a computer complex that includes various computer devices (according to the type of information to be processed). The most important function of the computer complex is to reproduce in real time the operating dynamics of individual units of a nuclear power plant (which is described by systems of differential and algebraic equations) and mathematical and logic functions that reflect the response of the subsystems of the energy units to disturbing effects in any operating modes.

Analog type computers were used in the history of simulator design for power engineering to achieve high operational characteristics in the quality of real-time simulation. Simulators were designed primarily on the basis of computers of a given class as digital computers were developed and improved. However, achieving real time on a digital computer, as before, is a difficult task since it is related to investigations of the required composition of differential equations and selection of the method of solving them. Therefore, it is more feasible to use hybrid type computers complexes consisting of digital and analog computers.

When using hybrid computer systems, one must first distribute the task between the analog and digital computers so as to best utilize the advantages of computers of both types.

An analog computer is usually employed as the main computer, while a digital computer is employed as a control computer which changes the structure of the dynamic model and simulates the operating logic of the facility control system [2, 3].

Redistribution of the calculating functions between digital and analog computers is determined by the specific designation of the simulator. If there is no need for frequent changing of the dynamics of continuous processes, models of the main units are reproduced on an analog computer, while logic functions and storage functions are reproduced on a digital computer. If there is need for frequent changing of the type of installation, the simulation functions can be entrusted to a digital computer while fixed processes can be simulated on an analog computer.

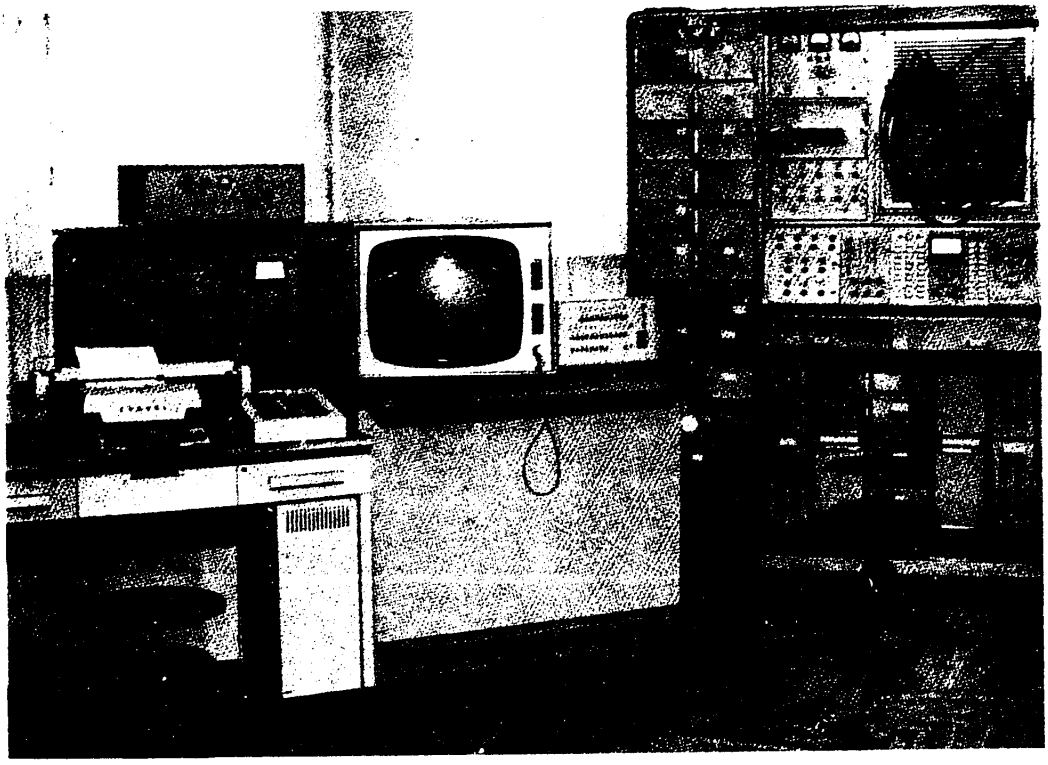
Let us consider the specific characteristics which analog and digital computers should meet for successful use of them in the computer complex of a simulator. These characteristics are as follows for an analog computer: reliability of the structurally realized model, capability of prolonged integration, permissibility of changing the structure of the model and developed parallel logic. Provision of real time by operating systems, the presence of a developed interface and large storage capacity should be inherent to digital computers.

Simulators both abroad and in our country, specifically a simulator to train operating personnel at the Novovoronezhskaya AES, are developed by the block diagram of the simulator presented in the figure. It should be noted that the initial conditions, modes and other operations are assigned in these simulators by flipping the corresponding toggle switches on the control console and the training supervisor's console. The modes which the training supervisor uses are determined beforehand and the set of control actions is fixed by a set of keys on the console.

During functioning of the simulator it becomes necessary to improve the simulation process, which is related to consideration of new models and modes of using them, modification of available models and introduction of new emergency modes. In this case a fixed configuration of the console and give set of actions on the model are ineffective.

One of the methods of achieving flexibility of interaction of the training supervisor with the complex simulator that provides modification and improvement of the control structure is a high-level problem-oriented language which the training supervisor can use to easily compile control programs and to provide a dialogue mode of interacting with the system.

Subsystems whose models should be reproduced on the simulator are used to solve systems of a large volume of equations that include algebraic, logic and differential equations. Real-time solution of these equations on a digital computer is difficult, while the use of analog devices leads to the need for structural realization of developed logic control devices of analog operating units. Highly efficient specialized devices, which reduce the calculating time with insignificant additional expenditures to develop them, can be developed to solve this problem.



GVS-2 Multiprocessor Hybrid Computer System With Developed Internal Software Designed By the Institute of Problems of Simulation and Power Engineering, Ukrainian SSR Academy of Sciences

The simplicity of rearranging the structure of models should be taken into account during development of simulators, which is provided by automatic switching and the presence of a convenient external language for communicating with the system.

The enumerated requirements can be met if a hybrid multiprocessor computer system with developed internal software based on a digital computer with structural interpretation of the external language is used as the computer complex of the simulator.

The overall diagram of a system which consists of a central language processor with structural interpretation of the external language that provides a dialogue mode of the user with the system, a set of problem-oriented processors which are included in its configuration as a function of the specific orientation of the system and a device for communicating with the system is considered in [4]. Problem-oriented processors can be serially produced analog computers and highly productive specialized processors for solving a specific class of problems (specifically, systems of algebraic equations). Problem-oriented processors are connected to the common bus of a digital computer. The structure of the system is hierarchical and a powerful digital computer can be connected at the upper level of the hierarchy to increase the productivity of the system. The use of this multiprocessor hybrid computer system yields the following distribution of the calculating capacities in the simulator. The training supervisor's console can be a central language processor that provides a dialogue mode of the training supervisor with the entire system. A central language processor, set of analog and digital problem-oriented processors and developed device for communicating with the system are used as the computer complex. If the volume of the equipment to be simulated in the simulator is high, the computer complex includes a digital computer of the upper level of the hierarchy.

The effectiveness of realizing the common algorithm in a GVS [hybrid computer system] is achieved by maximum parallelling of the calculating process provided that the individual fragments of the algorithm are reproduced by more suitable means: systems of differential equations on an analog processor and systems of algebraic equations on a digital problem-oriented processor. The central language processor implements the dialogue mode, coordinates fulfillment of the common algorithm and reproduces specific logic and calculating functions. Problem-oriented processors are the main computers of the system. Let us note the main advantages of a hybrid system of the given class with respect to using it in simulators.

The advantages of hybrid computer systems determined by the use of highly productive analog and digital problem-oriented processors are:

high equivalent speed and efficiency of performing such operations as adding, multiplication and integration that permit the use of real and accelerated time scales when solving problems on a simulator;

the capability of operationally composing models of the corresponding mathematical functions as a result of automatic switching and the simplicity of programming that simplify the process of simulator rearrangement;

the simplicity of connecting to real equipment that provides matching to nuclear power plant equipment.

The advantages of hybrid computer systems determined by use of a central language processor are:

a developed system of interpretation and as a result the capability of a dialogue mode and the presence of a high level of external and internal

languages that provide communication of the supervisor with the simulator equipment;

the presence of developed peripheral equipment that provides convenient display of the processes to be simulated;

high intelligence of the hybrid computer system achieved due to small material expenditures that permit the experiment to be conducted with low qualifications of the investigator in the field of programming;

the capability of simple expansion of the set of microprograms of the internal software that determine simple rearrangement of the simulator software;

changing of the set of "hybrid" operators that contribute to flexibility in problem orientation.

The computers used in hybrid computer systems, like the devices for communicating with the system, as not expensive.

An example of a hybrid computer system of the described class is the GVS-2 multiprocessor with developed internal software based on a digital computer with structural interpretation of the external language, designed at the Institute of Problems of Simulation in Power Engineering, Ukrainian SSR Academy of Sciences, and introduced successfully at many of the country's enterprises. An external view of the GVS-2 is shown in the photograph. The inventors of this system are V. D. Samoylov, V. V. Aristov, L. I. Tarasenko-Zelenaya, A. A. Bal'va, G. M. Vishnevaya, A. V. Zaranovskiy and others. The configuration of the system consists of a central processor with dialogue operating mode (digital computer of the MIR series), a set of problem-oriented processors (serially produced analog computers and a processor for solving systems of algebraic equations) and a device for communicating with the system. The system is oriented toward solution of real-time simulation problems with inclusion of real equipment, parametric optimization of dynamic facilities and identification and boundary-value problems and is designed to conduct experiments at scientific research organizations, in laboratories and at vuzes.

Let us present the main specifications of a multiprocessor system: The number of problem-oriented processors is up to eight, the composition of the digital computer is total, the input language of the system expanded by "hybrid" operators is Analitik, the operating mode of the computers of the system is autonomous, joint and semi-autonomous, the functioning of computers in the "system" mode is parallel and series, the number of interrupt channels is six, the number of program-accessible digital-analog conversion channels during simulation is two, the number of analog-digital conversion channels is eight, the number of independent timers is seven, the permissible simulation time is 0.1-999.9 seconds, the number of automatically set potentiometers is 64 and the number of channels for automatic control of the model structures is eight. Hybrid operators introduced into Analitik language permit automatic selection of the potentiometers of any of the problem-oriented processors, assignment of initial conditions, solution of systems of differential and algebraic equations,

taking the results of solutions, control of the structure of problem-oriented processors, conversion of the digital computer to subroutines on six interrupt channels, entry of any quantified functions written in the digital computer memory into problem-oriented processors through two channels continuously during simulation and enter up to eight functions from problem-oriented processors into the digital computer continuously during simulation.

The external language operators are divided into operators of "Set," "Simulation," "Interrogation" and "Verification" type.

Further development of multiprocessor hybrid systems of the given class is related to development of new and improvement of existing problem-oriented processors and development of an external language, programming system and peripheral devices of the system.

BIBILOGRAPHY

1. Klunin, Yu. A., N. G. Barykova, Z. K. Gribanov and A. S. Zisman, "Some Recommendations on Designing the Model of an Energy Unit Included in a Simulator," TEPLOENERGETIKA, No 6, 1976.

2. Malashinin, I. I. and I. I. Sidorova, "Trenazhery dlya operatorav AES" [Simulators for Operators of Nuclear Power Plants], Moscow, Atomizdat, 1979.

3. Yemel'yanov, I. Ya., A. I. Yefanov and L. V. Konstantinov, "Nauchno-tekhnicheskiye osnovy upravleniya yadernymi reaktorami" [Scientific and Technical Fundamentals of Nuclear Reactor Control], Moscow, Energoizdat, 1981.

4. Aristov, V. V., A. A. Bal'va, G. M. Vishnevaya et al, "Multiprocessor Hybrid Computer System with Developed Internal Software," in "Mnogoprotssornyye gibridnyye sistemi i algoritmy" [Multiprocessor Hybrid Systems and Algorithms], Kiev, Naukova dumka, 1976.

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CSO: 1863/150

UDC 681.33

SOME DESIGN PRINCIPLES OF SCALATOR COMPUTER DEVICES OF TIMER TYPE

Kiev ELEKTRONNOYE MODELIROVANIYE in Russian No 2, Mar-Apr 82 (manuscript received 20 Nov 80) pp 93-95

[Article by Candidate of Technical Sciences Vitaliy Feodos'yevich Bardachenko, chief of Computer Center, Kheml'nitskiy, Candidate of Technical Sciences Yuriy Vsevolodovich Korolev, laboratory head, Kiev Polytechnical Institute, and Design Engineer Ivan Isayevich Mitasov, Khmel'nitskiy]

[Text] The current state and prospects for development of high-speed computers and the feasibility of using hybrid computers in which machine variables are represented by proportional time intervals are analyzed in [1]. Parallel processing of these intervals permits one to achieve high total speed of calculating structures with simultaneous representation of variables. However, the time intervals proportional to independent variables are formed on digital counting structures by interrogation of the corresponding counters by timing frequency generator pulses. This leads to the need to develop complex multicounter structures, which is related to an increase of the equipment required and to the complexity of the system.

Parallelling of the calculating process is most easily accomplished during calculations using scalator computer devices that perform the binary operation of scalar multiplication of N-dimensional vectors:

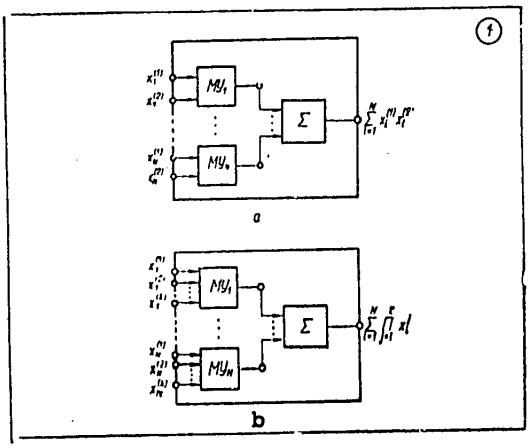
$$X_1 \cdot X_2 = (x_1^{(1)}, \ldots, x_N^{(1)}) \cdot (x_1^{(2)}, \ldots, x_N^{(2)}) = \sum_{i=1}^{N} x_i^{(1)} x_i^{(2)}. \quad (1)$$

It is necessary in this case to realize a group algebraic operation for finding the sum of pair products of the components of multidimensional vectors $x_i^{(1)}$ and $x_i^{(2)}$ by means of simultaneously operating adding and multiplier units. The design principles of digital scalators are described, for example, in [2-4].

The design principles of timer type hybrid scalators, in which the variables are resistances R of capacitance C, dependent on input variables $x_i^{(1)}$ and $x_i^{(2)}$, are considered in the given article. These scalators have been called timer devices by analogy with timers in which RC circuits are used as the time-giving components.

The principle of time-pulse conversion of the constant time of an RC circuit to digital code, where the RC circuit is used as an analog multiplier circuit whose time constant is proportional to the product of parameters R and C, is described in a hybrid multiplier device in [5, 6].

The controlled RC circuit with time-code converter is an elementary binary converter that operates the scalator sequentially in time, which will have digital input and output upon realization of R and C in the form of digital control resistor and capacitor. Connection of these parallel-operating elementary multiplier devices to calculate operation (1) into a homogeneous calculating structure permits one to find the sum of pair products $x_i^{(1)}x_i^{(2)}$ during execution of a single i-th multiplication operation. A block diagram of this N-dimensional binary scalator is presented in Figure 1, a.



Block Diagram of N-Dimensional Binary (a) and K-nary (b) Scalators

The functional principles, principles of structural realization and errors of binary timer scalators are described, for example, in [6-8], but there is a need to determine not only the binary, but also the K-nary (K-place) operation of the scalar product of vectors with real components. Thus, to find the K-nary operation of the scalar product of vectors $X_1 \ldots X_K$, expression (1) will have the form

$$X_1 \ldots X_k = (x_1^{(1)}, \ldots, x_N^{(1)}) \ldots (x_1^{(k)}, \ldots, x_N^{(k)}) = \\ = \sum_{i=1}^{N} x_i^{(1)} x_i^{(2)} \ldots x_i^{(k)} = \sum_{i=1}^{N} \prod_{j=1}^{k} x_i^{(j)}. \qquad (2)$$

Calculation of the sum of K-nary products by both digital and analog computer equipment is rather complex and it is practically impossible in parallel form with large values of K.

The problem of creating a simple hybrid timer scalator to calculate K-nary operations of the scalar product of vectors is postulated in this article. At the same time the division operation in timer scalators that use time-giving RC-circuits is carried out. A block diagram of an N-dimensional K-nary scalator is shown in Figure 1, b.

Functionally, a K-nary scalator is a hybrid computing structure with homogeneous analog calculating medium of timer type. The element of this medium is shown in Figure 2, a. Two control RC-circuits (R_1C_1 and R_2C_2) with discharge keys are exponential voltage generators (GEN) and the analog storage device (AZU) is strobed and is used to shape the reference voltage on a comparator. The input and output variables of the component are time intervals, which permits direct connection of components, forming a calculating medium homogeneous in structure. A fragment of this medium is shown in Figure 2, b. The first exponential voltage generator of the first component and the timer that counts interval t_0 are started upon a signal of the timing oscillator (GT). A signal from the timer output starts the second exponential voltage generator and the analog storage device of the first component. The instantaneous fixed value of exponential voltage is fed from the output of the first exponential voltage generator to the comparator input and is compared to the current exponential voltage of the output of the second generator. The condition is fulfilled at the moment the voltages are equal

$$U_{on_1} = E\left[1 - \exp - \left(\frac{t_0}{R_1C_1}\right)\right] = E\left[1 - \exp\left(-\frac{t_1}{R_2C_2}\right)\right], \quad (3)$$

hence

$$t_1 = \frac{R_2C_2}{R_1C_1} t_0 = \frac{\tau_2}{\tau_1} t_0. \quad (4)$$

At the same time the timer signal starts the second component through input 1 (Vkh 1), input 2 (Vkh 2) of which is started by a signal from the output of the first component. A similar equality is also valid for the second component

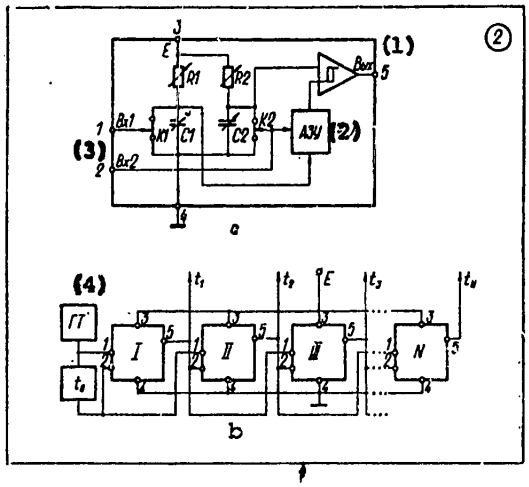
$$t_2 = \frac{R_4C_4}{R_3C_3} t_1 = \frac{\tau_4}{\tau_3} t_1, \quad (5)$$

Substituting (4) into (5), we have

$$t_2 = \frac{\tau_2 \cdot \tau_4}{\tau_1 \cdot \tau_3} t_0. \quad (6)$$

Relating the given arguments for the entire circuit of N series-connected components, we find

$$t_N = \frac{\tau_2}{\tau_1} \cdot \frac{\tau_4}{\tau_3} \cdots \frac{\tau_{2N}}{\tau_{2N-1}} t_0. \quad (7)$$



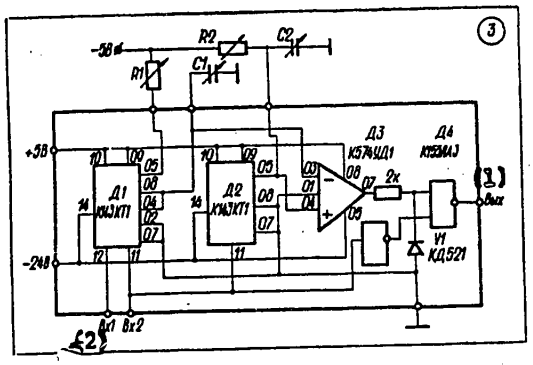
Functional Diagram of Component of Homogeneous Analog Calculating Medium of Timer Type (a) and a Fragment of It (b)

Key:
1. Output
2. Analog storage device
3. Input
4. Timing oscillator

The component shown in Figure 2, a can be used as a timer that controls interval t_0 provided that the analog storage device is replaced by a direct reference voltage source. In the general case the described component of a homogeneous medium is a functional timer that performs multiplication-division operations, which permits one to characterize scalator computing devices of the proposed type as timer devices.

A schematic diagram of the component is shown in Figure 3, in which an MOP [metal oxide semiconductor]--keys of 143 series--and operating amplifier K574UD1 having $R_{vkh} \geq 100$ Gohms are used. The high reverse resistances of the keys and the input impedance of the comparator made it possible to realize an analog storage device using a single capacitor C_1 that simulatneously performs the calculating function and one disconnect key (half of microcircuit D1). The comparator is power asymmetrically, due to which the number of power supply voltage sources could be cut in half and matching of the operating amplifier of the comparator to the logic circuit could be simplified to the maximum. The inputs of the component are potential and the signal fed to Vkh 2 is delayed by time t_0 with respect to Vkh 1.

It is easy to see that connection of the components (Figure 2, a) by the diagram shown in Figure 2, b permits one to construct a homogeneous calculating medium both in two-dimensional (plane) and three-dimensional (volumetric) version.



Schematic Diagram of Component of Homogeneous Analog Medium of Timer Type

Key:
1. Output
2. Input

The inputs and outputs of the elementary calculating units I, II,..., N can be commutated one after the other in a similar homogeneous calculating medium according to the given configuration required to make calculations by specific formula functions.

As already noted, the operating parameter (machine variable) of the given homogeneous calculating medium is time t. This permits rather simple connection of a similar homogeneous analog calculating medium to digital computing devices without using complex analog-digital converters and also permits one to create a hybrid processor, the role of the analog part of which is performed by the described homogeneous calculating medium, while the role of the digital part is performed by known digital processor components. The capability of realizing the component of this medium in the microelectronic conversion permits one to hope that a similar homogeneous medium may be an analog microprocessor with the corresponding circuit engineering and technological development. Fundamental connection of digital and the described analog microprocessors permits one to create qualitatively new microcomputers of hybrid type that combine the advantages of both digital and analog computer equipment.

One should especially note the capability of organizing the calculating process in any part of the processor on a specific group of components of a homogeneous calculating medium, which permits one to solve a number of independent problems simultaneously and mutually independently. If some components fail, the functions and calculating capabilities of the processor designed on its basis are essentially retained since the remaining components are operable, which determines the high viability of computer equipment of this type.

Taking the extensive use and simplicity of transmission of impulse duration modulated signals or the time intervals in the communications devices into account, one can connect spatially distributed homogeneous scalator timer processors into a unified computer network, which permits a practically unlimited increase of the calculating capacities of this network.

Thus, the given design principles of scalar computer devices of the timer type may serve as the basis to develop specialized analog and hybrid processors and microprocessors with homogeneous structure.

BIBLIOGRAPHY

1. Pukhov, G. Ye., V. V. Vail'yev, V. F. Yefdokimov, A. F. Katkov and V. P. Romantsov, "Promising Directions for Development of High-Speed Computer Equipment," MATEMATICHESKOYE MODELIROVANIYE I TEORIYA ELEKTRICHESKIKH TSEPEY, No 10, 1973.

2. Pukhov, G. Ye., "Structural-Analog Digital Computer Systems," ELEKTRONIKA I MODELIROVANIYE, No 7, 1975.

3. Pukhov, G. Ye., "Calculating Structures of Integrating Adders of Pair Products," ELEKTRONIKA I MODELIROVANIYE, No 1, 1974.

4. Stasyuk, A. I. and V. P. Yeremenko, "Using Processors of Group Operations to Solve Systems of Algebraic Equations," VYCHISLITEL'NAYA TEKHNIKA I MODELIROVANIYE SLOZHNYKH SISTEM V GRAZHDANSKOY AVIATSII, No 3, 1977.

5. Bardachenko, V. F., A. K. Kovtun and A. N. Shkuro, "Digital Multiplication-Division Device," IZMERITEL'NAYA TEKHNIKA, No 10, 1973.

6. Bardachenko, V. F., Yu. V. Korolev and V. V. Nester, "Hybrid Calculating Media Based on Time-Pulsed Scalators," in "Tezisy dokladov IV Vsesoyuznoy konferentsii 'Odnorodnyye vychislitel'nyye sistemy i sredy'" [Report Topics of Fourth All-Union Conference Homogeneous Computers Systems and Media], Vol 2, Kiev, 1975.

7. Bardachenko, V. F. and Yu. V. Korolev, "Analysis and Optimization of the Accuracy of Time-Pulse Multiplier-Division Devices," ELEKTRONIKA I MODELIROVANIYE, No 9, 1975.

8. Bardachenko, V. F., Yu. V. Korolev, I. I. Mitasov and V. V. Nester, "Accuracy Characteristics of Hybrid Time-Pulse Multiplier-Division Device With Exponential Scanning," ELEKTRONIKA I MODELIROVANIYE, No 10, 1975.

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SOFTWARE

UDC 681.3.068

PROGRAM MODULE PACK FOR CONFIGURATION OF MULTIPROBLEM REAL-TIME DIALOGUE SYSTEMS FOR M-7000 of ASVT-M AND SM-1/SM-2 OF SM EVM

Novosibirsk AVTOMETRIYA in Russian No 1, Jan-Feb 82 (manuscript received 2 Jun 80, in final form 13 Oct 80) pp 102-104

[Article by L. A. Akol'tseva, E. U. Knyazhanskiy, V. S. Naumova and P. A. Sadymak, Severodonetsk, Voroshilovgradskaya Oblast]

[Excerpt] Introduction. The program module pack for configuration of multiproblem real-time dialogue systems (DMSRV) is a complex of adjustable and permanent program modules, from which different versions of multiproblem real-time dialogue systems adjusted for a specific UVK [control computer complex] are developed by generation and configuration.

The DMSRV is designed to execute in real time in the interpretation modes programs compiled in the dialogue mode in BASIC-RV language.

BASIC-RV language is an expanded version of BASIC language [1]. The main expansions are as follows: the external subroutine call operator, the time and external events problem control operators, information input-output operations from facility communication devices, bit processing operations, expanded information input-output operators from devices and operators for working with files.

The typical problems solved by DMSRV is information gathering and processing in production process and scientific experiment control systems and also control of production or scientific (laboratory) equipment.

The following minimum configuration of equipment is required for operation of the DMSRV: M-7000, SM-1P and SM-2P processor, internal storage with capacity of 16 K words, a timer and device for keyboard entry and display of alphanumeric information.

Program structure. The program designed for execution in the DMSRV consists of one or several subroutines (problems).

The problem is a sequence of BASIC operators that carry out some final action, for example, interrogration and processing of a specific number of analog signals. Priorities, according to which fulfillment of the problems is controlled,

are assigned to them. The problems can be related to specific external events (for example, interruptions due to initiative signal sources), upon entry of which they are started for fulfillment or can be started for fulfillment at the onset of specific moments of time. BASIC-RV language offers the user the capability of controlling the problems by means of the corresponding operators.

The conditions for starting the task and their priorities are established during fulfillment and can be varied dynamically. An example of a problem that carries out information entry from sensors and registration of inforamtion is presented below.

```
1000 START (1000, 10)          --start of problem every 10 seconds;
1010  SETP (1000,60)           --priority of problem 60;
1020 AISQ (10, C(1), V(1), S)  --entry of information from 10 sensors;

1030 FOR I = 1 TO 10
1040 PRINT V(I);
1050 NEXT I                    --printout of values used.
1060 RETURN
```


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ABSTRACTS OF ARTICLES IN JOURNAL 'PROGRAMMING', JANUARY-FEBRUARY 1982

Moscow PROGRAMMIROVANIYE in Russian No 1, Jan-Feb 82 pp 95-96

UDC 681.3

ROLE OF A. A. LYAPUNOV IN PROGRAMMING

[Abstract of article by Kitov, A. I., Krinitskiy, N. A. and Podlovchenko, R.I.]

[Text] The article is devoted to the memory of A. A. Lyapunov and the basic phases of his creativity and his role in establishment of programming in the USSR are considered.

UDC 519.1

MODELS OF PROGRAMS ON A STRUCTURED BASIS

[Abstract of article by Podlovchenko, R. I.]

[Text] The basis on which program models are constructed is outlined. The class of semantic models on a structured basis is described. The sufficient conditions are found so that the model of the described class be a semi-group model.

UDC 681.3.323

INVESTIGATING THE EQUIVALENCE OF FLOW CHARTS BY THE THEORY OF FUNCTIONAL CIRCUITS

[Abstract of article by Fal'k, V. N.]

[Text] One approach to proof of the functional equivalence of standard flow charts, based on translation of flow charts to the language of functional circuits formalized within the framework of first-order theory with equality, is considered.

UDC 681.3.067

TABULAR MEMORY

[Abstract of article by Vel'bitskiy, I. V., Netesin, I. Ye. and Sholmov, L. I.]

[Text] A new structure of data--the tabular memory--is suggested. The problem of compact arrangement of a set of hatchure-tables whose dimensions are previously unknown in a memory is solved on its basis.

UDC 681.324.066.013

CONTROLLING ACCESS TO A COMPLEX RESOURCE BY MEANS OF THE YES OPERATING SYSTEM

[Abstract of article by Meleshchuk, S. B., Nedumov, A. N. and Tolstyakov, A. V.]

[Text] A system that includes groups of resources jointly used by parallel processes is considered. A method is suggested for organization of the dispatcher of complex resources in the operating system of the Unified Computer System that does not require modification of SVC programs when fulfilling processes in different sections.

UDC 681.3.06:51

ONE APPROACH TO THE PROBLEM OF DEVELOPING SYSTEMS SUPPORT OF PROGRAM PACKS FOR PROBLEMS OF COMPUTER PHYSICS

[Abstract of article by Koryagin, D. A.]

[Text] One of the approaches to the problem of developing systems support of program packs is discussed in the article.

UDC 62-501.72:681.3

USE OF FORTRAN LANGUAGE TO MODEL ANALOG SYSTEMS ON DIGITAL COMPUTERS

[Abstract of article by Dorri, M. Kh. and Klimachev, S. N.]

[Text] A brief survey of papers devoted to solution of the problem of modelling analog processes on a computer is given and the Radius-2 system is described. Procedures are described that permit one to avoid the disadvantages typical for Fortran modelling programs.

UDC 681.3.06

AUTOMATION OF BATCH PROCESSING OF PROBLEMS IN THE DISK OPERATING SYSTEM OF THE UNIFIED COMPUTER SYSTEM

[Abstractof article by Yegorov, I. V. and Muzychkin, P. A.]

[Text] A complex of programs that store assignments in a library, fulfill any assignment or chains of assignments, utilize parameters, correct assignments and also use copying and retrieval software is described. Primary generation is linked to any type of disk carriers and does not depend on the version of the disk operating system.

UDC 681.3.06

MINIMIZATION OF STACK LENGTH IN CALCULATION OF EXPRESSIONS

[Abstract of article by Ivanov, A. V.]

[Text] An algorithm for translation of expressions that minimizes the length of the stack used for calculations is described.

UDC 681.142

GENERAL-PURPOSE OBJECT LANGUAGE UNCODE

[Abstract of article by Rau, O. I.]

[Text] The universal object language Uncode, which is an internal language of the translating complex IZhIKA, oriented toward a broad class of computers, is described.

UDC 518.5

MAIN CHARACTERISTICS OF INPUT LANGUAGE AND IMPLEMENTATION OF SPT SUPER

[Abstract of article by Serebryakov, V. A.]

[Text] The main characteristics of the input language and implementation of SPT SUPER are considered. The syntax of the main constructions of the language is presented in BNF. Algorithms for implementation of calculation of global and structural attributes and for organization of memory control during calculation of attributes are outlined.

UDC 681.142:7

REALIZATION OF NONMONOTONIC ARGUMENTS

[Abstract of article by Bukhshtab, Yu. A., Kamynin, S. S. and Lyubimskiy, E. Z.]

[Text] The problem of designing deductive systems that have the capability of retrieving facts, relying not only on the presence but also the absence of the

corresponding information in the data base, is considered. A method is described that is used for realization of this nonmonotonic retrieval in the "QUESTION-ANSWER" system.

UDC 681.3.06

SYSTEM FOR INTRODUCTION OF NEW TYPES OF DATA INTO FORTRAN

[Abstract of article by Babayev, I. O.]

[Text] The basic features of the FP/FPG system that is called on to significantly facilitate work in development of translating facilities to expand Fortran with new types of data are described. The capability of using this system to support the concept of abstract types of data in Fortran language is considered.

6521
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UDC 519.68

SOFTWARE PACKAGES: METHODS AND DEVELOPMENTS

Novosibirsk PAKETY PRIKLADNYKH PROGRAMM: METODY I RAZRABOTKI in Russian 1981 (signed to press 10 Aug 81) pp 2-4, 219-223

[Annotation, editors' comments and abstracts from book "Software Packages: Methods and Developments", edited by Vladimir Mefod'yevich Matrosov and Oleg Georgiyevich Divakov, Irkutsk Computer Center, Siberian Branch of USSR Academy of Sciences, Izdatel'stvo "Nauka", 4450 copies, 223 pages]

[Text] This is a collection of articles on the technology of solving problems at collective-use computer centers, based on software packages (PPP). Described are software packages for this technology oriented to mathematical methods applied in various stages of research and those oriented to specific subject areas. Described are the purpose of specific packages, methods used in them and some software implementation.

This book is of interest to application software developers.

From the Editors

This collection describes the complex of software packages developed at the Irkutsk Scientific Center of the USSR Academy of Sciences, Siberian Branch, and certain organizations cooperating with it. It also deals with the technology of solving scientific problems at collective-use computer centers (VTs KP). Discussed is the technology based on a system of packages oriented to mathematical and cybernetic methods used in all basic stages of research, beginning with computer data input, construction of a mathematical model of the research object, formalization of the problem statement, study of the existence of and deriving the numerical solution to the problem, analysis of the properties of the derived solution, such as stability, invariance and others, and ending with making the decision on the direction of further research. These stages and their order are dictated by the methodology of systems research. This technology affords a high degree of problem research automation.

Presented in the articles in the first section of this collection is the approach to planning the computing process in packages and construction of a system that implements the technology of simulation and optimization of finite-dimensional systems.

Described in the second section are the main base packages in this technology, oriented to methods, and considerable attention in them is paid to these methods. The section begins with an article dealing with speech signal processing methods for computer input and recognition. A major stage in research is the construction of the mathematical model for the system to be studied. Presented in the subsequent articles are the approach to automating design of mathematical models, the information system for selection of the description of the mathematical model by features and a system of programs for deriving differential equations of the motion of certain mechanical systems in the second type of Lagrange form and isolating and analyzing their stationary solutions. Described are certain aspects of the procedures for designing a mathematical model of the research object which is the basis for the statement of the mathematical research problem and the algorithms for the packages intended for finding numerical solutions to optimization problems of the linear programming and optimal control types. A number of articles deal with packages for numerical solution of boundary problems for ordinary differential equations. Described in the latter articles in the section are the concluding stages of research or its iteration in the final iteration process of problem research. Described are a package intended for analysis of dynamic properties of a system or the solutions found for it (the package algorithm is based on the method of Lyapunov vector functions); a decision-making package oriented to the method of generating additional requirements, decision rules and criteria used to evaluate solutions obtained and to selection of the best decision; and an interactive computer-aided design system for complex systems by the criterion of reliability.

Articles in the third section of the collection cover packages oriented to specific subject areas of applications. Discussed are packages for computer-aided design of ground-effect machines. Described are software and computer systems for optimizing the structure of the USSR unified electric power system, complex thermal power facilities and multicircuit hydraulic systems. Finally, problems of developing a subsystem for operational planning of vehicle transportation in construction are discussed.

Included in the collection are articles discussed at the 2nd Siberian School for Young Scientists and Specialists on the Technology of Developing Software Packages held in July 1979 and which reflect the status of developments at that time.

V. M. Matrosov and O. G. Divakov

ABSTRACTS

UDC 681.3.06

THEORY OF PLANNING COMPUTER PROCESS IN SOFTWARE PACKAGES

[Abstract of article by G. A. Oparin]

[Text] Mathematical modeling method is used to perform theoretical research on the problem of planning the computational process in software packages organized on the modular principle. Introduced are definitions of a complex, problem in a complex and solving a problem in a complex. Solved for a static complex are the problems of existence, uniqueness and structural design of solving problems. Questions associated with program implementation of the scheduler are discussed. Method is given for solving a problem in a static complex. Figs. 1, bibl. of 9 titles.

UDC 519.68 : 007.51

TECHNOLOGY OF MODELING AND OPTIMIZING COMPLEX SYSTEMS

[Abstract of article by V. M. Matrosov, S. N. Vasil'yev, O. G. Divakov and A. I. Tyatyushkin]

[Text] An approach is suggested for designing an interactive system for automating scientific research. The system contains modules for designing the mathematical model of the research problem, stating the mathematical optimization problem, finding the numerical solution to the problem, investigating the properties of the derived solution, and making the decision on the direction of further research. The system is described at the level of algorithms and mathematical methods. Figs. 3, bibl. of 17 titles.

UDC 681.3.06 + 62-506.001.57

SOFTWARE PACKAGE FOR SIMULATING PREPROCESSING METHODS IN SPEECH RECOGNITION SYSTEMS

[Abstract of article by S. L. Lidin, A. I. Yegorov and Yu. D. Savitskiy]

[Text] Described is software for checking serviceability and optimizing various preprocessing methods in automatic pattern recognition systems by numerical experiment based on an arbitrary amount of acoustic information. Figs. 2, bibl. of 6.

UDC 919.68 : 007.52

INFORMATION SYSTEM FOR SELECTING AND OBTAINING DESCRIPTIONS OF MATHEMATICAL MODELS

[Abstract of article by M. A. Novikov]

[Text] Discussed are problems in automating simulation of dynamic processes and phenomena. Based on classification of known dynamic systems, an algorithm is compiled to obtain descriptions of models which has been implemented on the EVM-6 in the form of a program complex. Figs. 5, bibl. of 5 titles.

UDC 519.68 : 007.51

APPROACH TO AUTOMATING DESIGN OF MATHEMATICAL MODELS

[Abstract of article by O. G. Divakov, V. A. Kuz'min, T. I. Mad'yarov and Yu. V. Shurov]

[Text] The approach is based on a description of mathematical relations in the language of predicates which allows the user to conveniently describe them in computer memory. The mathematical relation is constructed in stages: statement of problems by the user in text form in a restricted natural language, syntactic and semantic analysis of the text to identify the name of the regularity being modeled, and design of the mathematical model. Figs. 4, bibl. of 16 titles.

UDC 531.011 : 519.68

SOFTWARE PACKAGE FOR ANALYSIS OF STATIONARY MOTIONS OF MECHANICAL SYSTEMS

[Abstract of article by M. V. Pochtarenko]

[Text] Described are a system of analytic computations for solving problems of general mechanics on the BESM-6 computer and a software package for analyzing stationary motions of mechanical systems. In the first part, system capabilities for symbolic conversions are discussed, a class of expressions on which manipulations are performed is singled out and features of implementation are investigated. In the second part, discussed are the main problems solved by the software package and its structure and principles of organization. Examples are given. Results are compared with the known. Figs. 2, bibl. of 15 titles.

UDC 519.95

OPTIMIZATION PACKAGE LINEAR PROGRAMMING ALGORITHMS

[Abstract of article by A. I. Zholudev and A. I. Tyatyushkin]

[Text] Discussed are computational schemes of two linear programming methods: adaptive and reference which allow use of apriori (expert) information on problem solving. Algorithms for these methods and results of numerical experiments are given. Table 1, bibl. of 3 titles.

UDC 62.50

THEORETICAL PRINCIPLES OF SOFTWARE PACKAGE FOR IMPROVING CONDITIONS AND LOCAL SYNTHESIS OF CONTROL

[Abstract of article by V. I. Gurman, I. V. Rasina, V. A. Baturin, A. A. Onkhotoyev, Ye. V. Danilina and Ye. Yu. Baturina]

[Text] Discussed is the theoretical basis of a software package designed to solve optimal control problems. It is the Krotov theory of sufficient conditions of optimality and the approximation of equations of the Bellman method accurate to small values of the second order inclusively, on the basis of which algorithms are suggested to search for optimal control and approximated local synthesis. The package also includes procedures for output of calculation results in graphic and cartographic form. Figs. 5, bibl. of 9 titles.

UDC 681.142.2

APPROACH TO DESIGN OF SOFTWARE PACKAGE FOR NUMERICAL INTEGRATION OF BOUNDARY PROBLEMS FOR A SYSTEM OF ORDINARY DIFFERENTIAL EQUATIONS

[Abstract of article by A. A. Loginov]

[Text] Described are a class of boundary problems solved by the package and a set of methods of numerical integration. Presented are requirements for package, modes of its use and service capabilities. The package is implemented in FORTRAN. The

input language is also FORTRAN, supplemented by a statement for the problem statement, which consists of problem-oriented sentences. Figs. 1, bibl. of 9 titles.

UDC 517.938 + 51.621.391

SOFTWARE PACKAGE FOR INFERENCE BY LYAPUNOV'S THEOREM OF METHOD OF VECTOR FUNCTIONS

[Abstract of article by V. M. Matrosov, S. N. Vasil'yev, V. G. Karatuyev, Ye. A. Sumenkov and S. A. Yadykin]

[Text] Discussed are questions associated with design of software package for inference by Lyapunov's theorem of method of vector functions. Described are architecture of the package, function of its basic modules, the system part and the information retrieval module. The package is designed for investigation of various kinds of dynamic properties and is oriented to a broad range of specialists in system dynamics and control theory. Figs. 4, table 1, bibl. of 9 titles.

UDC 62-50 : 007 : 65

DESIGN OF SOFTWARE PACKAGE FOR MAKING DECISIONS

[Abstract of article by S. N. Vasil'yev and A. P. Seledkin]

[Text] Discussed are questions associated with designing a software package for making decisions: classification of decision-making problems and apriori information on preferences of LPR [person making the decision], algorithmic filling and package structure. Figs. 2, bibl. of 16 titles.

UDC 62-192

INTERACTIVE COMPUTER-AIDED DESIGN SYSTEM FOR COMPLEX SYSTEMS BY RELIABILITY CRITERION

[Abstract of article by Yu. V. Bondarchuk, A. F. Voloshin and Yu. M. Pozdnyakov]

[Text] This interactive computer-aided design system (SAPR) implements selection of the element base for complex control systems by the reliability criterion and technical and economic indicators for designing control systems for flying vehicles on the YeS-1033. The main decision algorithms are based on the methodology of sequential analysis of alternatives. A scheme for modular design of the computer-aided design system is given and modes of its functioning are described. Figs. 1, bibl. of 10 titles.

UDC 681.142.2 : 532.501.32

MODULAR SYSTEM FOR SOLVING PROBLEMS IN AERODYNAMICS AND DYNAMICS OF FLIGHT OF FLYING VEHICLES BY ASYMPTOTIC METHODS

[Abstract of article by A. N. Panchenkov, Yu. F. Orlov, G. I. Antoshkina, M. N. Borisyuk, Yu. I. Laptev, V. D. Mishchenko and R. Yu. Shlaustas]

[Text] This package is designed for investigating aerodynamic coefficients and the lift/drag ratio of lift complexes and the LA [flying vehicle] as a whole during its motion close to the fluid boundary; fits and criteria of static stability during motion in the stationary mode, determinate flight dynamics, investigation of amplitude-frequency characteristics of apparatus; optimization of the basic lift complex and selection of parameters for design schemes for flying vehicles. Package structure is a combination of program modules and a control program. The package is intended for operation on the BESM-6 computer working with standard software; base language of the package is FORTRAN. Figs. 1, bibl. of 15 titles.

UDC 621.311.161 : 681.3 : 519.83

SOYUZ COMPLEX FOR OPTIMIZING STRUCTURE OF USSR UNIFIED ELECTRIC POWER SYSTEM: ORGANIZATION STRUCTURE AND PRINCIPLES

[Abstract of article by L. A. Ivankova and V. V. Trufanov]

[Text] Described is the program and information complex that implements on the BESM-6 computer an optimization linearized model of the YeEES [Unified Electric Power System], intended for selecting a promising structure of generating capacity by equipment types taking throughput of intersystem links into account. Given are the basic principles of organization of the complex and its information base, the scheme for its design and functioning modes. Characteristics of the method of auxiliary functions, used to solve problem of large dimension, and features of its implementation in the complex are given. Questions of its effective application are discussed. Analysis of computational feature of the method is made. Some recommendations on its use are given. Figs. 2, bibl. of 8 titles.

UDC 621.311.161 : 681.3.519.83

SOYUZ COMPLEX FOR OPTIMIZING STRUCTURE OF USSR UNIFIED ELECTRIC POWER SYSTEM: INFORMATION PROVISIONING AND MODES OF USE

[Abstract of article by A. A. Granovskiy, V. R. Takayshvili and V. V. Trufanov]

[Text] Described are principles of organizarion of the information base and its software in the Soyuz complex, which makes use of the LBD-6 and DIMON as the base systems for collective use. Discussed are questions of planning the storage budget with long-term computations of problems of large dimension, organization of modes of operation of complex and its subsystems. Described is the interactive monitor and features of its implementation in the complex applicable to these systems. Figs. 1, table 1, bibl. of 5 titles.

UDC 681.14

SOSNA PROGRAM AND COMPUTING COMPLEX AS TOOL FOR IMPLEMENTATION AND INVESTIGATION OF ALGORITHMS FOR OPTIMAL SYNTHESIS OF MULTISTREAM HYDRAULIC SYSTEMS

[Abstract of article by A. V. Khramov]

[Text] Discussed are the mathematical statement of the general problem of optimal synthesis of multistream hydraulic systems and the program-computing complex

intended for realization and investigation of the stated problem. Functional content and features of the program-computing complex are given. Discussed are capabilities of interrupting computation upon efflux and preservation of results of optimization upon random failure by computer. Figs. 2, bibl. of 8 titles.

UDC 0007 : 51 : 681.3

METHODOLOGY OF DESIGNING SOFTWARE PACKAGE FOR SUBSYSTEM OF OPERATIONAL PLANNING OF VEHICLE TRANSPORTATION IN CONSTRUCTION

[Abstract of article by B. B. Bliznyukov, I. M. Guterman and V. I. Chumakov]

[Text] A description is given of software being developed for a subsystem of operational planning for vehicle transportation in construction in the form of a software package (PPP-OPAS). The purpose of this subsystem is to automate the generation of interrelated daily shift schedules for shipment, transportation and receiving of construction freight (primarily prefabricated reinforced concrete items). Discussed are requirements for the PPP-OPAS, its structure and functions, and certain questions on package development technology. FIGS. 1, bibl. of 4.

UDC 519.685

DEVELOPMENT OF INTERACTIVE OPTIMIZATION SYSTEM FOR DESIGN OF THERMAL POWER FACILITIES

[Abstract of article by S. V. Avrutik]

[Text] Existing practice of designing energy facilities is a very complex multilevel system of control and organization of generation processes. Discussed in this work are the basic principles and approaches to automating such systems based on using interactive (dialogue) and batch modes of information processing and coordinating solutions at the inidvidual levels of the hierarchy. Figs. 1, bibl. of 16 titles.

UDC 517.9:536.24

SOFTWARE PACKAGE FOR APPROXIMATE NUMERICAL AND ANALYTIC SOLUTION TO STEFAN'S PROBLEM

[Abstract of article by S. G. Grigor'yev]

[Text] Described is a software package designed to automate research associated with solving the single-phase Stefan's problem, to which research of physical processes is reduced. These processes occur during change of aggregate state of matter. Package structure and operating mode are described. Examples of using package to solve certain problems are given. Package speed is evaluated. Figs. 3, bibl. of 4 titles.

UDC 007.52

FUNCTIONAL MODULES OF SOFTWARE PACKAGE FOR MANIPULATION ROBOT DESIGN PROBLEMS

[Abstract of article by S. V. Yeliseyev, S. A. Butyrin and A. A. Zasyadko]

[Text] Discussed are design principles for software package to automate process of constructing mathematical models, analysis and processing of digital experiment results in designing robotic systems. Discussed is structure of design of system and subject parts of package and organization of operation with it. Makeup of modules in the subject part by package phases is discussed. Figs. 2, tables 3, bibl. of 7 titles.

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CSO: 1863/105

UDC 681.3.06 + 62 - 506.001.57

SOFTWARE PACKAGE FOR SIMULATING PREPROCESSING METHODS IN SPEECH RECOGNITION SYSTEMS

Novosibirsk PAKETY PRIKLADNYKH PROGRAMM: METODY I RAZRABOTKI in Russian 1981 (signed to press 10 Aug 81) pp 36-42

[Article by S. L. Lidin, A. I. Yegorov and Yu. D. Savitskiy]

[Text] 1. Problem Statement

Designing automatic auditory image recognition systems (SARSO) is a major problem in modern cybernetics and part of the overall problem of automatic pattern recognition. There are many different domestic and foreign SARSO, but the problem evidently is still a long way from definitive solution.

In general form, the SARSO design problem can be formulated as follows. The recognition process consists of preprocessing of the source image, i.e. conversion of the source pattern into some description, and decision-making proper, i.e. establishing the affiliation of the description obtained to a particular class. It is evident that processing plays the main role in the recognition process since on the one hand, there are few decision-making principles (usually five basic principles are singled out) and they have all been developed and described to a sufficient extent, and on the other, because it is precisely the preprocessing that determines the form of the end description and, consequently, the selection of the decision-making rule. Thus, the preprocessing process has to be optimized so that the simplest possible decision-making rule is used (and, consequently, the least time and equipment cost is required). Design of the optimal preprocessing scheme can be formalized as follows.

Let us consider the problem of recognizing isolated words. Let us describe a speech signal that is (in digitized form) a sample of n values of a nonstationary random process as an n-vector

$$X^n(s, t) = (x_1(s, t), x_2(s, t), \ldots, x_n(s, t))$$

that is dependent on the speaker s and the uttered word t. Thus, if k_1 speakers utter k_2 words each in common order, we will have the matrix

$$k_2 \times k_1 : \mathscr{X} = [X_{ij}^n],\ i \in [1, k_2],\ j \in [1, k_1].$$

Let us call the columns of this matrix, made up of identical words uttered by the different speakers, classes, and the rows, vocabularies.

Let us introduce a finite set, generally speaking, of nonswitching statements that convert the signal into a certain description:

$$\{\alpha_p^{nm}\}_{p=1}^{N} : \alpha_p^{nm} X_{ij}^n = Y_{ij}^m.$$

Let us also consider the compound statement

$$A^{nm} = \prod_{k=1}^{M} \alpha_{p_k}^{n_k m_k}, \qquad (1)$$

where $n_k = m_{k-1}$, $n_1 = n$, $m_M = m$, $M \leq N$, which is an analog of a certain preprocessing scheme.

Let us define on the matrix $\mathscr{X}$ and the set of compound statements the discrete functional

$$\Delta[A] = \frac{\max\limits_{i, j_1 \neq j_2} D\left(AX_{ij_1}^n, AX_{ij_2}^n\right)}{\mu + \min\limits_{i_1 \neq i_2, j} D\left(AX_{i_1 j}^n, AX_{i_2 j}^n\right)},$$

where D is a certain metric and $\mu << D(X_1, X_2)$ is a minor constant introduced to eliminate a possible pole. The functional numerator is the maximum intraclass spacing in the entire sample of patterns. The minimum interclass spacing is in the denominator. By the value of Δ one can judge the applicability of a particular rule for decision making. For example, when $\Delta < 1$, let us use the nearest neighbor method and when $\Delta \geq 1$ and the minimum interclass spacing is nonzero, the method of dividing hyperplanes; when the minimum interclass spacing is zero (i.e. when pattern classes intersect), one can use probability methods etc.

It is obvious that the optimum "preprocessing scheme" will be the statement A^{opt} that minimizes the numerator and maximizes the denominator of the functional Δ:

$$\Delta[A^{opt}] = \min_{A \in \mathscr{A}} \Delta[A],$$

where $\mathscr{A} = \{A\}$.

Thus, the problem is to select the most effective (in the sense of minimizing Δ) minimum combination of statements α_p^{nm}, with the nature of the speech signal itself (randomness, nonstationarity, presence of various individual fluctuations etc.) making it possible to use the facilities of correlation and spectrum analyses as statements α_p^{nm}. And in fact, both domestic and foreign researchers use mainly these facilities in particular combinations when designing SARSO.

2. General Description of Package

We developed a software package to simulate various preprocessing methods in automatic pattern recognition systems that implements the approach described above. The package has its own input language ("problem statement language") that meets the requirement of being unencumbered with regard to procedural orientation, being natural like and consequently suitable for the user who is not too familiar with computer programming.

The purpose of the package is the facilitate development, optimization and verification of the serviceability of the various preprocessing methods through numerical experiment based on an arbitrary amount of experimental acoustical information.

This package includes a program to translate the package input language and a library of subroutines from which the source program is generated. The package functions under control of ASVT DOS [Modular Computer System, Disk Operating System]. In the general case, the sequence of operation of the package looks like this (see fig. 1). From the DOS phase library, the translator program, placed there beforehand, is loaded. It processes the package input language program, input from cards, and compiles the output program on a tape file. In the process, errors can be corrected and some parameters input from the system console. After completion of the operation, the translator is unloaded and the output program is processed by DOS facilities. The subroutine library is placed in the DOS module library and it is also accessed automatically. Two tape units are required for package operation: a data file and a source program file, also used as the working file.

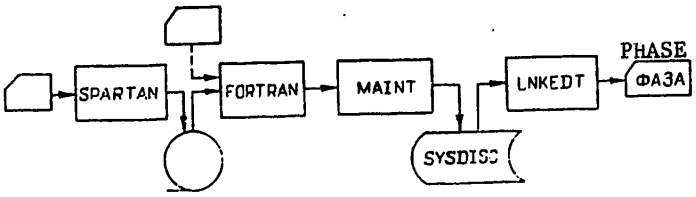

Fig. 1.

3. Subroutine Library

The subroutine library has about 50 modules, conventionally divided into basic and auxiliary. The basic modules include implementations of the following algorithms: discrete Fourier transform, fast Fourier transform by a two-point scheme with thinning out by frequency, Laplace transform, fast Adamar transform, quasilinear prediction based on autoregression model, computation of autocorrelation and cross-correlation functions, introduction of (Hahn) window, signal or spectrum clipping at some absolute or relative threshold, determination of signal energy in a specified frequency band, determination of frequency of intersection by a signal of a given level, isolation of formant frequencies, etc.

The fast Fourier transform algorithm is described in detail in [1, 2]. As is known, when a fast Fourier transform [FFT] is used on the dimension of an array, the limitation

$$N = 2^m \tag{2}$$

is imposed, where m is an integer, but the FFT requires $N\log_2 N$ operations of complex multiplication instead of N^2, which permits a substantial reduction in computation time.

The Adamar transform is a rotation group statement. The matrix N x N of the Adamar transform is specified by the recurrent formula

$$H_N = \begin{bmatrix} H_{N/2} & H_{N/2} \\ H_{N/2} & -H_{N/2} \end{bmatrix}, \quad H_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}.$$

It is evident that on the dimension of an array to be transformed, the same limitation (2) is imposed as in the FFT by a two-point scheme. The graph of computation of the fast Adamar transform (BPA) is shown in fig. 2. Structurally, it is identical to the FFT computation graph, but only addition (solid lines) and subtraction (broken lines) operations occur in it. The order of the elements of the array to be transformed is simply changed to the inverse, instead of the inversion of binary multiindexes required in the FFT. The FFT and fast Adamar transforms can be used both independently and in more complex procedures, such as in the generalized Wiener filtering procedure [3].

Seelected for the quasilinear prediction procedure was an autoregression model, i.e. a model, the transfer function of which has only poles and no nulls, since this model best describes the speech signal [4].

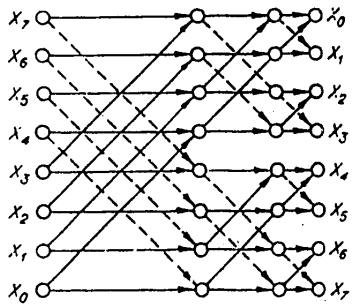

Fig. 2.

The auxiliary modules include subroutines to convert data types (for example, conversion of a source array of one-byte integer numbers into a similar array of complex eight-byte numbers, and vice versa), as well as to printout results, including printing of graphs, histograms and the so-called visible speech with four levels of quantization, subroutines for manipulation with the data file on the tape unit and certain others.

4. Input Language and Translator

The SPARTAN (Speech Patterns Automatic Recognition Translative Algorithmic Notation) input language is a problem-oriented language essentially fully machine-independent. The SPARTAN translator is written in standard COBOL and makes use of FORTRAN as the base language.

A SPARTAN program consists of optional declarative statements, the F and S statements. Declarative statements describe the experimental acoustic data (number of words, speakers, device on which the information is located, blocking, size of elementary data unit in bytes, frequency of acoustic signal quantization) and characteristic features of system to be modeled (width and shape of window). If the declarative statements are omitted, default values are assumed for these parameters.

F statements are FORTRAN statements. They are essentially not processed by the translator and included in the output program without change.

S statements consist of mandatory instructions and optional explanation. The sequence of instructions describes the structure of the transformation (1) and is a program for processing experimental information. Explanations are used to declare types of variables and dimensions of arrays mentioned in the instructions. Thus, in contrast to other programming languages, SPARTAN does not require declaration of variables and arrays at the start of a program (subroutine, block), although the task of declaring objects as they appear in a program is also handled for simple variables (but not for all types and not for arrays) in some languages, such as in FORTRAN and PL/1. The explanation begins with the key word WHERE and is processed separately, irrespective of instruction contents. The problem of declaring variables and arrays as they appear in the program has been resolved because (and only because) the SPARTAN translator is a complete preprocessor of the FORTRAN translator. During scanning of the SPARTAN program, the explanations generate the first, declarative portion of the output program, and the instructions generate the second, executable protion.

In addition to a proper identifier, an object (variable, array) in SPARTAN can be referred to by using the reserved word IT. IT refers to the last object mentioned in a given or preceding instruction. The language also has another reserved word that replaces an identifier, ELEMENT or EL. EL refers to an element, i.e. a one-dimensional subarray of fixed length, selected out of an array of experimental data.

The SPARTAN translator provides for partial interaction without using special systems. If work is being done in the interactive mode, then the translator, after detecting the absence of a particular declarative statement, sends an inquiry on the appropriate parameters to the system console. The user inputs the required declarative statement or the message "STANDARD" from the console. STANDARD effects the default conditions. When a syntax or orthographic error is detected in an S statement being examined, the translator puts out the statement text and an error message on the system console. From the console, the user inputs the corrected text or indicates discontinuance of interaction by the message "NO DIALOGUE." This partial interaction, naturally, is not very applicable in large systems, but is convenient in operating with computers of small configurations.

The SPARTAN translator also executes certain control functions. Thus, for example, when an instruction to subject some array to a Fourier transform is encountered, the translator determines the overall length of the array (the array does not have to be one-dimensional) and if condition (2) is met, includes a call to the FFT subroutine in the source program; otherwise, a call to the DPF [discrete Fourier transform] subroutine is included. If the named array is not complex, it is automatically transformed into such, etc.

Since low-level machine-oriented languages are not used in the package, and COBOL and FORTRAN compilers are available in many modern operating systems, it should evidently be noted that a rather high mobility of the package has been achieved in contrast to, say that of the "GRAF" package [5], written in autocoder-ITM and strictly oriented to the BESM-6. It should also be noted that the subroutine library can be utilized fully even without the SPARTAN translator. In this case, the package input language will be a set of references to the available subroutines in a manner similar to, say the GRAFOR package [6].

We have made provision for future expansion of the subroutine library and, since the package translator is easily expanded and added to, a corresponding increase in the number of possible instructions in the input language.

BIBLIOGRAPHY

1. Marchuk, G. I., "Metody vychislitel'noy matematiki" [Methods of Computational Mathematics], Moscow, Nauka, 1977.

2. Rabiner, L. and Gould, B., "Theory and Application of Digital Processing of Signals," Moscow, Mir, 1978.

3. Pratt, W. K., "Generalized Wiener Filtering Computation Techniques," IEEE TRANS. COMPUTERS, Vol C-21, No 7, 1972, pp 636-641.

4. Makhoul, J., "Linear Prediction: A Tutorial Review," PROC. IEEE, Vol 63, No 4, 1975, pp 561-577.

5. Somin, N. V., "The GRAF Software Package," in "Analiz i raspoznavaniye rechevykh signalov na EVM" [Computer Speech Signal Analysis and Recognition], Moscow, USSR Academy of Sciences, Computer Center, 1975, pp 31-48.

6. Bayakovskiy, Yu. I. et al., "GRAFOR: kompleks graficheskikh programm na FORTRANe" [GRAFOR: A FORTRAN Graphic Program Package], Moscow, IPM [Institute of Applied Mathematics], USSR Academy of Sciences, 1972.

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SOFTWARE PACKAGE FOR ANALYSIS OF STATIONARY MOTIONS OF MECHANICAL SYSTEMS

Novosibirsk PAKETY PRIKLADNYKH PROGRAMM: METODY I RAZRABOTKI in Russian 1981 (signed to press 10 Aug 81) pp 82-92

[Article by M. V. Pochtarenko]

[Excerpt] Ever greater interest has been shown recently in using computers to perform analytic computations. Encountered often in practice is the necessity of operating with unwieldy analytic expressions that are extremely difficult or impossible to transform. In many cases, using computers permits bypassing the difficulties associated with a large volume of analytic computations and eliminating the errors of manual computation. It is therefore no coincidence that special programming languages and systems for analytic computations (SAV) are being developed.

All analytic computation systems can be conventionally divided into general-purpose and specialized. General-purpose systems have a large number of built-in capabilities and therefore take up a great deal of main storage and require large time inputs. Specialized systems are oriented to a specific subject area. Typical of these systems is high speed and relatively minor requirements for main storage size.

An exhaustive survey of available analytic computation systems is not our goal here. Let us just mention the program facilities used in our country. Among the early domestic systems are the ANALITIK [1] language for the Mir-2 computer and the SIRIUS system for the M-222 [2]. These general-purpose systems have not received due application; this is apparently due to the impossibility of solving the serious problems associated with processing of symbolic information on those computers because of limited machine resources. These general-purpose facilities should also be mentioned: the LISP [3] and REFAL [4] languages, the AVTO-ANALITIK [5] system, and the analytic computation system for operation with Poisson series [6, 7]. The foreign systems, SCHOONSHIP, CLAM and REDUCE-2, have been introduced at the OIYaI [Joint Institute of Nuclear Research] in Dubna. A survey of these and other systems is available in [8].

Described in this article is an analytic computation system for solving problems of mechanics and a software package for analysis of stationary motions of mechanical systems, that has been implemented on the basis of this system on the BESM-6 computer in the ALGOL-GDR language [9]. The main reason for initiating development of this system was the lack of facilities for matrix-vector algebra on symbolic objects in the known domestic systems. (The SIRIUS system [2] is an exception.)

The orientation of this system to processing expressions of a specific structure has made it possible to substantially simplify certain algorithms and perform transformations that are either inefficient or unacceptable for the general type of expressions. System implementation based on a language with a computational orientation, which ALGOL-GDR is, has enabled a natural transition from the symbolic form of representation of expressions to computation of their numerical value.

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OPTIMIZATION PACKAGE LINEAR PROGRAMMING ALGORITHMS

Novosibirsk PAKETY PRIKLADNYKH PROGRAMM: METODY I RAZRABOTKI in Russian 1981 (signed to press 10 Aug 81) pp 92-104

[Article by A. I. Zholudev and A. I. Tyatyushkin]

[Excerpts] Discussed in this article are the computational schemes of two linear programming methods that start the operation from a specified plan and end computation upon reaching a specified approximation to the optimal plan. One of them, the adaptive method [1], differs substantially from the simplex-method and operates more efficiently with the main limitations of the type of inequalities. In its structure, the other, the reference method [2], is close to the simplex-method and allows multiplicative representation of an inverse matrix, which is a significant advantage in solving problems of large dimension. Both methods have been implemented in ALGOL-60 and applied for solving a number of linear programming problems.

2.3. Numerical Implementation

The algorithm described was implemented in ALGOL-60 (ALGOL-GDR). The computational procedure implementing it uses a multiplicative scheme of representation of an inverse reference matrix with compact storage of the multipliers, which permits economic use of computer storage and reduces problem solving time. An MD [magnetic disk] is used to store the inverse matrix. Exchange between main storage and the MD is performed in complete zones, i.e. in files with a length of 1024 words, with an integer number of multipliers being stored in each zone. A buffer file with a length of 1024 words, to which new multipliers are written, is used to reduce the number of accesses to the MD. After it is filled, it is copied to the next MD zone.

Matrix A is stored in compact form on ML [magnetic tape]. To speed up computation, it can be copied to the MD or, for small problems, to computer main storage.

This procedure was used to solve a series of problems in the model REGION, developed at the IEiOPP SO AN SSSR [Institute of Economics and Organization of Industrial Production, Siberian Branch, USSR Academy of Sciences]. Sizes of the matrix of limitations ranged from 148 to 660 rows and from 408 to 4200 columns. Time to solve one problem was 3-58 minutes. Maximum errors in rows on the optimal solution did not exceed 10^{-6}.

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MODULAR SYSTEM FOR SOLVING PROBLEMS IN AERODYNAMICS AND DYNAMICS OF FLIGHT OF FLYING VEHICLES BY ASYMPTOTIC METHODS

Novosibirsk PAKETY PRIKLADNYKH PROGRAMM: METODY I RAZRABOTKI in Russian 1981 (signed to press 10 Aug 81) pp 149-157

[Article by A. N. Panchenkov, Yu. F. Orlov, G. I. Antoshkina, M. N. Borisyuk, Yu. I. Laptev, V. D. Mishchenko and R. Yu. Shlaustas]

[Text] Applied in this work is the modular principle for developing a software package intended for investigating aerodynamic factors and the lift/drag ratio of carrier systems and flying vehicle as a whole as it moves close to the fluid boundary; fits and criteria of static stability during motion in the stationary mode, determinate flight dynamics, investigation of amplitude-frequency characteristics of apparatus; optimization of the basic carrier system and selection of the parameters of design schemes for flying vehicles [1, 2].

The main aim in developing this package was to put into the hands of the investigator and user-developer of new types of flying vehicles an effective tool for multivariant analysis of various phenomena associated with motion of flying vehicles. This is done by creating a library of special subroutines, the use of which requires no knowledge of methods and algorithms.

1. Package Subject Area

The essence of the subject area is composed of research on problems of motion of bodies in a restricted flow. A large number of the problems in the package are united by the common problem of airfoil motion in a restricted fluid. A typical problem is that of the motion of an airfoil of arbitrary geometry in an ideal fluid close to a solid surface. The boundary problem corresponding to it, notated in terms of velocity potential, has the form [3, 4]

$$\begin{gathered}\Delta\varphi = 0,\ g \in \Omega;\ \varphi_z = (\nabla\eta,\ \nabla\tilde{\varphi}) + \partial\eta/\partial t,\\ \tilde{\varphi} = -x + \varphi;\ g \in S;\ \varphi_z = 0,\ z = 0;\ [P] = 0,\ g \in L;\\ [P] = 0,\ g \in \Sigma;\ \varphi = \varphi_0|_{t=0},\ g \in \Omega;\ \nabla\varphi \to 0,\ x \to \infty.\end{gathered} \tag{1}$$

Here ϕ is the disturbance velocity potential, Ω is the area occupied by the fluid, g is the current point coordinate, S is the airfoil, L is the trailing edge of the surface S, Σ is the surface of turbulent disturbances, P is the pressure in the fluid flow, $z=\eta(x,y)$ is the airfoil equation, ϕ_0 is the initial value of velocity potential and $(\nabla\eta, \nabla\phi)$ is the scalar product in two-dimensional Euclidean space.

As a rule, introduced into consideration in the case of minor disturbances is acceleration potential and the boundary problems are solved by the methods of the theory of acceleration potential [4]. In problem (1), the solutions are functions of the characteristic parameter h (h is the relative distance) and various algorithms and asymtotic theories are applied as a function of its value.

Implemented for $\bar{h} \in [\bar{h}_1, \infty)$, $\bar{h}_1 \sim \bar{0}(\varepsilon)$ are algorithms of the asymtotic method of functional parameters (MFP). Used in the MFP is the group comparison scale $\{\tau^d\}$ $c\,\tau = \sqrt{(1+4\bar{h}^2)} - 2\bar{h}$ and solutions are sought in the form of the asymtotic series $\varphi = \varphi_0 + \tau\varphi_1 + \tau^2\varphi_2 + \ldots + \tau^n\varphi_n + 0(\tau^{n+1})$. Rather complete information on the MFP is contained in [5]. For values of $\bar{h} \sim 0(\varepsilon)$, quadrupole theory [6] allows making considerable simplifications in type (1) boundary problems. When $\bar{h} \to 0$, there is a certain singular confluence of problem (1). A regular asymtotic algorithm for solving this singularly perturbed problem is provided by quadrupole airfoil theory. In the first approximation of quadrupole theory, the singular confluence of problem (1) in the case of stationary motion of the wing has the form of a boundary problem for the flow under the wing [7]

$$\begin{gathered} \Delta\varphi = 0, \quad g \in \Omega_-; \\ \varphi_z = (\nabla\eta, \nabla\varphi) + \partial\eta/\partial t, \quad g \in S; \\ \varphi_z = 0, \quad z = 0; \quad \varphi_x = 0, \quad g \in L; \quad \Delta\varphi \to 0, \quad x \to \infty, \end{gathered} \tag{2}$$

where Ω is the area under the wing.

Algorithms for solving specific problems based on problem (2) also are the basis for the unit of modules for analysis of the aerodynamic performance of airfoils.

This package contains certain generalizations of problem (1) within the bounds of perturbation theory. They include mathematical models of motion in proximity to a free surface of heavy fluid of hydrofoils [3] and generation of ship waves and wave drag when there are turbulent perturbations behind the body [6]. Formulation of the boundary problem in these cases takes the form of (1) with replacement of the boundary condition on the solid screen by the known conditions of the theory of waves of small amplitude. In stationary problems, these conditions are notated as:

$$\varphi_{xx} - \mu\varphi_x + \omega_0\varphi_0 = 0, \quad z = 0, \tag{3}$$

where μ is the coefficient of dissipative forces, approaching zero in the final results; $\omega_0 = 1/2Fr^2$ and Fr is the Froude number. Algorithms for the analysis of hydrodynamic performance are constructed by using the MFP just as in the corresponding algorithms for problem (1). The difference is that with the lack of confluence of the main integral operator of the problem when $h_1 \to 0$, the results extend to the entire parametric interval

The theory of ship waves and wave drag is represented in the package by stationary problems on motion over a surface of heavy fluid of certain compact regions of increased pressure or solid bodies (systems of bodies). Used in the first case are classical algorithms for the theory of waves of small amplitude [9], and in the second (and in combination with the first case), the theory of ship waves with

turbulent perturbations behind the bodies [6]. Solutions to these problems have been implemented in the form of regular asymptotic algorithms with local incorrectness. Enlisted to obtain the unique solution to problems of this type is the apparatus of the theory of proper solutions [6] which enables simulating the generation of turbulent structures on the knife edges of body surfaces or spray jets in the theory of gliding. When the algorithms mentioned above are added to the package, one can investigate systems having lifting elements both under and above the free surface of the fluid.

All required information on problems (1)-(3) of the theory of acceleration potential and quadrupole theory is contained in [2-6]. In this package, a mathematical model of three-dimensional aircraft motion is synthesized in the "dynamics" model which primarily implements algorithms of longitudinal aircraft dynamics in restricted fluid. Owing to the specifics of aircraft which make use of the effect of a supporting surface, there are many grounds for considering a large number of problems of dynamics in linear approximation. This is precisely why problems of linear approximation are represented in this software package.

The "dynamics" module includes four separate versions of a mathematical model of three-dimensional aircraft motion. The fact is that a characteristic feature of any transport object is the presence of two groups of operating situations that are designed and that determine a basic problem of optimal design: (1) cruising mode of motion governed by the purpose of object functioning and assumed to be usually designed when the economic and operating-technical indicators of design operation are established; and (2) critical situations that are designed for selection of design solutions that afford durability, survivability in emergency situations, specified dynamic object characteristics, etc. As a rule, these situations are described by equations of aircraft disturbed motion. The range of hydroaerodynamic problems subject to solution in the first and second cases is substantially different. Thus, while in the first version it is found possible to stay within the bounds of stationary problem statements, in the second, the nature of nonstationary aircraft motion plays a major role in generating the mathematical model.

The first block in the module, an algorithm for computing aircraft position in space (fit) during stationary motion at a fixed speed, is based on constructive use of formulas for initial stability, widely known in ship theory, and the concept of conventional metacentric height [6, 10]. The algorithm allows deriving the position in space of an aircraft of arbitrary configuration as a function of the basic independent variable in the algorithm, the Froude number, as well as the aerodynamic performance corresponding to the given speed and the criteria of static stability, conventional metacentric height. The second and third blocks in the module implement computation of transient processes of aircraft disturbed motion in a quasistationary arrangement and with regard to nonstationarity of aerodynamic factors.

In determining the aerodynamic factors from stationary theory, aircraft longitudinal dynamics are described by a system of linear differntial equations. In determining aerodynamic factors from the theory of a wing in a nonstationary flow (see problem 1), aircraft dynamics are described by a system of integral-differential equations with Volterra operators having the form

$$\dot{x} = Ax + By, \quad y = \int_0^t K(t - t_1)\, x(t_1)\, dt_1, \quad x(0) = x_0. \qquad (4)$$

In this case, additional difficulties arise that can be overcome by using an exponential approximation of the nucleus of the integral Volterra operator. The initial system of equations (4) is reduced to a system of differential equations of substantially greater dimension [11].

The fourth block is an algorithm for computing aircraft path in takeoff/landing modes in a quasistationary arrangement.

Algorithms for solving Cauchy problems for ordinary differential equations are based on the asymptotic method of small time (a partial implementation of the MFP [method of functional parameters]). In this method, instead of physical time $t \in [0, \infty)$, small time $\tau \in [0, 1)$. is introduced. The solution is sought in the form of an asymptotic series

$$x = \sum_{n=0}^{N} x_n \tau^n + 0(\tau^{N+1}).$$

The time relationship is often provided by the formula $\tau = 1 - e^{-qt}$. In numerical computations of rigid systems of differential equations, the step for computing the solution is very small because of the large values of the derivatives. Thanks to the switch to small time, the calculation step can be increased and the type (4) problem solved on large time intervals. This modification of the method of small time is called the method of large steps. The advantages of the method of large steps in a computational respect compared to a number of known methods have been established by experience by savings on memory and computer efficiency.

A major problem in aircraft design is optimization of the lift system. The basic difficulties in optimizing the lift system are most often of a computational nature which imposes severe requirements on mathematical models of hydroaerodynamics used in extremal problems. The computational difficulties associated with application of these models are overcome by quadrupole theory which is used as the basis in formulating a large number of various extremal problems. As a rule, these extremal problems cover the following problem with meaningful formulation: finding the optimal geometry of the lift complex that ensures minimum value of induced drag with constant lift and various limitations.

There are different versions of extremal problems as a function of type of limitations. Isolated in the software package are three groups of problems. The first determines the optimal geometry of a wing of specified area and distance from the screen; the second, the optimal wing with a specified center of pressure; and the third is the problem on the optimal wing with constant seaworthiness. In physical variables, the latter extremal problem is formulated as

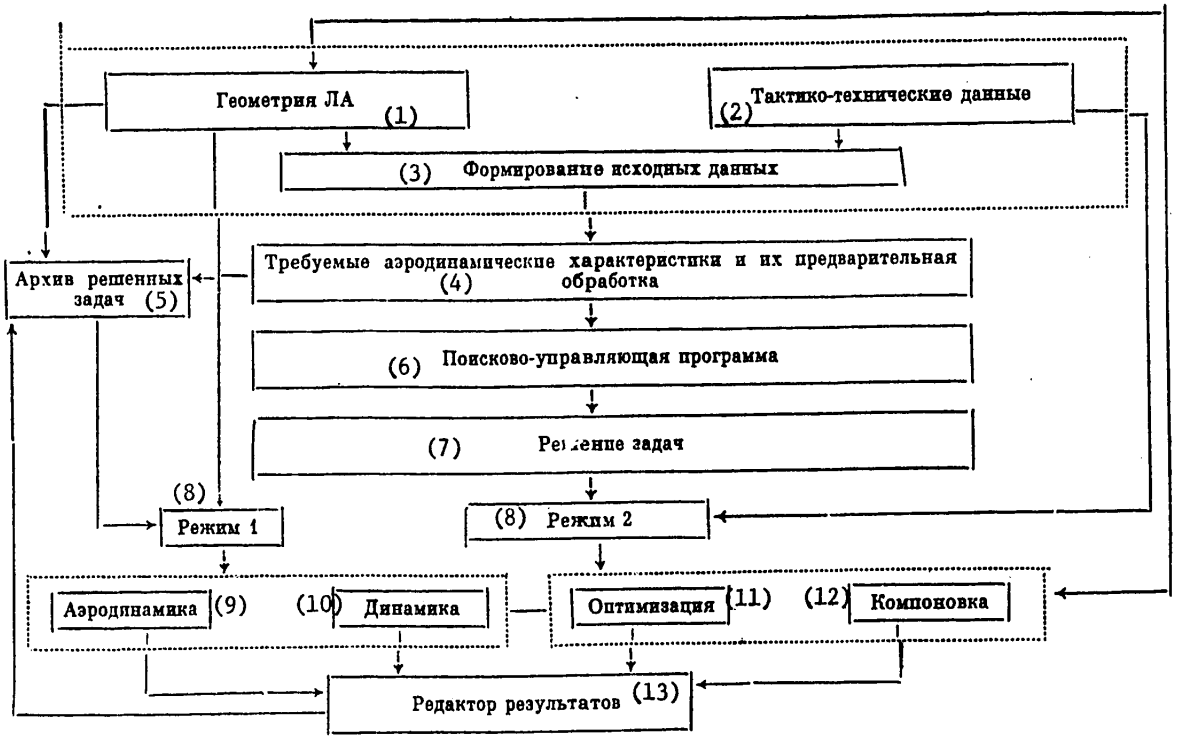
$$H(y)\partial^2\Gamma/\partial x^2 + [1/\lambda^2(y)]\partial/\partial y[H(y)\partial\Gamma/\partial y] = -\alpha(x, y)/[4\lambda^2(y)],$$
$$x \in [0, 2),\ y \in [-1, +1]; \qquad (6)$$
$$\partial\Gamma/\partial x = 0 \text{ when } x = 0;\ \Gamma(x, \pm 1) = 0;\ \Gamma(2, y) = 0;$$
$$C_{xi} = \min_{\{\Gamma, H\}} \left[-\lambda \int_{-1}^{1} \int_{0}^{2} \partial\Gamma(x, y)/\partial x \cdot \alpha_i ds \right];$$
$$\alpha_i = -4\partial/\partial y[H(y)\partial\Gamma/\partial y];$$
$$C_y = \lambda \int_{-1}^{1} \Gamma(y)\, dy = \text{const};\quad \bar{S} = \int_{0}^{1} \bar{H}(y)\, dy = \text{const};$$
$$\Gamma(\pm 1) = 0;\ H(0) = H_0;\ H(\pm 1) = H_1,$$

where $\Gamma(x,y)$ is the running circulation in a cross-section; $\Gamma(y)=\Gamma(0,y)$ is the circulation in cross-section y; $\alpha_i=\alpha_i(x,y)$ is the angle of induced wash; $\partial\Gamma/\partial x=0$ is the condition of the Zhukovskiy-Chaplygin postulate; and $\Gamma(2,y)=0$ is the condition of unstressed entrance.

Here the aerodynamic portion of the problem is determined according to the quadrupole theory of the wing [12]. In essence, this extremal problem (6) can be classified as a problem of optimal control of a system with distributed parameters. The extremal problems in the package are investigated by methods of asymptotic programming.

2. Package Structure

This software package consists of modules intended for solving particular problems. The package can operate in two modes (see drawing): computation and design.



Flowchart of computer computation of problems of aerodynamics and flight dynamics of flying vehicles

Key:
1. Flying vehicle geometry
2. Tactical-technical data
3. Generation of initial data
4. Required aerodynamic performance and preprocessing of it
5. Archive of solved problems
6. Search-control program
7. Solving of problems
8. Mode 1, 2
9. Aerodynamics
10. Dynamics
11. Optimization
12. Configuration
13. Editor of results

The basic modules in the first mode are:
Aerodynamics. This module is a set of subroutines for computing the aerodynamic coefficients of the airfoil and thin and body wings by quadrupole theory, by the method of functional parameters and by the stationary, quasistationary and nonstationary theories under the assumption of the insignificant amount and arbitrariness of disturbances in a restricted flow.

Dynamics. This module has subroutines for computing and analyzing problems of flying vehicle dynamics using various mathematical models and with different disturbances, including the problems of controllable dynamics, as well as subroutines for computing fits (in stationary mode) and criteria of static stability.

The main modules in the design mode are:

Optimization. This module solves the problem of optimizing the basic lift complex of the flying vehicle.

Configuration (overall design). In this case, parameters of configuration schemes and optimization of them are selected by using the obtained aerodynamic coefficients and extremal geometry of the flying vehicle lift elements.

The structure of the body of the package, pertaining to the specified subject area, includes the computer problem modules as well as a description of them.

Recorded in the module description are [13, 14]:
--module name
--module functional description
--names in the description of input and output parameters
--description of module messages
--resources required (memory, time, etc.), and
--module address.

Exchange between modules is effected through COMMON blocks. Modules for solving the various particular problems match strictly in inputs and outputs of information.

This software package is designed to operate on the BESM-6 computer with the DISPAK operating system and the DUBNA monitor system. The base languages used to develop the package are the standard high-level languages, FORTRAN and ALGOL-GDR. The package structure is a combination of program modules and the control program. Package operation is governed by the control program and it is used to call the required computational modules and select the solution method. Control program operation consists in analyzing user instructions and generating the output module in accordance with these instructions.

The control program for this package includes the following modules:
--input data processing
--problem solution control
--analysis of validity of solution obtained, and
--output data processing.

We have made use of a number of ideas from the work performed under the direction of S. M. Belotserkovskiy for computing the aerodynamic performance of lift systems [15].

BIBLIOGRAPHY

1. Yanenko, N. N.; Karnachuk, V. I. and Konovalov, A. N., "Problems of Mathematical Technology," in "Chislennyye metody mekhaniki sploshnoy sredy" [Numerical Methods of Continuum Mechanics], Novosibirsk, VTs, ITiPM SO AN SSSR [Computer Center, Institute of Theoretical and Applied Mechanics, Siberian Branch, USSR Academy of Sciences], Vol 8, No 3, 1977, pp 129-157.

2. Davydova, I. M. and Davydiv, Yu. M., "Elementy organizatsii bol'shikh programm" [Large Program Organization Elements], Moscow, MFTI [Moscow Physicotechnical Institute], 1972.

3. Panchenkov, A. N., "Gidrodinamika podvodnogo kryla" [Hydrofoil Hydrodynamics], Kiev, Naukova dumka, 1966.

4. Panchenkov, A. N., "Teoriya potentsiala uskoreniy" [Theory of Acceleration Potential], Novosibirsk, Nauka, 1975.

5. Panchenkov, A. N., "Osnovy teorii predel'noy korrektnosti" [Principles of Theory of Maximum Correctness], Moscow, Nauka, 1976.

6. "Asymptotic Methods in Systems Theory," No 1-11, Irkutsk, IGU-SEI SO AN SSR [Irkutsk State University-Siberian Institute of Power Engineering, Siberian Branch, USSR Academy of Sciences], 1970-1978.

7. Panchenkov, A. N., "Extremum Problems of Quadrupole Airfoil Theory," in "Asymptotic Methods in Systems Theory," Irkutsk, SEI SO AN SSSR, No 11, 1978, pp 4-40.

8. Orlov, Yu. F., "Potentsial uskoreniy v gidrodinamike korabel'nykh voln" [Acceleration Potential in Hydrodynamics of Ship Waves], Novosibirsk, Nauka, 1979.

9. Sretenskiy, L. N., "Teoriya volnovykh dvizheniy zhidkosti" [Theory of Wave Motions of Fluid], Moscow, Nauka, 1977.

10. Orlov, Yu. F., "Problem of Static Stability of Bodies Moving Close to Fluid or Solid Surface," in "Asimptoticheskiye metody v mekhanike" [Asymptotic Methods in Mechanics], Irkutsk, SEI SO AN SSSR, 1979, pp 88-107.

11. Slaustas, R. Yu., "Consideration of Nonstationarity of Aerodynamic Coefficients in Aircraft Dynamics That Uses the Effect of the Supporting Surface," Ibid., pp 107-123.

12. "Asymptotic Methods in Dynamics of Systems," Novosibirsk, Nauka, 1980.

13. Zagatskiy, V. A., "Applications Programs for the Unified System of Computers," in "Sistemnoye programmirovaniye" [Systems Programming], Part 2, Novosibirsk, VTs SO AN SSSR, 1973, pp 161-177.

14. Legon'kov, V. I., "FORTRAN Applications Program Module," in "Kompleksy programm mat. fiziki (materialy V Vsesoyuz. seminara po kompleksam programm mat. fiziki)" [Software Systems for Mathematical Physics (Materials of Fifth All-Union Seminar on Software Systems for Mathematical Physics)], Novosibirsk, ITiPM SO AN SSSR, 1978, pp 175-176.

15. Ganiyev, F. I.; Skripach, B. K. and Shitilov, S. D., "Complex Design System for Computer Determination of Linear Stationary and Nonstationary Aerodynamic Performance of Lift Systems. Experience of Application and Introduction," in "Tez.

dokl. na XXIV Krylovskikh chteniyakh" [Theses of Papers at the 24th Airfoil Readings], Leningrad, Sudostroyeniye, 1977.

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IMPROVING ASSIMILATION OF COMPUTER CAPACITIES

Kiev MASHINNAYA OBRABOTKA INFORMATSII in Russian No 33, 1981 (manuscript received 19 May 80) pp 99-108

[Article by senior scientific worker S. F. Lazareva, Kiev Institute of the National Economy]

[Excerpts] The development (design, construction and installation of equipment) of a VTs [computer center] is organized by the unified scheme regulated by guiding methodical materials of the State Committee of the USSR Council of Ministers on Science and Technology, State Standards and other normative and technical documents of USSR Gosstroy and USSR Gosstandart.

A newly created computer center, like any new plant, passes through the so-called stage of composition in which three periods can be distinguished: preparation for introduction, introduction into operation and assimilation of computer capacities. But insufficient attention is devoted to organizing the stage of composition of the computer center. Therefore, preparation for introduction, introduction and assimilation are not substantiated beforehand in the operating practice of computer centers and fulfillment of them depends on the experience and intuition of individual executors.

Organizing the management of the production and economic activity of a computer center at the stage of composition assumes that all problems that determine the composition and content, the sequence and methods of performing work to ensure timely and high-quality introduction of the computer center into operation and assimilation of computer capacities will be worked out. In this case the composition and content of work in organization of production, labor and planning differ from those during the period of industrial operation. Moreover, they vary during the three indicated periods.

The period of preparation toward operational status coincides by schedule with the stage of developing the computer center when a new computer center is planned, the building is constructed (or reconstructed) and the equipment is installed and adjusted. The problem of providing everything necessary for timely introduction of the computer center into operation and assimilation of it is solved at this time.

Preparation of the computer center toward operational status requires that the following work be performed within specific deadlines: organization of effective monitoring of the planning and construction of the computer center, delivery, installation and adjustment of equipment, provision of selection and training of qualified personnel, development of algorithms and problem-solving technology, information support and programs of the computer center, provision of experimental testing of planning solutions, development of operating instructions for personnel of the computer center, training users for introduction of machine processing of information, compilation of a schedule of organizational measures (organizational plan) with respect to operational status and assimilation of computer capacities and so on.

It should be noted that development of a computer center is regarded in economic literature as the planned development of the hardware of ASU [automated control system] to be introduced, which is a simplified interpretation of the essence and designation of a computer center at the modern stage of development of the organizational forms of utilizing computer technology. Indeed, development of a computer center is the first step in development of an ASU. However, its activity is usually not restricted to a specific closed automated system. For example, most computer centers participate in formation of a state fund of algorithms and programs and is contained in its system. And the functional links of this fund of the computer center carry out the activity that goes beyond the limits of specific ASU [9]. The independence of a computer center will be manifested even more with the development of collective forms of using computer equipment--development of KVTs [multiple-user computer center] and VTsKP [collective-use computer center] and formation of a state network of computer centers. Therefore, development of a computer center should be regarded as a fact of developing special subdivisions (enterprises) for information processing with specific functions and tasks attached to them [7]. From this viewpoint the development with respect to an ASU can be compared to technical preparation of production for a computer center and its completion, i.e., introduction of the ASU, should coincide with introduction of the computer center into operation. The possibility of gradual increase of the computer capacities of the computer center with simultaneous expansion of the range of introduced problems of the ASU is not excluded in this case.

We feel that the period of introduction into operation begins at the moment of installing the computer equipment and ends with official acceptance of it for operation. A computer center can be put into operation in parts--starting complexes (units) or as a whole. The method of putting a computer center into operation by individual starting complexes (units), i.e., by groups of KTS [hardware complex] of the computer center, separate production lines designed to process information of specific complexes of problems, is now used extensively, which was determined by the step by step design and introduction of the ASU. The feasibility of putting a computer center into operation in units is noted in [1, 7].

Despite the universal application of this method, a unified approach to determining the composition and to selection of the efficient structure of starting complexes has not yet been worked out. Therefore, the number and structure is usually not substantiated. The problem of selecting a rational structure of

starting complexes and their composition is rather complex and requires special investigation.

The considered method of putting a computer center into operation permits one to accumulate known experience of introducing the computer equipment, which is then used in assimilation of subsequent units, which contributes to reduction of the deadlines of putting the computer center into operation and accelerating the return of basic production funds of the computer center. However, a number of deficiencies is observed in practical implementation of the given method. For example, equipment is frequently introduced into operation that is not provided with the necessary volume of computer operations due to the untimely technical preparation of computer center production (due to lack of readiness of programs and information support and so on) and lack of training of computer center personnel and users. Analysis of the use of computers at 16 computer centers of the Ukrainian SSR TsSU [Central Statistical Administration] system, developed in 1977, showed that the idle time during the first six months after the computers were introduced into operation comprised an average of 26.29 percent of the actual working time due to the absence of work. The given percentage exceeded 60 percent at some of the considered computer centers.

Moreover, when designing a computer center, the structure of the KTS is usually determined for the total inventory of problems to be solved without regard to step by step introduction of them. Therefore, acquisition of a computer with a complete set of information input-output and magnetic disk and magnetic tape memory devices, with expanded capacity of internal storage and also with a complete set of peripheral equipment is planned [7], which leads to inefficient use of the computer resources and peripheral equipment.

The main cause of the indicated deficiencies is individual solution of problems of planning the organization of introduction of KTS, determination of the composition and structure of starting complexes (there are usually discrepancies in the composition of the equipment to be put into operation and the requirements of the problems to be solved at the computer center) and substantiation of the priority of introducing starting complexes.

Besides the enumerated deficiencies, one of the deficiences of step by step introduction of the KTS of a computer center is too long a period of its run, during which the computers and production processes become obsolete in some cases. The computer equipment introduced during the first stage may have to be replaced and the technology of performing computer operations may have to be replaced and sometimes the building of the computer center may have to be redesigned by the time the computer center reaches full operational status. This situation occurred at the end of the Ninth Five-Year Plan and at the beginning of the 10th Five-Year Plan with regard to the appearance of third-generation computers. To eliminate this deficiency, the capability of further pre- and re-equipping must be provided during design of the computer center or the computer center must be put into operation as a whole.

In current practice of developing computer centers, the method of making the KTS fully operational is difficult to realize since it requires considerable

acceleration of work in technical preparation of the computer center for production and accordingly recruitment of considerable labor, material and financial resources to support timely fulfillment of the operations, which is not always possible. In the opposite case the computer capacities will operate for a long time in the underloaded mode and the technical and economic indicators of computer center operation will be underestimated. Moreover, several computers cannot be practically installed immediately and one cannot receive the complete complement of makeup equipment due to the strictly limited distribution of computers, communications and other equipment (the manufacturers usually do not produce finished KTS but develop individual components of them over a number of years [1].

Development of a system of standards for the length of assimilation is of important significance to solve the problem of accelerating the assimilation of computer capacities.

Temporary standards for introduction and assimilation of computers, confirmed by USSR Gosplan and USSR TsSU, are now in effect [2]. The norm for the length of computer assimilation within the indicated standards is understood as the time from the day the document for acceptance for operation is signed until the standard average daily load is reached. The norms for the length of assimilation are established with regard to productivity of computer classes and comprise 0.5-1.5 years or 1-2 years if the first computer of a given class is installed at the computer center.

We feel that the existing system of standards of assimilation has a number of deficiencies and requires considerable finishing. The first disadvantage is related to the fact that they are designed to monitor the level of assimilation of computers put into operation, regardless of whether a computer is installed at a new or already operating computer center. As analysis showed, the assimilation of a computer is considerably slowed down at a new computer center, where the collective has not yet been selected and the production process is unregulated.

The second disadvantage is that the standards are established without regard to the dimensions of the computer center, operating modes, the complexity of the problems to be solved, the degree of automation of the production process, the nature of technical preparation of the computer center for production (original development or using standardized components of the ASU--TRP [standard design solutions], PPP [applied program pack], SUBD [data base control system] and so on) and also without regard to the newness of the equipment to be assimilated (it is assimilated for the first time in the country or it is assimilated for the second time).

The third disadvantage is that they take into account only one aspect of assimilation of computer capacities--technical assimilation. The indicators and periods of achieving economic, production and social assimilation have not been established. At the same time one of the causes of prolonged assimilation of computer capacities is that the technical and economic indicators to be monitored, by the level of which one can judge the degree of assimilation of computer capacities, have not been established at the computer center.

As a result the level of the indicators, toward improvement of which the efforts of the entire collective of a new computer center should be directed, remains unmonitored.

It should be noted that standardization of the periods of assimilation of computer capacities, although important, is not the basic factor that affects the reduction of deadlines of assimilating the computer capacities of new computer centers. Regardless of how well substantiated the standard deadlines of assimilation are, observation of them depends primarily on the level of organization of work during periods of preparation for introduction, introduction into operation and assimilation of computer capacities.

Plant management of their fulfillment is of decisive significance in providing the corresponding level of organization work. The list of measures on preparation for operational status is now presented in the contract design according to the methodical and guiding materials, while the measures that ensure that the computer center will be put into operation and assimilation are worked out during the detail design phase. This is related to the fact that a number of operations in organization of operational status and assimilation are performed during the period of designing the computer center.

To intensify monitoring and the attention of management and workers of a new computer center in the problems and difficulties of the stage of composition, we feel that the plan (organizational plan) of organizing preparation for introduction, introduction and assimilation can be formulated as a separate document. A number of methodical problems--determination of the structure and content of the organizational plan, the order, methods and deadlines of developing it, substantiation of the period for which it is being developed (for the entire stage of composition or individually for each phase of it) and so on--must be solved.

Organization of accounting for the actual totals of fulfillment of the planned organizational measures and creation of the document form of registering them are also of important practical significance to improve management of the process of establishing a computer center. This is indicated by the experience of operating the computer centers of the Ukrainian SSR TsSU system, made available monthly as the "Report on entry and introducing into operation computers and PVK [punch card computer complex] (Form No 6 mechanical accounting), the format of which is confirmed by decree No 249 of the USSR TsSU, dated 29 March 1977. In this regard they keep a record and register the fulfillment of certain measures of the period of preparation toward operational status: receipt of the computer, preparation of the building, completion of specialist training and putting the computer into operation. This was a factor that made it possible to reduce the number of cases of excessive standard deadlines of putting a computer into operation.

Thus, improvement of standardization, planning and accounting for the length of each phase of the stage of composition is a considerable reserve for accelerating the introduction and assimilation of computer capacities.

6521
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METHODS OF IMPROVING SECTOR USE OF COMPUTER EQUIPMENT (FOLLOWING EXAMPLE OF UKRAINIAN SSR MINISTRY OF MOTOR TRANSPORT)

Kiev MASHINNAYA OBRABOTKA INFORMATSII in Russian No 33, 1981 (manuscript received 16 Jun 80) pp 126-132

[Article by A. G. Nikolenko, assistant, Kiev Institute of the National Economy]

[Excerpts] The Ukrainian SSR occupies one of the leading places in development of motor transport, the role of which is exceptionally high in solution of the most important national economic problems of the republic. The Ukrainian SSR Minavtotrans [Ministry of Automotive Transport] combines more than 900 motor transport enterprises. Approximately one billion tons of national economic goods and 7.0 billion passengers are hauled annually by the motor transport of the Ukrainian SSR and at the same time more than 100,000 different trucks and turck trains participate, providing the populace of the republic and more than 22,000 enterprises and organizations with transport service [2].

Management of motor transport is a complex dynamic process characterized by large volumes of processed information, laboriousness of performing management functions, the need to find correct solutions within optimum deadlines and also the relationship of functional indicators of individual structural sections of the sector in the overall system.

Small and medium enterprises--motor transport enterprises (ATP), motor columns (AK), service stations (STO), refuelling columns and so on predominate in the quantitative sense in the structural plan within the Minavtotrans system. As management facilities, the enterprises of motor transport have their own specific production process, which determines the characteristics in information flows, the documents used, the time and principles of data formulation and the methods and procedures of processing it.

One of the main conditions that contributes to a further increase of the intensity and efficiency of operation of motor transport is extensive introduction of the advances of science and engineering and of leading technology into production and improvement of management on the basis of using economic-mathematical methods and computer equipment (VT).

A wide network of various types of computer installations (VU)--a main computer center (GIVTs), multiple-user information computer centers (KIVTs) and their branches, machine calculating stations (MSS) and mechanized accounting

stations (MSB)--functions in the system of the Ukrainian SSR Minavtotrans. Moreover, a considerable number of small and medium enterprises utilize keyboard computers at the operators' positions of control apparatus or are serviced by computer installations belonging to other ministries and agencies.

Analysis of the composition of the hardware utilized shows that the computer centers of the Ukrainian SSR Minavtotrans are equiped mainly with second- and third-generation computers. The specific weight of the series YeS [Unified Computer System] and ASVT [modular system of computer equipment] computers comprises approximately 80 percent, which is an important factor for organization of highly efficient systems of machine processing of data. At the same time a considerable number of enterprises and organizations of the sector has low-power computer installations equippedwith keyboard and punch equipment of obsolete models and that do not meet the increasing needs for information and calculating work.

Despite the fact that the needs for information and calculating work in the sector are not being met, the average daily load of the computers throughout the ministry as a whole is half the technical capabilities and fluctuates within a considerable range at different computer centers. The low specific weight of the useful operating time of the computers (approximately 40 percent), the considerable amount of idle time (more than 10 percent) and also the degree of computer concentration at the computer center--the load is higher where there are two or more machines--affect its level.

With the current forms of using computer equipment, each enterprise and organization is trying to have local VU [computer installation] and to use their own computers or other data processing hardware, which leads to dispersion of computer equipment, disconnection of operating VU and those being developed, reduction of the load, duplication of planning work and increasing the cost of data processing. All this sharply limits the capability of automation of management at the numerous small and medium enterprises, which are dominant in the sector. These enterprises do not have sufficient volumes of information to be processed to use a computer and in the absence of user stations and the required number of communications channels can utilize the capabilities and advantages of large computer installations.

The problems of improving the existing and development of a new system of computer equipment use on a sector scale become timely in this regard. One of the basic directions of improving the level of data processing is development of a network of computer centers which permits a considerable increase in the efficiency of using computer equipment and which provides future development of the most progressive forms of using it.

Based on investigation of the existing management structure of the Ukrainian SSR Minavtotrans, the territorial disposition of enterprises and organizations of the sector, the information flows circulating in the sector and also the territorial disposition of functioning computer installations of the ministry, the radial structure of the network of the Ukrainian SSR Minavtotrans can be used, which satisfies more fully the requirements placed on it.

6521
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DEVELOPMENT OF ORGANIZATIONAL AND ECONOMIC CONTROL IN AUTOMATED CONTROL SYSTEMS IN USSR MINISTRY OF POWER AND ELECTRIFICATION

Moscow ENERGETIKA I ELEKTRIFIKATSIYA. SERIYA: SREDSTVA I SISTEMY UPRAVLENIYA V ENERGETIKE in Russian No 3, Mar 82 (manuscript received 29 Dec 81) pp 1-5

[Article by Ye. I. Blank, V. A. Semenov and V. F. Shumilin]

[Excerpt] During th 10th Five-Year Plan much work was done in the USSR Ministry of Power and Electrification to develop automatic systems for organizational and economic control at the level of union and republic ministries, power systems, and enterprises in the electricity networks.

In 1980 the second stage of the "Energiya" sector automated control system [OASU] was commissioned. During 1979-80 the first stages of the republic automated control systems [RASU] were put into industrial operation under the Ukrainian and Kazakh ministries of power and electrification. In 1979 the second stage of the Uzbek SSR Ministry of Power and Electrification RASU was brought into industrial operation.

By the end of 1981 automated control systems [ASU's] will be functioning in most power systems, including in the 11 union republic power and electrification main production administrations.

The control computer centers that have been organized in 80 power systems form the technical base of the power system ASU's. During the 10th Five-Year Plan the number of control computer centers more than doubled.

More than 60 percent of the tasks set for the power system ASU's are those of organizational and economic control (bookkeeping, control of energy marketing, material-technical supply, control of power repairs and so forth).

With each passing year there is an increase in the number of subdivisions and enterprises that utilize the results from machine problem-solving. In 1980 machine time for solving problems of organizational and economic control was spread as follows (mean values for 64 power systems): regional power administration (economic planning department) subdivisions, 74.7 percent, power system enterprises 25.3 percent. Centralized bookkeeping uses 20.7 percent of machine time and maintenance and operating services for electrotechnical and heat-technical equipment, the operation of the electricity networks, reliability and technical safety and so forth, 6.8 percent; the departments of material-technical supply

and fuel and transportation service, 3.5 percent, the planning section 2.7 percent, and the personnel department, labor and wages section, and laboratory scientific organization of labor 1.9 percent.

Of the power system enterprises, the most active are energy marketing (energy inspection) and the enterprises of the electricity networks, which use 8.9 and 7.1 percent of machine time respectively.

The Kiev Power System, the Latvian Main Power System, the Volgograd Power System, the Novosibirsk Power System and other power systems make extensive use of the computers.

Bookkeepers at a number of power systems (the Donbas Power System, the Odessa Power System, the Smolensk Power System, the Chelyabinsk Power System, the Volgograd Power System and so forth) use 3,000-5,000 hours of machine time annually to solve bookkeeping tasks (calculating the movement of commodity and material value, fixed capital, financial-calculation operations and so forth).

Power systems are making increasing use of the YeS-9002 and YeS-9004 devices to prepare data on organizational and economic control tasks, which enables hundreds of thousands of punch cards to be saved each year.

In a number of power systems (the Belorussian Main Power System, Dnepr Power System, Donbas Power System, Kiev Power System, Khar'kov Power System, Moldavian Main Power System, Rostov Power System and so forth), three to six reference stations have been set up for initial data processing. These stations are equipped with punch accounting machines and keyboards, and in individual cases, with a computer (the Donetsk mobile power station, the Uglegorsk and Voroshilovgrad GRES's of the Donbas Power System). Problems of organizational and economic control are solved at the reference stations, which makes it possible to remove some of the load from the administration computer center in the power system.

During the 10th Five-Year Plan work was started on the development of an automated control system for electricity networks, based mainly on the computers installed at the power system administration computer centers. In the mobile power stations themselves there is data transmission equipment or teletype machines for communicating with the administration computer center. In individual cases invoicing machines are installed in the mobile power stations.

In most power systems that have introduced an automated control system improved labor productivity has been achieved with nominal redundancy of something of the order of 1,300 personnel during the 10th Five-Year Plan. Improvements in labor productivity are being achieved through resolving dispatcher problems (computation of set regimes, stability, short circuits and so forth), mass accounts with the consumers of electric power and heat, bookkeeping tasks, and monitoring of power maintenance, for example:

in the Dnepr, Donbas and L'vov power systems, during the period that the ASU's have been functioning 209, 185 and 145 persons respectively have been made redundant;

in the Smolensk Power System the transfer of bookkeeping to the computer has made it possible to significantly improve the labor productivity of bookkeepers and

to use the name number to process a large increase in the amount of information; nominal reduction of personnel has been 37 persons;

use of the computer in the eastern networks of the Latvian Main Power System has made it possible to reduce labor costs for accounting and working up estimates for capital repairs on the electricity networks from 7 to 0.5 men per month, and search time to find damage on power transmission lines from 4.4 to 3.1 hours.

During the 11th Five-Year Plan work on the ASU development in power engineering will be continued. Further improvement and development of the "Energiya" OASU is planned, along with operation of the second stage of the RASU's for the Kazakh and Ukrainian ministries of power and electrification. During this work further expansion of tasks solved will take place on the basis of the more extensive use of data banks, dialogue systems, and the integration of data streams both within the framework of the "Energiya" OASU and the RASU's, and between the levels (communications with the power system ASU's).

New programs will be constantly written for the YeS operating systems using data banks tested within the sector (the "Elektra" input data control system, the economic information system and SETOR [expansion unknown]).

Dialogue systems will be used mainly for inputting and outputting operational data.

The first stages of ASU's will be commissioned in 28 power systems. The power system ASU's introduced during the Seventies will be further developed.

9642
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UDC 666.5:65

YeS-1022 COMPUTERS IN AUTOMATED CONTROL SYSTEMS

Moscow STEKLO I KERAMIKA in Russian No. 3, Mar 82 p 29

[Article by Yu.V. Petrov, deputy chief of the Automated Association Management System Department and S.V. Petelin, chief of the Programming Office, Konakovo Glazed Earthenware Plant imeni M.I. Kalinin: "Experience with the Efficient Utilization of the YeS-1022 Computer in Automated Control Systems"]

[Text] In our plant, the first stage of an ASU [automated control system] based on the Minsk-32 computer and punched card/tape machines was placed in service in 1974.

Bookkeeping tasks were carried out using the punched card/tape machines, where the most important of these tasks in terms of the volume of data processing were labor and wage accounting, banking and cash flow operations, as well as accounting for the arrival and movement of material valuables, production process wastes and breakage.

The Minsk-32 computer was used to solve problems of quarterly, monthly and daily planning of product output by the main production shops (all the way down to sections and shifts) and operational monitoring of plan execution at the same level, as well as a number of problems for economic planning services.

The problem oriented "Tver'" software, developed just as the system as a whole, by the Tsentrogrammsistema scientific production association was taken as the basis for the Minsk-32 computer software.

After the system was in place, the collective of the computer center of the plant developed and executed tasks in the standard Cobol language for the Minsk-32 computer.

Operational experience with the system has demonstrated the effectiveness of the decisions which were made and the high level of its development. Thanks to the automation, the labor intensity of bookkeeping and analysis has been significantly reduced. The economic planning subsystem has made it possible to provide for centralized production of differentiated plans for product production as well as operational monitoring of their execution, something which has

played an important role in establishing a steady work cycle for the plant as a whole.

The very existence of computer hardware in the plant and the presence of specialists has made it possible for plant services to put forward additional requirements to be placed on the realization of more complete automation of management functions. The necessity of expanding the functions of the ASU in the plant at the present time is also explained by the fact that a department of the automated control system for the republic level industrial association Rosprom-farfor [RSFSR China Industry Administration] was created based on the computer center, and in 1980, the association ASU (ASUO) based on the YeS-1022 computer was brought on line.

The expansion of the computer fleet has caused serious problems. First of all, it has become necessary to improve the level of servicing of the equipment which is in operation and to master fundamentally new third generation computer hardware, something which is complicated by the large number of different types of equipment in a computer center. Thus, electronic keyboard calculators and adding machines are used in the manual information processing section; in the sorting section, tabulators and totalizing card/tape perforators are used; and digital perforators are used in the section for data preparation using punched cards/tapes. Peripherals for repairing data on punched cards and tape, as well as teletypes for data preparation on five punched tape tracks are also used for the Minsk-32 and YeS-1022 computers.

All of this creates definite difficulties when processing the information simultaneously in all sections.

An analysis of the situation which has arisen showed that the most effective results for assuring the development of both the plant ASU and the association ASU can be obtained through improving the technological suitability of data processing on the YeS-1022 computer. The following directions for the modernization of YeS-1022 computer software were selected:

--The use of magnetic tapes only for copying information for the purpose of duplication;

--The maximum possible exclusion of the role of the computer operator in the data processing within the framework of the given task;

--Standardization of the preliminary data processing operations on the computer.

The assumption has been made in this case that one disk pack of a store with a capacity of 29 megabytes for data storage is sufficient for functioning of the association ASU, including the programs and one working pack. The third pack was set aside for the translators. A procedure governed by regulations has been introduced for copying a functioning pack at the level of one generation.

Since the problem solving process or the translation process does not require more than two disk drives following modernization, a system reserve has been

provided with respect to the failure of the third disk drive of the computer (previously, three disk drives were used in the system).

Indicator	Before Modernization	After Modernization
Number of operations to set up magnetic tapes or when switching the number of stores	More than 100	1
Number of packs for program starting	More than 60	10
Duration of computer run, hours	No less than 7	Less than 1

The modernization of the system was started with the formulation of optimization tasks for product output plans of individual enterprises and the association as a whole, where this optimization was automated. Thus, by the curtailing of magnetic tape use for operating purposes, a considerable savings in time was achieved when solving this labor intensive problem for one enterprise (see the table). This was the prerequisite for the complete automation of the data processing within the framework of a single task. For this purpose, a program was developed which makes it possible to utilize a job packet to do the job which is found in the library of initial data modules. This reduces the function of the operator for the majority of tasks to a single operation: indicating the designation of the task. On the other hand, such an approach to data processing makes it possible for the programmer to move on from the compilation of a packet to start a single program to the programming of the process itself using the standard hardware of the disk operating system of the unified system of computers. In this case, the modernization of the existing software involves minimal reworking of the programs.

The existing software of the association ASU for the preliminary data processing for data monitoring and correction is based on the "Input-Output Generator" packet of applied programs (PPP GVV-DOS) and supplemental correction routines. In this case, practically every task has its own input and correction algorithm. The complexity of any of them does not allow for the development of a sufficiently simple process technology for the preliminary data processing. Instead of these algorithms, a single algorithm is introduced for all tasks, which utilizes the PPP GVV-DOS programs of the second type using scratchpad files. It is assumed that the storage of scratchpad files will not be realized using magnetic tapes. This will in practice curtail the volume of the data stored on magnetic tapes by an order of magnitude.

The number of control operators for the tasks, which provide for the execution of the preliminary data processing routines, will be reduced by a factor of 30 times. Standardization of the preliminary data processing facilitates the modernization of the system as a whole.

The work being done makes it possible to come up with a comprehensive solution of the problem of freeing operational personnel and programmers, as well as computer resources. This will provide the conditions for further expansion of the enterprise ASU.

8225
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UDC [[025.4.036: 007.51]: 61] (497.2)

DIALOGUE FACILITIES USED BY BULGARIAN CENTER FOR SCIENTIFIC INFORMATION ON MEDICINE AND PUBLIC HEALTH

Moscow NAUCHNO-TEKHNICHESKAYA INFORMATSIYA, SERIYA 2: INFORMATSIONNYYE PROTSESSY I SISTEMY in Russian No 3, Mar 82 (manuscript received 2 Jul 81) pp 6-8

[Article by Ye. Pavlovska and P. Prodanova, Bulgaria]

[Excerpts] Design of the National Automated System of Scientific and Technical Information [NASNTI] in Bulgaria was oriented toward up-to-date technical facilities and a developed terminal network. All the sector systems of scientific and technical information in the country and their information organs have access to data bases located at the Central Institute of Scientific and Technical Information [TsINTI], the central organ of NASNTI. Data bases covering an extensive range of subjects and of interest to a large number of users are concentrated in its automated information center.

The sector system for scientific medical information uses data bases set up within TsINTI on the basis of data files stored on magnetic tapes obtained from other countries and their specialized international systems. At this time its central organ, the Center for Scientific Information on Medicine and Public Health [TsNIMZ] with a central medical library to serve its users, employs the following data bases:

1. MSIS NIR, series "Medicine, Pharmacology and the Medical Industry, contains data on scientific research work done in the socialist countries and dissertations in the field of medicine.

Since 1981, every 3 months TsNIMZ has made available current information from this data base for scientific reseaerch institutes of the Bulgarian Medical Academy.

2. INIS (International Nuclear Information System), an international information system on nuclear energy.

Information on nuclear medicine, radiology and radioisotope diagnostics from this data base (bibliographic references and abstracts in English) is made available monthly as selective distributions of information in the form of machine printouts for 160 users, mainly from the X-ray and radiology and oncology scientific research institutes.

3. INSPEC (Information Service in Physics, Electrotechnology, Computers and Control). An information system on physics, electronics and computer and control equipment, Great Britain.

4. COMPENDEX (Computerized Engineering Index), United States.

The data bases of INSPEC and COMPENDEX are made available for retrospective searches of bibliographies and abstracts in English to specialists in the fields of optics, medical equipment, prosthetics and diagnostic methods.

5. BIOSIS (BioSciences Information Service), United States. An information services on biology.

The data files of the system are made up 50 percent of material on theoretical medicine, 15 percent on botany, 15 percent on microbiology, immunology, parasitology and public health, 10 percent on zoology and 10 percent on general biology.

Each year more than 260,000 documents are inputted to the system; they consist of books and articles from 8,000 periodical medical journals and collections of materials from conferences and symposiums.

One serious defect in the use of the data bases formed in other countries is the difficulty in accessing primary sources, which quite frequently are not available in the countries working with these bases.

The BIOSIS data bank satisfies 60-65 percent of the information requirements of physicians in Bulgaria.

Interactive mode and a flexible search strategy when using the TsINTI data bases are insured through the utilization in the Bulgarian NASNTI of the STAIRS/VS applied prgram package--(Storage and Information Retrieval System), a system for storing and retrieving document information in natural language.

In the sector system of scientific medical information, dialogue facilities are also used for data retrieval in the "Medik" data base. This data base has been created within the framework of the International System of Scientific Medical Information in the Socialist Countries (MEDINFORM) which includes Bulgaria, Hungary, the GDR, Cuba, Poland, the USSR and Czechoslovakia; scientific medical information is exchanged on magnetic tape.

Individual organs of scientific medical information in these countries process their own national medical literature, record it on magnetic tapes and send them to the base organ, which function is fulfilled by the TsNIMZ and TsINTI of Bulgaria.

The base organ combines the data bases on magnetic tape into a common file, makes copies for the participants and sends each participant one copy of the aggregate file, and it accumulates data on the aggregate files onto the magnetic disks of the "Medik" data base.

Each year 10,000 documents from the MEDINFORM countries are inputted to the "Medik" data base.

The "Medik" data base now comprises 30,000 items of information and includes bibliographies for articles from 420 periodicals and continuing medical publications from the socialist countries.

9642
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SIXTH ALL-UNION SCIENTIFIC AND TECHNICAL CONFERENCE 'DEVELOPMENT AND USE OF ANALOG AND ANALOG-DIGITAL COMPUTER EQUIPMENT'

Kiev KLEKTRONNOYE MODELIROVANIYE in Russian No 2, Mar-Apr 82 pp 105-107

[Article by N. I. Senchenko]

[Text] The routine Sixth All-Union Conference "Development and Use of Analog and Analog-Digital Computer Equipment" was held in Moscow on 27-29 October 1981. The conference was organized by the Central Administration of the Scientific and Technical Society of Radio Engineering, Electronics and Communications imeni A. S. Popov, the Ministry of the Radio Industry, the Ministry of the Electronics Industry, the Ministry of the Communications Equipment Industry, the USSR Ministry of Communications, the Ministry of Instrument Building, Means of Automation and Control Systems, the USSR Ministry of Higher and Specialized Secondary Education and the USSR Academy of Sciences. Representatives of ministries, agencies, scientific institutions, enterprises and higher academic institutions from 68 cities of the Soviet Union participated in the work of the conference. Approximately 150 reports and brief communications were heard at two plenary sessions and four sections.

Three reports were read at the plenary session of 27 October. Problems of integration of one to eight analog computers (AVM) of type AVK-32 with typical digital computers of the YeS EVM [Unified Computer System] of domestic manufacture were considered in the report of V. B. Ushakov, I. M. Vitenberg and G. M. Petrov "ATsVK-3 analog-digital computer complex of the unified system and its software."

In his report entitled "Method of evaluating and ways of increasing the productivity of analog-digital computer systems," V. G. Belyakov considered the method of evaluating and ways of increasing the productivity of analog-digital computer systems (ATsVS).

It was said in the report of N. R. Andronatiya and A. A. Chelyshev "Investigating methods of automating the monitoring of analog computer equipment in production" that it is economically feasible to use digital computers to automate the monitoring and diagnosis of analog units in production.

Further work of the conference proceeded in four sections that represented the basic directions of modern theory and practice of development and application of analog and analog-digital computer equipment.

The reports were divided into the following groups by topic in the section "General design principles and software of analog-digital computer equipment and analog computer equipment."

1. Structural organization and simulation of analog-digital computer equipment and analog computer equipment. Reports and brief communications were heard during the discussions devoted to the principles of simulation modelling of parallel structures, problems of designing integration equipment for a two-level computer network, means of organizing work in design of analog-digital computer systems and software.

2. The software of analog-digital computer systems. A system for automation of compilation of analog-digital programs that provides automatic compilation of the program for analog-digital computer systems in FORTRAN with description of the input problem in high-level input languages, proposed and developed at NIIschetmash [Scientific Research Institute of Calculating Machines] was considered in the reports and communications. Problems of designing systems software for single- and two-level analog-digital computer systems and also systems for automation of compilation of analog and analog-digital programs were considered.

3. Methods and accuracy of solving problems and problem-oriented complexes. Various aspects of constructing the methods for modelling multidimensional reciprocal problems for differential equations of parabolic and elliptical types with regard to their incorrect postulation, hybrid methods of solving operator equations with high accuracy and applied software for modelling various dynamic systems were considered in the reports and communications. Problems of constructing algorithms and programs to carry out preliminary processing of analog signals by microprocessors and systems for automated input and display of analog information using analog and analog-digital computer equipment were discussed.

4. Machine methods of solving boundary-value problems. The structures of hybrid systems with analog network processor oriented toward solution of equations with partial derivatives were considered. The network models contained in the system contain both fixed parameters and commutation of assemblies and also regulated parameters and variable commutation of assemblies.

The report of K. A. Babordin, V. N. Skorik and A. Ye. Stepanov "Problems of Designing a Probabilistic Calculator for Solving Boundary-Value Problems," presented by the Institute of Problems of Simulation in Power Engineering, Ukrainian SSR Academy of Sciences, in which a specialized probabilistic device designed to solve multidimensional boundary-value problems with complex forms of domain boundaries, evoked great interest. The use of the Monte Carlo method and the corresponding algorithms for organization of calculations permits a significant reduction of the time required to solve the indicated problems compared to a digital computer.

It was noted that the absence of serially produced network models does not contribute to development of hybrid methods of solving boundary-value problems.

Meetings of the section "Analog and analog-digital computers and general-purpose systems" aroused great attention on the part of the conference participants.

The reports of the participants of the section were devoted to the following directions.

1. Analog and analog-digital computers and systems. Operating amplifiers. Reports concerning the configuration and functional principles of hybrid computer systems were heard and discussed at this session. Problems of design and investigation of the characteristics of operating amplifiers were also illuminated.

The report of G. N. Aleksakov and V. V. Gavrilin "An analog integrating calculator," devoted to development and to the method of using a calculator measuring 540 X 240 X 80 mm for automation of calculations in design of automatic control systems, evoked great interest.

2. Development of the AVK-3 third-generation analog computer complex. Universal non-linear converters of one variable. The reporters talked about specific engineering developments and improvements of various functional converters of one variable, units for communicating with the channel, units of the AVK-32 and specialized trigonometric units.

3. Multiplication devices. Functional converters of two variables and special analog units. The reports were devoted to design of multiplication devices and two-variable functional converters of increased accuracy. The results of developments of solving elements of increased accuracy were presented for the analog part of the Rusalka hybrid computer system and also special units for modelling the dynamics of complex mechanisms.

The reports and communications were divided into two groups in the section "Analog-digital and digital-analog conversion of information."

1. Problems of the theory of analog-digital and digital-analog conversion. Problems related to design of analog-digital converters (ATsP) based on microprocessors, to development of models and structures of high-speed ATsP and development of converters of increased reliability were touched on at this session. Methods of investigating and reducing the static error of analog-digital converters of various types were considered.

2. Hardware for analog-digital and digital-analog converters. This group included reports devoted to the structures and design of analog-digital converters to determine the parameters of signals with wide frequency spectrum, of high-speed analog-digital converters with parallel and parallel-series coding that provide conversion time of 50 nanoseconds and analog-digital converters with programmable conversion accuracy. The design principles of digital-analog converters (TsAP) in CAMAC standard with information output over four channels and integrated digital-analog converters with minimum control components were considered. Problems of designing digital-analog and analog-digital functional converters and conversion devices for microprocessor systems

and analog-digital computer systems and for information processing upon entry into a digital computer were touched on.

The reports of the participants of the section "Use of analog computer and analog-digital computer equipment" were devoted to the following directions.

1. Analog-digital modelling of dynamic systems. At this session the conference participants exchanged experience in using various types of hybrid computer systems to investigate the dynamics of turbounits and identification of individual facilities and sections of SAU [automatic control systems] and to investigate mechanical systems and design of modern following devices. Special attention was devoted to design of simulators using analog-digital computer systems and also to the application of analog-digital computer systems for processing experimental results.

2. Modelling of elasticity and vibration problems. The use of various specialized modelling systems for investigating the characteristics of individual mechanisms and machines and vibration processes for solving problems of elasticity theory was discussed in the reports.

3. Modelling of various applied problems on analog computer and analog-digital computer equipment. The reports of this direction were devoted to using analog and analog-digital computer equipment to investigate the stability of energy systems, the dynamics of automatic control systems of nuclear power plants and production machines, the dynamics of a nuclear reactor of variable volume and input-output devices, modelling of systems containing valves, gas lines and phase automatic tuning systems.

Problems of modelling heat- and mass-transfer processes by analog and analog-digital computer equipment were considered at the fourth section of this session.

Three talks were heard at the concluding plenary session of 29 October. The report of B. Ya. Kogan, A. I. Kaz'min, A. A. Menn and G. M. Petrov "Rusalka third-generation hybrid computer system" evoked the interest of the conference participants. The design principles of hierarchical hybrid computer systems and their software were considered in it.

The report of V. G. Belyakov, V. A. Svyatnyy and L. P. Fel'dman "Main results and prospects for development of analog-digital computer systems based on the AVK-3 complex, control complexes of the SM EVM and models of the unified computer system" evoked great interest.

Attention was devoted in the report of G. V. Chalogo, I. Ya. Shor and M. G. Levin "Prospects for design of systems for automation of design of a controlled electronic device based on an analog-digital computer complex" to problems of developing problem-oriented software.

In the final talk, the chairman of the organizing committee Doctor of Technical Sciences, Professor V. B. Ushakov summarized the decisions made at the Fifth All-Union Conference on Analog and Analog-Digital Computer Equipment, held in 1977.

The decision was adopted at the Sixth All-Union Conference in which it was noted that serial production of the AVK-3 and ATsVK-3 and also of conversion and integration devices must be increased and the publication and transfer of the software of analog and analog-digital computer equipment to the user must be organized.

The Sixth All-Union Conference on Analog and Analog-Digital Computer Equipment summarized the work of specialists in the field of development and application of analog and hybrid computer equipment, considered new directions of the theory and practice of hybrid calculations and determined the most important problems for further investigations on the basis of the needs of the country's national economy.

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ALL UNION SEMINAR 'SPECIALIZED PARALLEL PROCESSORS FOR SOLUTION OF BOUNDARY-VALUE PROBLEMS'

Kiev ELEKTRONNOYE MODELIROVANIYE in Russian No 2, Mar-Apr 82 p 107

[Article by L. L. Kotovich]

[Text] The All-Union Seminar "Specialized parallel processors for solution of boundary-value problems," organized by the National Committee of the USSR, International Association of IMACS, Central Administration of NTORES [expansion unknown] imeni A. S. Popov, the Ministry of Higher and Secondary Specialized Education, Latvian SSR and the Riga Order of the Red Banner of Labor Polytechnical Institute, was held in Riga on 14-16 October 1981. Promising methods of solving boundary-value problems of field theory on specialized parallel processors (special processors) and problems of designing special processors were considered at the seminar. A great deal of attention was devoted to existing and planned network models of analog-digital computer complexes of the R-network--digital computer type.

The following sections worked at the seminar: Theory and Methods, Hardware, Software and Applied Problems. Approximately 200 specialists from Moscow, Leningrad, Kiev, Odessa, Khar'kov, Taganrog, Kuybyshev, Penza, Donetsk and other cities of our country participated in the work of the seminar.

The proceedings of the seminar were published in a collection of topics: Specialized parallel processors for solution of boundary-value problems. Report topics of an All-Union Seminar, Riga, 14-16 October 1981, edited by A. P. Spalvin', Riga, Riga Polytechnical Institute, 1981, 177 pages.

The following reports were presented at the Plenary session: N. N. Yanenko, V. G. Khoroshevskiy and A. D. Rychkov (Novosibirsk) "Computer systems with programmable structure and parallel methods of calculations in problems of mathematical physics," A. V. Kalyayev (Taganrog) "Multiprocessor structures with programmable structure of processors for solution of boundary value problems," I. I. Krashin and V. I. Trushkin (Moscow) "Experience of operating the Saturn-2 analog-digital computer complex and general requirements on specialized processors for solution of hydrogeological problems" and M. M. Maksimov, A. P. Spalvin' and E. E. Rode (Moscow and Riga) "Aspects of technical realization of a parallel processor for solution of boundary-value problems."

The seminar summarized investigations and developments in the field of development and use of special processors for solution of boundary-value problems of field theory, made a decision on further development of the most promising scientific and applied works and contributed to strengthening the creative ties between developers and users of special processors.

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ROLE OF A. A. LYAPUNOV IN PROGRAMMING

Moscow PROGRAMMIROVANIYE in Russian No 1, Jan-Feb 82 pp 3-8

[Article by A. I. Kitov, N. A. Krinitskiy and R. I. Podlovchenko]

[Text] September 1981 marked 70 years since the birth of the prominent Soviet scientist Corresponding Member of the USSR Academy of Sciences Aleksey Andreyevich Lyapunov.

A. A. Lyapunov was an erudite scientist who worked fruitfully in many fields of science and who left a rich scientific heritage (a list of A. A. Lyapunov's papers, which number 205 titles, is published in [1]). The descriptive theory of sets, mathematical statistics, geophysics, biology, cybernetics, philosophy and pedagogy comprise an incomplete list of the fields in which A. A. Lyapunov worked.

A. A. Lyapunov's personal passion for science was combined with the unusual gift of attracting others to himself. Many successfully working scientists are now either direct students of A. A. Lyapunov or students of his students; those who experienced to one degree or another the influence of his scientific ideas are even more numerous.

One of the characteristic features of A. A. Lyapunov's scientific activity was his desire to work in new fields of science that had just become established, introducing mathematical methods of investigation in them. A clear example of this is his activity in cybernetics, which he began during the difficult years of its birth in our country. A. A. Lyapunov played an exceptionally important role in the establishment of cybernetics. The first article in the USSR in which the scientific content of cybernetics came to light and in which its place in the system of sciences was indicated was the article "Fundamental Features of Cybernetics," written by A. A. Lyapunov jointly with S. L. Sobolev and A. I. Kitov and published in the journal VOPROSY FILOSOFII in 1955. In later years A. A. Lyapunov was involved in theoretical investigations of the subject of cybernetics, classification of its basic directions and analysis of its problems and methods.

A new science was outlined from different scientific directions, methods, approaches and individual problems from positions of dialectical materialism and the subject of investigation and the range of fundamental problems were

determined. The results of these investigations are presented more clearly in an article [2] written in 1968. The subject of cybernetics is defined in this article in the following manner: "Cybernetics is the science of the general principles of constructing control systems and the flow of control processes."

In an article [3] that reveals a collection of the most significant works of A. A. Lyapunov in the field of theoretical and applied cybernetics, the following is stated: "A. A. Lyapunov carried out extensive work in comprehending the fundamentals of cybernetics, precise definition of its subject and classification of the basic concepts and problems." To this should be added that the establishment of such sections of cybernetics as programming, mathematical biology, machine translation and mathematical linguistics is related to A. A. Lyapunov's name.

A. A. Lyapunov's cybernetics period of activity encompasses the last 20 years of his life and begins with investigations in programming. This occurred at the beginning of the 1950s during the appearance of the first Soviet computers. A. A. Lyapunov was among those who immediately appraised the great revolutionizing role of computers in the life of man. Let us present the words with which begins the report that he prepared with his colleagues for the session of the USSR Academy of Sciences in automation in 1956 (see [3]):

"Modern electronic calculators have created a revolution in the field of application of mathematical calculations in natural science, engineering, economics and other fields, having much expanded the range of problems accessible to mathematical investigation. However, the significance of mathematical, logical and engineering principles that are the basis for development of electronic calculators goes far beyond the field of design and application of mathematical calculators themselves. These principles can be applied to development of a number of new automatic devices that free the human brain from performing many functions, the process of which can be described by a specific sequence of logic or arithmetic operations. Among these functions can be named those such as control of a number of production processes, dispatching in production or transport, processing and sampling of various types of information, translation from one language to another and so on."

The problems that comprised the theme of "artificial intelligence," as this scientific direction is now called, were actually formulated in this report.

A. A. Lyapunov became involved in determination of the principles of computer design from the first days of their appearance and at the time of the report the operator method of program that he developed had already achieved wide distribution both in practical programming and in courses on the teaching of programming.

The operator method of programming was first outlined in detailed form by A. A. Lyapunov in a series of lectures on programming that he read during the academic year of 1952/1953 for students of the chair of computer mathematics, mechanical and mathematics faculty, MGU [Moscow State University]. This course was then repeated many times to a wider audience. It was never

published as a whole, but individual chapters of it were used in [4-6] that were published only in 1957-1958.

In [5] A. A. Lyapunov formulated the problem of programming as a scientific direction and it consists in working out efficient methods of program compilation to solve problems on high-speed automatic digital computers.

For these purposes A. A. Lyapunov first replaced the variety of real computers by a single abstract machine that still embodied the basic features of design and functioning of real machines; he called it a conditional computer (see [5]). Its description is essentially an outline of the principles of designing computers, which in itself had great scientific value. The conditional computer became the bench to work out on it the procedures of programming and demonstration of the operator method in action.

Rational methods of program compilation can be developed only if there is a "rational" language to describe the algorithms to be programmed--a programming language. At this time the theory of algorithms had at its disposal several languages (Turing's machine, normal algorithms and recursive functions). However, none of them met the requirements which were placed on programming language (true at the cognitive level). This nonconformity follows from the difference of goals which are followed in developing language of the theory of algorithms and programming language. In the first case A. A. Lyapunov defines these goals thusly (see [7]): "The overall desire in development of systems of concepts in the theory of algorithms consists in reducing the number of elementary acts to a minimum and to maximum standardization of them. This significantly facilitates the establishment of the nonexistence of algorithms of one or another type." Talking in the same reference about programming language, A. A. Lyapunov notes: "Its purpose is to provide a convenient form of describing algorithms that are used to solve one or another problems." Thus, a new language was required.

The language that A. A. Lyapunov proposed was named the apparatus of logic circuits. It was written at the cognitive level. The elements from which programming algorithms are "made up" are determined within this apparatus: these are the operators that accomplish the act of information processing and the logic conditions that accomplish the act of information verification in order to determine the order of fulfillment of the operators. The description of the algorithm by operators and logic conditions was called the logic circuit of the algorithm by A. A. Lyapunov. Two levels of description--counting circuit and flow chart--were envisioned. A. A. Lyapunov defines these levels of description and their relationship with each other in the following manner (see [7]):

"The logic circuits of algorithms are used in programming in two different forms. On the one hand, the initial task (problem-solving algorithm--authors) is represented in the form of a logic circuit. Only the operators used to process the initial data of the problem are taken into account here. These circuits are called counting circuits. The operators contained in them are counting operators. To realize some algorithm in the computer, one must bring the computer memory to such a state after fulfillment of the next

counting operator that it fulfills the next counting operator or checks the next condition. Additional operators which prepare the state of the computer memory must be introduced for this. These additional operators are called control operators. The second form of the algorithm circuit--flow sheet--is called the logic circuit compiled of counting operators, control operators and logic conditions which determine the order of operation of the computer since the counting operators in all accessible initial data are fulfilled in the order which the counting circuit requires."

Making an analogy between counting circuits and flow charts on the one hand and our modern concepts on the other, one can say that the former are a representation of algorithms in high-level language and the latter are representation in a low-level language.

The logic circuit apparatus became the first language in the world that made it possible to talk about general programming procedures. The combination of these procedures was also named the operator method in programming. This is a method in which the program compilation process is represented in the form of a sequence of steps, each of which has a specific function. The input information for each step is writing the algorithm to be programmed in one language and the result is writing it in another language. The following steps are always provided: 1) transition from some initial description of the algorithm to its description in the form of a counting circuit, 2) transition from a counting circuit to a flow chart and 3) transition from a flow chart to the program itself.

The appearance of the logic circuit apparatus made it possible to talk about equivalent conversions of circuits and consequently to raise the question of improving program quality. The equivalence of the counting circuits was determined in this case by the requirement of the equality of functions implemented by these circuits (i.e., as functional equivalents in current terminology), while the equivalence of flow charts was determined be the requirement of the equality of a chain of counting operators to be carried out.

The operator method laid the basis of many programming handbooks published during the 1950s. This indicates its enormous pedagogical value. But the role of the operator is especially great in transformation of programming from a craft to a science having its own range of problems.

Designation of programming as a science consists in reducing the laboriousness of the programming process. The first specific tasks in this general path were clearly formulated only with the appearance of the operator method. These are primarily problems discussed directly by the operator method itself: 1) the problem of multilevel description of programming algorithms and development of languages used at individual levels, 2) the problem of developing algorithms for transition from objects of one level to objects of another level and 3) the problem of constructing optimization transformations of algorithms of one or another level.

The standardization of programming procedures established in the operator method was naturally aimed toward design of a programming routine, i.e., a

program which will itself construct programs for solving different problems. This problem was posed by A. A. Lyapunov in 1953 and determined the direction of investigations in programming that has been actively developed up to the present time.

A. A. Lyapunov assumed it was possible to begin design of a programming routine directly on the basis of logic circuit language. The first experiments in design of a programming routine were made in 1954 at MGU by graduate students of A. A. Lyapunov. These were alternate versions that had not been preserved up to the present. Many programming routines* were subsequently designed on the basis of logic circuit language and A. A. Lyapunov was consulted in some of these developments.

The work in development of programming routines comprises an important step in the history of Soviet programming, although the programs themselves did not find broad application in programming practice. A significant reason for this was the following circumstance: our computers of that time were equipped only with digital input and required manual coding of the initial algorithm.

In [8] A. A. Lyapunov designated the program of further investigations in this field; it briefly reduces to the following--intelligent classification of problems is required, languages are needed that are easily adaptable to these classes of problems and a specialized programming routine (oriented toward this language as the input language) should be developed on the basis of each of them.

And indeed work in development of a programming routine, being interrupted for some time, was restored after the first algorithmic languages oriented toward descriptions of algorithms of one or another class were developed and computers were equipped with symbolic input. It was restored in the form of work on compilation of translators from algorithmic languages. The experience acquired during development of programming routines was fully utilized and it is no accident that the first compilers of translators were the collectives headed by former developers of programming routines.

The development or translator and investigation of the principles of their development is the basic direction in modern programming. Its founder was A. A. Lyapunov.

Postulation of the problems that are the foundation of algebraic programming theory belongs to A. A. Lyapunov. Its objects are consideration of algorithms

*In 1954 E. Z. Lyubimskiy developed PP-1. One year later a collective consisting of M. R. Shura-Bura, E. Z. Lyubimskiy, S. S. Kamynin, V. S. Shtarkman, E. S. Lukhovistkaya and I. B. Zadykhaylo developed the considerably more improved PP-2. In 1956 A. P. Yershov, V. M. Kurochkin, L. N. Korolev, L. D. Panov and V. D. Podderyugin developed a programming program for the BESM computer; in 1957 N. A. Krinitskiy, A. M. Bukhtiyarov, G. D. Frolov, I. V. Pottosin, L. V. Voytishek and A. A. Levina developed PP-S for the Strela computer and so on.

as algebraic objects constructed in some alphabet, formal methods of introducing the relation of equivalents in a set of circuits and searching for algorithms for resolution of equivalents and designing a complete system of equivalent circuit conversions.

From its first days, logic circuit language was used not only to describe specific programming algorithms. A. A. Lyapunov suggests that a logic circuit be considered as description of a class of programs. In this case the operators and logic conditions contained in it are interpreted as arbitrary structural displays. A specific program is obtained from a circuit if a specific image is attached to each of its operators and logic condition--in other words, the symbols of operators and logic conditions are interpreted in some manner. Since some equivalence ratio is determined in a set of programs, it induces the equivalence ratio in a set of circuits. A. A. Lyapunov posed the problem of constructing an algorithm that recognizes the equivalence of flow charts and that searches for a complete system of equivalent circuit transformations.

If the equivalence ratio is introduced between programs by the feature of the equivalence of displays realized by the programs, then the circuit equivalence introduced by this ratio achieves convenient and adequate algebraic interpretation. In this case (and also for algebraic interpretation of the problem), the problems posed by A. A. Lyapunov were completely solved by Yu. I. Yanov (1957). The papers of Yu. I. Yanov are the first in algebraic programming theory. This scientific direction is being developed actively and serious theoretical and applied results have now been achieved in it.

A. A. Lyapunov paper "On Algebraic Interpretation of Programming" played an important role in development of programming and its theory [9]. It is devoted to formalization of the basic concepts of programming: programs, the process of fulfilling it, functions, the implemented routine of the equivalence ratio of programs and so on. This paper determined the approach to a development of the concept apparatus of programming.

A. A. Lyapunov's operator method was the first major scientific result in programming. An entire generation of programmers was reared on its basis. It provided the soil for numerous investigations in programming. In programming theory and practice, A. A. Lyapunov advanced those problems which determined for many years the direction of research in this field. And therefore we link the establishment of programming in our country to the name of A. A. Lyapunov.

Philosophical and methodological problems occupy a significant position in A. A. Lyapunov's scientific activity during the last years of his life. A. A. Lyapunov's concepts that were not published in his papers, but have been retained in the memory of his students, about such problems as the fundamentals of mathematics and the theory of algorithms, are interesting.

A. A. Lyapunov did not confine himself to a single one of the concepts that arose as a result of the third crisis of the foundations of mathematics, assuming that one must in each case make use of the mathematical apparatus and the terminology which are most convenient. For example, he did not feel

that constructive mathematics is any more competent than classical mathematics (and vice versa).

He suggested that the main designation of the theory of algorithms is not to serve as the foundation of mathematics but felt that it is of greater interest as an independent scientific discipline of interest and should be the methodology of the analysis and synthesis of algorithms.

In papers on the methodology of cybernetics and mathematics and on scientific kno ledge in general [1, part 5], he investigates the role of mathematics and cybernetics in modern society, the problems of providing a mathematical basis to science, the place of cybernetics among other sciences, general problems of the current state of scientific knowledge and classification of the sciences and the relationships of different scientific fields. These papers are essentially the result and journalization of his investigations and creative activity in different fields of science.

As a scientist, organizer of science and person, Aleksey Andreyevich is now a model second to none.

BIBLIOGRAPHY

1. Lyapunov, A. A., "Problemy teoreticheskoy i prikladnoy kibernetiki" [Problems of Theoretical and Applied Cybernetics], Moscow, Nauka, 1980.

2. Lyapunov, A. A. and S. V. Yablonskiy, "Theoretical Problems of Cybernetics," in "Problemy kibernetiki" [Problems of Cybernetics], No 3, Moscow, Fizmatgiz, 1963.

3. Lyapunov, A. A., M. V. Keldysh and M. R. Shura-Bura, "Mathematical Problems of Computer Theory," in "Problemy teoreticheskoy i prikladnoy kibernetiki," Moscow, Nauka, 1980.

4. Lyapunov, A. A. and G. A. Shestopal, "Initial Data on Solving Problems on Computers," in "Matematicheskoye prosveshcheniye" [Mathematical Education], No 1, Moscow, 1957.

5. Lyapunov, A. A., "Logic Flow Charts," in "Problemy kibernetiki," No 1, Moscow, Fizmatgiz, 1958.

6. Lyapunov, A. A., "Algorithms for Information Processing," IZVESTIYA VUZOV, RADIOFIZIKA, No 1, Gor'kiy, 1958.

7. Lyapunov, A. A., "Mathematical Problems of Cybernetics," IZVESTIYA VUZOV, MATEMATIKA, No 5, Kazan', 1958.

8. Lyapunov, A. A. and O. M. Yurkevich, "O problematike issledovaniy v oblasti programmirovaniya" [Problems of Research in the Field of Programming], Moscow, Nauka, 1980.

9. Lyapunov, A. A., "Algebraic Interpretation of Programming," in "Problemy kibernetiki," No 8, Moscow, Fizmatgiz, 1962.

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PUBLICATIONS

INDEX TO THE JOURNAL 'MEASUREMENTS, CHECKING, AUTOMATION' FOR 1981

Moscow IZMERENIYA, KONTROL', AVTOMATIZATSIYA in Russian No 6, Nov-Dec 81 pp 2, 50-51

[Text] The main purpose of the periodical scientific and technical reference collection IZMERENIYA, KONTROL', AVTOMATIZATSIYA (IKA), which has been published by the Central Scientific Research Institute of Information and Technical and Economic Research of Instrument Making, Automation Equipment and Control Systems, under the Ministry of Instrument Making, Automation Equipment and Control Systems, since 1974, is to systematically explain the latest achievements, analyses of the state of the art and prospects for development of current trends in the field of measurements, checking and automation.

There are typically two types of articles in the IKA collection:
encyclopedic (IKA-E), which are systematizing reviews briefly explaining the state of the art of a rather broad theme, and
articles on prospects, which cover trends and prospects for development, and the main scientific and technical problems of the current direction (IKA-P).

The material published in IKA is intended for a broad group of scientists, engineers and technicians engaged in development of new instruments and automation equipment and in design of automated control systems, workers in industrial enterprises producing and operating instruments and automation equipment, as well as instructors and students of upper-level courses in the higher educational institutions for corresponding specialties.

Index to Articles Published in the Scientific and Technical Collection IZMERENIYA, KONTROL', AVTOMATIZATSIYA in 1981

Makarov, I. M.
Scientific and Technical Problems of Robotization, IKA, 1981, No 4(38), pp 11-17..
Men'shikova, L. A.
Small Computers for Economic Calculations, IKA, 1981, No 2(36), pp 53-56.
Mikhotin, V. D.; Chuvykin, B. V. and Shakhov, E. K.
Methods of Synthesis of Weight Functions for Effective Filtration of Measurement Signals, IKA, 1981, No 5(39), pp 3-12.
Moskvich, V. A.
Organizational and Methodological Aspects of Forming Quality of New Equipment and Evaluating the Effectiveness of Its Development, IKA, 1981, No 2(36), pp 65-72.
Novoselov, O. N. and Plyushchev, A. V. and Fomin, A. F.
Methods and Means of Raising the Validity of Measurements of Continuous Processes, IKA, 1981, No 4(38), pp 3-10.
Pevsner, G. S.; Tsvetkov, E. I.; Tsodikov, M. B. and Shcherbakovskiy, G. Z.
Principles of Design of Parametric Series of Modular Facilities IKA, 1981, No 1(35), pp 3-8.
Petrovich, V. I.
Portable Balancing Instruments, IKA, 1981, No 6(40), pp 27-33.
Plonskaya, T. N.
State of the Art and Trends in Development of Microprocessors IKA, 1981, No 5(39), pp 73-77.
Prangishvili, I. V. and Stetsyura, G. G.
Current Status of the Problem of Developing a Computer with Nontraditional Structure and Architecture Controlled by a Data Stream, IKA, 1981, No 1(35), pp 36-48.
Pustyl'nikov, V. M.
Frequency and Time Converters of Information of Follow-Up Balancing IKA, 1981, No 1(35), pp 9-17.
Rozenberg, V. Ya.
Evolution of Concept of Uncertainty in Theory of Information Systems IKA, 1981, No 3(37), pp 53-63.
Rozenblat, M. A.
Cylindrical Magnetic Domain Devices for Information Storage and Processing IKA, 1981, No 4(38), pp 18-36.
Roytman, M. S.; Tsimbalist, E. I.; Ruzayev, Ye. N.; Kanunov, A. I. and Murav'yev, S. V., Design of Optimal Structures for Metrological Support Systems IKA, 1981, No 5(39), pp 13-18.
Sarkin, V. I. and Kruglov, M. G.
Facilities for Checking Geometric Parameters of Instrument Parts IKA, 1981, No 5(39), pp 50-60.
Serdyuk, G. B.
Integrated Diagnostics of Electrical and Radio Products IKA, 1981, No 3(37), pp 36-42.
Sinitsyn, B. S.; Belogorodskiy, S. A.; Zelenkov, A. A. and Miroshnichenko, O. G.
Application of Mathematical Statistical Methods in Analysis of Accuracy of On-Board Automated Control Systems, IKA, 1981, No 3(37), pp 43-52.
Stakhov, A. P.
Prospects for Application of Number Systems with Irrational Radices in Analog-to-Digital and Digital-to-Analog Conversion Technology, IKA, 1981, No 6(40), pp 3-9.

Taranenko, Yu. K.; Rezvitskiy, V. A.; Shalynin, V. D. and Yemets, S. I.
Vibration Level Gages, IKA, 1981, No 6(40), pp 20-26.
Tikhomirov, O. K.; Belavina, I. G. and Voyskunskiy, A. Ye.
Psychological Principles of Computer Software, IKA, 1981, No 1(35), pp 49-56.
Ulitskiy, M. B.
Methods and Algorithms for Preprocessing of Results from an Automated Physical Experiment, IKA, 1981, No 3(37), pp 64-73.
Utkin, V. I. and Kostyleva, N. Ye.
Principles of Design of Algorithmic Provisioning of Local Automation Systems with Variable Structure, IKA, 1981, No 1(35), pp 27-35.
Filinov, Ye. N.; Grobman, D. M. and Sergeyev, B. G.
Prospects for Development of Methods and Facilities for Checking Logic Circuits IKA, 1981, No 5(39), pp 61-65.
Khulap, G. S.; Tananov, A. I. and Akin'shin, V. S.
Prospects for Development of Facilities for Research and Checking of Quality of Structural-Nonhomogeneous Materials in a Broad Temperature Range IKA, 1981, No 2(36), pp 40-46.
Tsapenko, M. P.; Aliyev, T. M. and Klistorin, I. F., et al.
State of the Art and Prospects for Development of Measuring Information Systems IKA, 1981, No 5(39), pp 66-72.
Sheremet'yev, V. K.
Main Trends in Development and Standardization of Languages and Packages for Automated Process Control Systems, IKA, 1981, No 1(35), pp 57-65.

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REVERSIBLE MODELS

Moscow OBRATIMYYE MODELI in Russian 1981 (signed to press 4 Sep 81) pp 2-6, 115-121

[Annotation, introduction, section 5.6, bibliography and table of contents from book "Reversible Models" by Georgiy Yevgen'yevich Pukhov and Aleksandr Fedorovich Katkov, Izdatel'stvo "Nauka", 2150 copies, 121 pages]

[Text]

Annotation

This book is devoted to the theory and principles of executing direct and inverse mathematical transformations. Analog models of mathematical operations, algebraic and differential equations are examined along with digital models of logical and algebraic equations and hybrid algorithmic systems with reversible integrators for solving boundary problems.

The book is intended for students, engineers and graduate students. 84 illustrations, 2 tables, 85 bibliographic references.

Introduction

Modern society is characterized by intensive development of science and scientific research methods, one of the most powerful of which is the method of modeling. Modeling is based on similarity theory, and models are constructed so that the equations of the model and the equations of the object are similar, i.e., analogous. The use of analogy in the form of the mathematical expression for physical processes occurring in different objects with the processing occurring in electrical and electronic circuits has provided the basis for the development of the electrical modeling method.

Electrical modeling is a method for experimental investigation of physical processes under conditions which have a precise mathematical formulation. Similarity theory as applied to electrical analogs is used in order to extend the initial data and the solutions obtained. In order to do this, the similarity criteria are defined which establish the relationship between the analogous quantities in the electrical models and the physical processes being investigated.

The functional capabilities of the electrical modeling method are expanded significantly by using the method of quasi-analogies, which is based on the principle of equivalence between the objects of the equation and of the model in terms of the results obtained. Similitude between the equations of the physical process and of the electrical model is achieved in quasi-analog models when certain conditions, called equivalence conditions, are satisfied [51, 56].

As modeling technique develops, the criteria by which the modeling devices are divided with respect to the quantities with which they operate into continuous (analog) and discrete (discrete) becomes increasingly conditional. In view of various practical considerations it is sometimes more convenient to use discrete codes to represent the modeled quantities, while analog representation may be more convenient in other cases. It may be the case that the structure of the connections between the modeled quantities is fully defined by the singularities of the discrete model, while the modeled quantities themselves, being elements of a discrete set, are not analogous to the modeled quantities, which are elements of a continuous set. The correspondence between these is established according to the principles of logical equivalence or class analogies. In one case the original system of equations is solved by modeling of equations which are similar bit by bit to the original equations in finite word length; in the other case, a system of logical equations is modeled which is logically equivalent to the assigned system in the sense of closeness of the results obtained. If the modeling is done in continuous time in both cases and the model is a digital automaton, it is convenient to call the latter the modeling automaton. The problem of synthesis in investigating such automata is urgent, since "life is moving to the forefront of exploratory research the need for studying objects (automata) which function in continuous time and which, strictly speaking, cannot be related definitely either to continuous dynamic systems or to discrete automata" [17].

The modeling devices which are in extensive use are not reversible. This means that the external poles of the model are strictly divided into input and output. The fact that the external poles are not equivalent limits the group of problems which can be solved, and prevents the same model from being used to obtain a solution to equations for different groups of variables.

Models in which the initial quantities can be assigned on any set of external poles and in which quantities satisfying the system of modeled equations can be obtained on the remaining poles are called reversible. These models are needed in constructing automatic control systems, and in designing objects when it is necessary to be able to use the results of experimental investigations, which are in the general case the solutions of certain systems of equations, to determine the external effects to which the objects are subjected during the experiment, i.e., to solve a group of reversible problems.

The first publications on the theory of models having the property of reversibility appeared in the late 1950s and early 1960s: this includes A.N. Lebedev's work [43, 44] on quasi-reversible models with artificial reversibility, as well as G.Ye. Pukhov and B.A. Borkovskiy's work on reversible models [55, 58] and G.Zh. Yuffler's study [78].

The entire set of models which have reversibility properties can be divided into three groups. The first group is made up of reverse information models, i.e., models in which reverse cause-and-effect relationships are modeled. The reverse information model of a process which develops over time follows various criteria, usually probabilistic, based on experience or model learning, to find the set of event circuits which lead to a known effect [48].

The second group includes reversible models with equivalent external poles. Information may be assigned on each of these poles, depending upon the conditions of the problem, and a result satisfying the required mathematical relationship can be obtained [54, 55, 58]. There are reversible models with natural and artificial reversibility.

Models with natural reversibility are reversible models constructed using physical principles of conservation, as well as models for which the mathematical notation for the operating principle has the nature of the principle of conservation due to a defined set of parameters of the modeling device.

Artificially reversible models which accommodate a set of individual models of direct and inverse mathematical relationships in a defined manner are called reversible models with multichannel structure. Symmetrical reversible models are a special case of these. The external poles of these devices are equivalent in the sense of assigning or obtaining information, and the device as a whole has the property of symmetry. When information is assigned on any group of poles, the result of the modeling of the same mathematical operation is obtained on the remaining poles. For example, a symmetrical reversible logical AND circuit outputs the corresponding values of the logical AND function on the third pole when information is assigned on either of the other two poles.

The broadest group is made up of artificially reversible models obtained using balancing devices. These have the property of reversibility due to the use of various tracking system circuits which act as balancing devices and due to constructing the external poles such that the input signals are capable of controlling the structure of the model. Depending upon the method by which the modeled quantities are represented and the principle by which the balancing device is constructed, it is convenient to divide these models into analog, logical, digital and hybrid.

In reversible analog models, the balancing device is a d.c. amplifier, which is called a generating amplifier below since it generates a null potential voltage level at its input over the corresponding feedback circuits when connected to the modeling circuit. The role of the balancing device in logical reversible models is played by logic circuits which execute mod 2 summation. Digital reversible models use digital tracking systems, while in hybrid models the information can be assigned in either digital or analog form. Combining digital and analog reversible modeling circuits into a unified modeling system in which the individual parts are connected by reversible data converters makes it possible to create hybrid reversible modeling systems.

Finally, the third group includes quasi-reversible models which model mathematical relationships which are the inverse of direct relationships by means of

switching operations which cause the structure of the model to change.

The present work investigates reversible models with balancing devices.

The book consists of five chapters.

Chapter 1 is devoted to general questions of the reversibility of models and phenomenon. It briefly presents information concerning the reversibility of physical systems and mutuality principles, which are often identified with the reversibility property when applied to electrical circuits; the principles behind the construction of reversible models with natural and artificial reversibility reversibility are also examined.

Based on the general principles of synthesizing quasi-analog modeling devices, chapter 2 presents methods for constructing reversible and quasi-reversible models of linear and nonlinear algebraic and differential operators.

Chapter 3 is devoted to dynamic reversible models in which the required mathematical relationships are modeled in a process of continuous switching of the generating amplifier.

After a brief exposition of questions associated with the theory of point calculus, chapter 4 examines the construction principles of reversible point integrators and the structures of hybrid systems based on them for solving differential equations with complex boundary conditions.

Chapter 5 is devoted to reversible modeling automata -- digital models in which reversibility is attained by using digital tracking systems and special construction of the external poles. This chapter examines reversible models of elementary logical functions, systems of logical equations, as well as symmetrical reversible logic circuits. This chapter concludes with an exposition of the construction principles of reversible hybrid systems with reversible data converters.

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5.6. Hybrid Models

There is a great deal of attention to problems of hybridizing computing devices in the scientific and technical literature. This interest is associated with the need for creating computers which are economically more efficient, faster and more accurate than existing computers. Many authors believe that it is possible to construct machines which combine these features by combining different methods of representing the information and principles for processing it. In order to reduce the amount of hardware and increase economic efficiency while realizing high speed and accuracy, it is possible to combine methods of representing the information and processing it within each operating unit, or within the entire computing system. Modeling systems which are built from such operational units can be called hybrid modeling systems (HMS). We shall consider HMS in which the

digital section is executed in the form of modeling automata. The following basic ways of constructing HMS are possible.

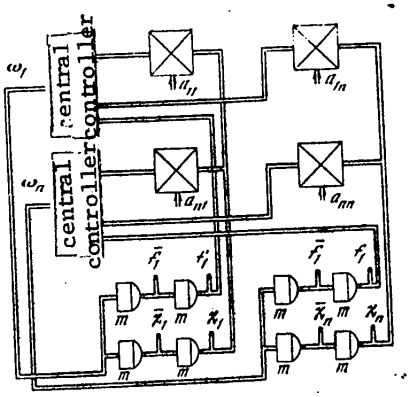

Figure 5.35

1. HMS using hybrid method of representing information and processing it at operational unit level.

2. HMS which combine operational units which work with information represented in different forms.

The first construction method is based on representing the information within each operational unit of the computer in hybrid form. For example, in coarse systems, the main part of each variable is represented in digital form, while the rest of it is represented in analog, i.e., $x = x_d + x_a$. The operational unit in such hybrid modeling systems consists of two sections - digital and analog - which are interconnected by carry circuits and a device which generates the sign of the result. The operating principle of the digital and analog circuits is identical - the result is obtained in the modeling process.

An adder which operates with information represented in hybrid form consists of the following units: the sign adder, which generates the sign of the result of the operation; the digital parallel adder, which adds the digital parts of the input terms; and the analog adder which adds the parts of the input signals which are represented in analog form. These summator units operate in parallel; therefore, the device outputs a signal when signals appear at the inputs after completion of the transient processes in the circuit.

Most of the elements which are needed to construct the operational units which operate with information represented in hybrid form are familiar. Building HMS from such operational units consists of connecting them in accordance with the structural programming method which is characteristic for analog computing

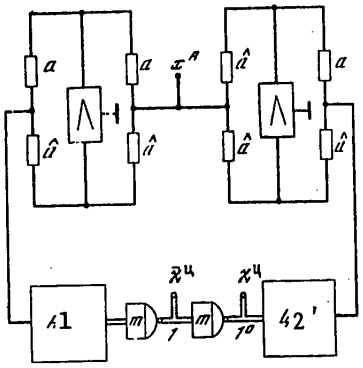

Figure 5.36

Key: 1--analog-digital converter; 2--digital-analog converter

equipment. In constructing the structural circuit to solve the problem, the outputs of the sign units and digital and analog sections of one group of hybrid modeling operational units are connected to the inputs of the sign, digital and analog units of the other operational units respectively.

When the conditions for stable system operation, as well as the equivalence or similarity conditions of the equations of the problem to be solved and the equations which are described by the hybrid model are satisfied, the corresponding operational units will output the solution to the problems. The accuracy of the solution is determined by the word length of the digital section of the operational units, and the time required to solve the problem in modeling non-inertial objects described by finite equations will be comparable to the decay time of the transient processes in the electronic circuits of the system.

By combining analog reversible models and reversible modeling automata it is possible to create reversible HMS. The reversible units which operate with information represented in different forms must be connected through reversible data converters [62, 68].

Figure 5.36 shows the diagram of a reversible data converter. It consists of two reversible analog inverters, an analog-digital converter and a digital-analog converter. In order to assign information in digital form, it is represented in paraphase code. A special construction of the circuits connected to the external poles is used whose operating features were examined above. If a quantity x^A is assigned, it is input to the reversible inverter, after which the analog-digital converter converts it to a parallel digital m-bit code which is input to the digital-analog converter through the logical inverter units. The digital-analog converter outputs an analog quantity equal to $-x^A$. This quantity is input to the second analog reversible inverter and re-converted to its original form. When this is done, the quantity x^D is output in digital code by the output poles 1, 1^0. An analogous situation occurs if the quantity x^D is assigned in digital form in parallel m-bit code. This is first converted to an analog quantity, then the sign is reversed twice in the reversible analog inverters, converted to code in the analog-digital converter and output at poles 1, 1^0. The quantity $-x^A$ is

output at the pole which is common to both of the reversible inverters.

A reversible HMS can consist of a reversible analog model, a reversible modeling automaton, a reversible data converter and devices for inputting and outputting information represented, respectively, in analog and digital form. An interesting point is that each of these computing units is a modeling unit, and a unified hybrid modeling system can be built from such units only if each of them is reversible.

BIBLIOGRAPHY

1. Asmakhnovskiy, A.G., Varshavskiy, V.I., Marakhovskiy, V.B., et. al. Aperiodicheskiye avtomaty (Aperiodic Automata). Moscow, Izdatel'stvo Nauka, 1976

2. Bellman, R., Kalaba, R., Metod kvazilinearizatsii i nelineynye krayevye zadachi (Quasi-Linearization Method and Nonlinear Boundary Problems), Moscow, Izdatel'stvo Mir, 1968

3. Verezovenko, G.Ya., "Toward the Theory of the Point Method". In Elektronika i modelirovaniye: Tsifrovye analogi (Electronics and Modeling: Digital Analogs), Kiev, Izdatel'stvo Nauk. Dumka, 1974

4. Vorkovskiy, B.A., "Calculation of Balanced Rectifier Circuits Using Point Method", Tr. Taganrog. radiotekh. in-ta, 1954, No. 1

5. Borkovskiy, B.A., "Calculation of Periodic Processes in Nonlinear Electrical Circuits with Rectifiers", Doctoral Dissertation. Tomsk, Polytechnical Institute, 1955

6. Borkovskiy, B.A., "Determination of Eigenvalues and Eigenvectors of Matrices of Reversible Electronic Models", In Matematicheskoye modelirovaniye i elektricheskiye tsepi (Mathematical Modeling and Electrical Circuits), Kiev, Izdatel'stvo Nauk. Dumka, 1965, No. 5.

7. Borkovskiy, B.A., "Dynamic Modeling of Non-Inertial Objects", KIBERNETIKA, No. 3, 1965

8. Borkovskiy, B.A., "Dynamic Modeling of Differential Equations", KIBERNETIKA, No. 6, 1965

9. Borkovskiy, B.A., "Theory of Quasi-Analog Integrating Machines Based on Modeling of Algebraic Operators Using Inductances and Capacitances", In voprosy teorii i primeneniya matematicheskogo modelirovaniya (Problems of Theory and Application of Mathematical Modeling), Moscow, Izdatel'stvo Sov. radio 1965

10. Borkovskiy, B.A., Vollerner, A.N., Kamkov, A.F. et. al., Modeliruyushchiye matematicheskiye mashiny peremennoy struktury (Modeling Mathematical Machines With Variable Structure), Kiev, Izdatel'stvo Nauk. Dumka, 1970

11. Borkovskiy, B.A., Galuzichkiy, G.P., Kamkov, A.F., Romantsov, V.P., Algoritmicheskiye gibridnye sistemy (Algorithmic Hybrid Systems), Kiev, Izdatel'stvo Nauk. Dumka, 1972

12. USSR Patent 402146. "Data Converter." B.A. Borkovskiy, A.F. Katkov, V.P. Romantsov. Application Date 21 Jan 1972, No. 1737080/26-9; Published in B.I., No. 41, 1973

13. Borkovskiy, B.A., Kamkov, A.F., Romantsov, V.P., "Reversible Logic and Algebraic Converters", in Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Theory of Electrical Circuits), Kiev, Izdatel'stvo Nauka Dumka, 1975, No. 13

14. USSR Patent 504195. Digital Function Generator. B.A. Borkovskiy, A.F. Katkov, V.P. Romantsov, Ye.T. Lyashuk. Application date 2 Jan 1974, No. 1982665/18-24; published in B.A., No. 7, 1976

15. USSR Patent No. 486331. Device for Modeling Systems of Logical Equations. B.A. Borkovskiy, A.F. Katkov, V.P. Romantsov. Application date 2 Jan 1974, No. 1982667/18-24; published in B.I., No. 36, 1975

16. Borkovskiy, B.A., Kamkov, A.F., Romantsov, V.P., "Reversibility of Computer Modeling Devices", In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Theory of Electrical Circuits), Kiev, Izdatel' stvo Nauka Dumka, 1977, No. 5.

17. Burlenko, N.P., Modelirovaniye slozhnykh sistem (Modeling Complex Systems), Moscow, Tzdatel'stvo Nauka, 1968

18. Budinskiy, Ya., Logicheskiye tsepi v tsifrovoy tekhnike (Logical Circuits in Digital Technology), Moscow, Izdatel'stvo Svyaz', 1977

19. Vasil'ev, V.V., Klepikova, A.N., Timoshenko, A.G., Resheniye zadach optimal'nogo planirovaniya na elektronnykh modelyakh (Solution of Optimal Planning Problems on Electronic Models), Kiev, Izdatel'stvo Nauka Dumka, 1966

20. Verlan', A.F., "Some Principle Properties of Reversible Electronic Models" In Elektronika i modelirovaniye (Electronics and Modeling), Kiev, Izdatel'stvo Nauk. Dumka, 1975, No. 7

21. Voronov, A.A., Garbuzov, A.R., et. al., Tsifrovye analogi dlya sistem avtomaticheskogo upravleniya (Digital Analogs for Automatic Control Systems), Moscow, Leningrad, Izdatel'stvo An SSSR, 1960

22. Gantmakher, F.R., Teoriya matrits (Matrix Theory), Moscow, Izdatel'stvo Nauka, 1967

23. Godunov, S.K., Ryaben'kiy, V.S., Raznostnye skhemy (Difference Circuits), Moscow, Izdatel'stvo Nauka, 1973

24. Gutenmakher, L.I., Elektricheskiye modeli (Electrical Models), Moscow, Leningrad, Izdatel'stvo AN SSSR, 1949

25. Zhuk, K.D., "Reversible Functional Converter" In Matematicheskoye modelirovaniye i elektricheskiye tsepi (Mathematical Modeling in Electrical Circuits), Kiev, Izdatel'stvo AN Ukr SSR, 1963, No. 1

26. Zelyakh, E.V., Osnovy obshchey teori lineynykh elektricheskikh skhem (Fundamentals of General Theory of Linear Electrical Circuits), Moscow, Izdatel'stvo AN SSSR, 1951

27. Kalyayev, A.V., Vvedeniye v teoriyu tsifrovykh integratorov (Introduction to Theory of Digital Integrators), Kiev, Izdatel'stvo Nauk. Dumka, 1964

28. Kartsev, M.A., Arifmetika tsifrovykh mashin (Arithmetic of Digital Machines), Moscow, Nauka Press, 1969

29. Kamkov, A.F., "Reversible Dynamic Models of Mathematical Operations", In Analogovaya i analogo-tsifrovaya vychislitel'naya tekhnika (Analog and Analog-Digital Computing Equipment), Moscow, Izdatel'stvo Sov. radio, 1968, No. 2

30. Kamkov, A.F., "Investigation of Dynamic Reversible Models", Doctoral Dissertation, Kiev, Ukrainian SSR Academy of Sciences Cybernetics Institute, 1968

31. Kamkov, A.F., Romantsov, V.P., "Hybrid Model for Solving Boundary Problems", VOPR. RADIOELEKTRONIKI SER. VYCHISL. TEKHNIKA, No. 2, 1971

32. Kamkov, A.F., "Convergence of One Method of Solving Boundary Problems on Hybrid Quasi-Analog System", In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Theory of Electrical Circuits), Kiev, Izdatel'stvo Nauk. Dumka, 1971, No. 9

33. Kamkov, A.F., Romantsov, V.P., "Questions of Scaling Variables in Solving Problems on Hybrid System", In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Theory of Electrical Circuits), Kiev, Izdatel'stvo Nauk. Dumka, 1972, No. 10

34. Kamkov, A.F., "Hybrid Class Systems", ibid, No. 11

35. Kamkov, A.F., Romantsov, V.P. "Principle of Construction of Reversible Combination Circuits", ibid.

36. Kamkov, A.F., Romantsov, V.P., "Homogeneous Digital Grids for Solving Equations of Mathematical Physics", ibid, No. 12

37. USSR Patent 414604. Integrator. A.F. Katkov, Application date 28 Feb 1974, No. 1752345/18-24; published in B.I., No. 5, 1974

38. Kamkov, A.F., "Homogeneous Modeling Asynchronous Logical Networks With Feedback', In Odnorodnyye vychislitel'nyye sistemy (Homogeneous Computing Systems), Kiev, Izdatel'stvo Nauk. Dumka, 1975

39. Kamkov, A.F., "Principle of Logical Equivalence and Synthesis of Modeling Logical Networks", In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Theory of Electrical Circuits), Kiev, Izdatel'stvo Nauk. Dumka, 1976, No. 14.

40. Kamkov, A.F., "Digital Generating Amplifier for Codes and Balancing Logical Circuits", Preprint No. 224: Spetsializirovannyye protsessory (Special-Purpose Processors), Kiev, Ukrainian SSR Academy of Sciences Electrodynamics Institute, 1980

41. Kozan, B.M., Ter-Mikaelyan, T.M., (Solution of Engineering Problems on Digital Computers), Moscow, Leningrad, Izdatel'stvo Energiya, 1964

42. Levin, V.I., "Infinite-Valued Logic and Transient Processors in Finite Automata", AVT, No. 6, 1972

43. Lebedev, A.N., Modelirovaniye transtsendentnykh uravneniy (Modeling Transcendental Equations), Leningrad, Izdatel'stvo Sudpromgiz, 1963

44. Lebedev, A.N., Schetno-reshayushchiye ustroystva (Computing Devices), Moscow, Izdatel'stvo Mashinostroyeniye, 1966

45. Lomonosov, Yu.V., "Periodic Processes in Nonlinear Circuits", ELEKTRICHESTVO, No. 7, 1952

46. Muller, P., Teoriya pereklyuchatel'nykh skhem (Theory of Switching Circuits), Moscow, Izdatel'stvo Nauka, 1971, Vol. 2

47. Milyakh, A.N., Pidlovskiy, A.K., Printsip vzaimnosti i obratimost' yavleniy v elektrotekhnike (Mutuality Principle and Reversibility of Phenomena in Electrical Engineering), Kiev, Izdatel'stvo Nauk. Dumka, 1975

48. Novorusskiy, V.V., "Reverse Conversion of Data in Control Problems", In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Theory of Electrical Circuits), Kiev, Izdatel'stvo Nauk. Dumka, 1971, No. 8

49. Pospelov, D.A., Logicheskiye metody analiza i sinteza skhem (Logical Methods of Analyzing and Synthesizing Circuits), Moscow, Izdatel'stvo Energiya, 1974

50. Pukhov, G.Ye. "Introduction to Point-Method Theory", TR. TAGANROG. RADIOTEKH. IN-TA, No. 1, 1954

51. Pukhov, G.Ye., Borkovskiy, B.A., "Construction Principles of Quasi-Analog Models of Systems of Linear Algebraic Equations" In Tr. Vsesoyuz konf. po modelirovaniyu (Proceedings of All-Union Conference on Modeling), Moscow, Izdatel'stvo MEI, 1962

52. USSR Patent 149128. Operational Amplifier (Reversible), G.Ye. Pukhov. Application date 3 Nov 1961, No. 750272/26-24; published in B.I., No. 15, 1962

53. Pukhov, G.Ye., "Use of Quasi-Negative Resistances to Improve Operating Mode of Amplifiers in Reversible Model of Linear Equations", In Matematicheskoye modelirovaniye i elektricheskiye tsepi (Mathematical Modeling and Electrical Circuits), Kiev, Izdatel'stvo AN Ukr SSR, No. 1, 1963

54. Kukhov, G.Ye., "Reversible Quasi-Analog Models, Their Theory and Some Applications", IZV. VUZOV. ELEKTROMEKHANIKA, No. 2, 1963

55. Kukhov, G.Ye., "Possibility of Building Mathematical Controller Using Reversible Computing Elements", In Matematicheskoye modelirovaniye i elektricheskiye tsepi (Mathematical Modeling and Electrical Circuits), Kiev, Izdatel'stvo AN Ukr SSR, No. 1, 1963

56. Pukhov, G.Ye., Izbrannye voprosy teorii matematicheskikh mashin (Selected Questions of Theory of Mathematical Machines), Kiev, Izdatel'stvo AN Ukr SSR, 1964

57. Pukhov, G.Ye., "A Method for Obtaining Potential-Null Points", KIBERNETIKA, No. 2, 1965

58. Pukhov, G.Ye., Borkovskiy, B.A., "Methods for Constructing Reversible and Quasi-Reversible Models", In Metody analiza i sinteza elektronnykh kvazianalogovykh tsepey (Mathematical Modeling and Electrical Circuits), Kiev, Izdatel'stvo AN Ukr SSR, No. 2, 1965

59. Pukhov, G.Ye., Metody analiza i sinteza elektronnykh kvazianalogovykh tsepey (Methods of Analyzing and Synthesizing Electronic Quasi-Analog Circuits), Kiev, Izdatel'stvo Nauk. Dumka, 1967

60. USSR Patent 194436. Reversible Integral-Differentiating or Adding Device. G.Ye. Pukhov, A.N. Vollerner, A.F. Katkov. Application date 18 Mar 1966, No. 1061281/26-24; published in V.I., No. 8, 1967

61. Pukhov, G.Ye., Vasil'yev, V.V., Yevdokimov, V.F., et. al., "Promising Areas of Development of High Speed Computers", In Matematicheskoye modelirovaniye i elektricheskiye tsepi (Mathematical Modeling and Electrical Circuits), Kiev, Izdatel'stvo Nauk. Dumka, 1972, No. 10

62. USSR Patent 409233. Data Converter. G.Ye. Pukhov, A.F. Katkov, V.P. Romantsov, Application date 21 January 1972, No. 1742186-18-24; published in V.I., No. 48, 1973

63. USSR Patent 432491. Device for Solving Systems of Algebraic Equations. G.Ye. Pukhov, B.A. Borkovskiy, Yu.N. Gruts, A.F. Katkov, V.P. Romantsov. Application date 21 January 1972, No. 1741661/18-24; published in P.I., 1974, No. 22

64. Pukhov, G.Ye., "Digit Equations, Their Composition, Solution and Modeling", In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Electrical Circuit Theory), Kiev, Izdatel'stvo Nauk. Dumka, No 74, No. 12

65. Pukhov, G.Ye., Kamkov, A.F., Romantsov, V.P., "Principles of Constructing Ordering Analogs from Combination Operational Units", In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Electrical Circuit Theory), Kiev, Izdatel'stvo Nauk. Dumka, 1975, No. 13

66. Pukhov, G.Ye., Evdokimov, V.F., Sin'kov, M.V. Razryadno-analogovye vychislitel'nye sistemy (Digit - Analog Computing Systems), Moscow, Izdatel'stvo sov. radio, 1978

67. Pukhov, G.Ye., Yevdokimov, V.F., Sin'kov, M.V. et. al., "Hybrid High-Precision High-Speed Computing Systems" In VI Vsesoyuznoye soveshchaniye po matematicheskomu modelirovaniyu i metodam gibridnykh vychisleniy (Sixth All-Union Conference on Mathematical Modeling and Methods for Hybrid Computation). Report abstracts. Moscow, Izdatel'stvo IAT, 1972

68. Romantsov, V.P., "Reversible Data Converters" In Matematicheskoye modelirovaniye i teoriya elektricheskikh tsepey (Mathematical Modeling and Electrical Circuit Theory), Kiev, Izdatel'stvo Nauk. Dumka, 1975, No. 13

69. Romantsov, V.P., "Investigation of Transient Processes in Digital Combination Models of Algebraic Equations", ibid.

70. Romantsov, V.P., "Dynamic Method for Localizing LSI Faults", In Preprint: Spetsializirovannye protsessory (Special-Purpose Processors), Kiev, Ukranian SSR Academy of Sciences Electrodynamics Institute, 1980

71. Smolov, V.B., Analogovye vychislitel'nye mashiny (Analog Computers), Moscow, Izdatel'stvo vysshaya shkola, 1972

72. Strett, Dzh.V. (Lord Rayleigh), Teoriya zvuka (Theory of Sound), Moscow, Gostekhizdat, 1955, Vol. 1

73. Tetel'baum, I.M., Tetel'baum, Ya.I., Modeli pryamoy analogii (Direct Analogy Models), Moscow, Izdatel'stvo Nauka, 1979

74. Feynman, P., Kharakter fizicheskikh zakonov (The Nature of Physical Laws), Moscow, Izdatel'stvo Mir, 1968

75. Khemming, R.V., Chislennye metody (Numerical Methods), Moscow, Izdatel'stvo Nauka, 1968

76. Shannon, C. "Mathematical Theory of Differential Analyzer", In Raboty po teoryi informatsii i kibernetike (Works in Information Theory and Cybernetics) Moscow, Izdatel'stvo Inostr. Lit., 1963

77. Shannon, C., "Computing Devices and Automata", ibid.

78. Yuffler, G.Zh. "New Type of Universal Mathematical Machine" In Trudy Kongressa IFAK (Proceedings of IFAK Congress), Moscow, Izdatel'stvo AN SSSR, 1961, Vol. 3

79. Joseph O., Campeau. The Synthesis and Analysis of Digital System by Boolean Matrices, Ire, V EC-6, 1957, N. 4, Dec.

80. McCallum, D.M., Smith, J.B., Mechanized Reasoning, Electron. Eng. (Cr. Brit.), 1951

81. Borkovskiy, V. Ad., Katkov, A.F., Romantsov, V.R., Asynchronous Logical Nets With Feedback for Dynamic Systems Modeling, In: Proc. Symp. on Hybrid Comp. in Dynamic Systems Design. Rome (Italy), 1974.

82. Pukhov, G.Ev., Borkovskiy, V.Ad., Katkov, A.F. et. al. A Hybrid System With Analog Integrators of Discrete Functions. Tokyo: AICA, 1971

83. Pukhov, G.Ev., Katkov, A.F., Evdokimov, V.F., Romantsov, V.P., Hybrid Digit Computers, Prague, 1973, Vol. of Congr. 7th AICA.

84. Pukhov, G.E., Caluzinsky, G.P., Katkov, A.F., Romantsov, V.P., Dispositif d'integration et de differentiation d'ne fonction diskrete. Pat. 2.119.195 (Republique Francaise), 1972

85. Pukhov, G.E., Borkovskiy, B.A., Belik, V.K., Katkov, A.F., Romantsov, V.P., Device for Integrating and Differentiating Discrete Functions. Pat. 3.786.241 (USA), 1974

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