

Central Intelligence Agency



Washington, D.C. 20505

MEMORANDUM FOR: Chief, Policy and Planning Staff,
Intelligence Community Staff

SUBJECT: Supercomputers

REFERENCE: Your Memorandum, dtd 26 January 1983, Same
Subject, DCI/ICS 83-4224

1. In the Reference, you asked CIA to respond to a set of questions on supercomputers. Brief answers to these questions are provided in the attachment.

2. From a CIA perspective, there are two main points we would like to make concerning supercomputers. First, we are currently uncertain as to whether we have definite requirements for a supercomputer capability. In fact, we are investigating this very issue at this time. We, therefore, have not made a decision to acquire a supercomputer. We believe that this would be a costly and complex exercise and are not prepared to proceed until we are convinced that the benefits outweigh the costs.

3. Second, we are quite concerned about being limited to foreign sources (presumably Japanese) should we decide to acquire a supercomputer. Agency policy generally prohibits the use of foreign ADP resources. This policy is derived from security concerns only. That is, in our judgment, the use of foreign ADP resources greatly increases our vulnerability to manipulation by a hostile intelligence service. Therefore, we believe domestic sources for supercomputers should be fostered. How to do this, however, is a complex policy question for which we have no simple answer at this time.

25X1

Executive Director

Attachment: a/s

25X1

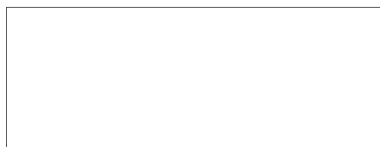
SECRET

U/FOUO when Separated from Attachment

ES

~~No checking~~

Response in yet?



25X1

EXECUTIVE SECRETARIAT

Routing Slip

TO:		ACTION	INFO	DATE	INITIAL
1	DCI				
2	DDCI				
3	EXDIR		X		<i>[Handwritten Signature]</i>
4	D/IGS				
5	DDI		X		
6	DDA		X		
7	DDO		X		
8	DDS&T		X		
9	Chm/NIC				
10	GC				
11	IG				
12	Compt				
13	D/EEO				
14	D/Pers				
15	D/OEA				
16	C/PAD/OEA				
17	SA/IA				
18	AO/DCI				
19	C/IPD/OIS				
20	D/ODP	X			
21					
22					
		SUSPENSE	4 Feb		
			Date		

Remarks:
 Please coordinate with all Directorates and prepare a response for EXDIR's signature.

[Signature]

Executive Secretary
 28 January 1983
 Date

25X1

UNCLASSIFIED INTERNAL USE ONLY CONFIDENTIAL SECRET ✓

ROUTING AND RECORD SHEET

SUBJECT: (Optional)

Supercomputers

FROM: [Redacted] EXTENSION: [Redacted] NO. [Redacted]
 Chief, Policy & Planning Staff
 Intelligence Community Staff
 DATE: 26 January 1983

TO: (Officer designation, room number, and building) DATE RECEIVED DATE FORWARDED OFFICER'S INITIALS COMMENTS (Number each comment to show from whom to whom. Draw a line across column after each comment.)

	TO: (Officer designation, room number, and building)	DATE		OFFICER'S INITIALS	COMMENTS (Number each comment to show from whom to whom. Draw a line across column after each comment.)
		RECEIVED	FORWARDED		
1.	Executive Director, CIA Rm. 7E-12 Hqs.			[Redacted]	
2.					
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15.					

The Director of Central Intelligence

Washington, D.C. 20505

Intelligence Community Staff

DCI/ICS 83-4224
26 January 1983

MEMORANDUM FOR: Director, Defense Intelligence Agency
Director, National Security Agency
Executive Director, Central Intelligence Agency

VIA: Acting Director, Intelligence Community Staff *ERP/ks*

FROM:
Chief, Policy & Planning Staff

SUBJECT: Supercomputers

1. The ad hoc committee on Supercomputers convened by the Office of Science & Technology Policy (O/S&TP) met on 24 January 1983 to review the many issues on this subject. The opinions and proposals presented differed dramatically; consequently, no consensus could be developed. Doug Pewitt, Assistant Director, O/S&TP, tasked the members to respond to the following questions by Monday, 7 February 1983.

- A. Do you currently own and operate or time share a supercomputer? How many or how much usage?
- B. Do you have firm plans to acquire the next generation supercomputer? What specs? When? How many? Approximate dollar funds per supercomputer?
- C. Is there a difference in your requirement between a "big number cruncher" and an even bigger and more complex AI-based machine?
- D. Have you identified a US source or sources?
- E. What impact would a successful Japanese fifth generation and supercomputer with the approximate performance characteristics have on your agency? (See attachment)
- F. Is there a role for the federal government in stimulating, partially funding, or actually developing the fifth generation supercomputer. One body of opinion asserts the US Government should only indicate the range of performance characteristic desired, the best estimate on quantity required and probable time frame for delivery with a tolerable price range.
- G. Do you have an opinion on the probable success or range of performance the Japanese are likely to achieve? Basis for opinion?

UNCLASSIFIED



2. My assessment is that there is not now a strong commitment for US Government involvement in any aspect of the next supercomputer, nor to any concentrated reaction to the potential Japanese computer project.

25X1 3. Please provide me your comments (which may be classified if
appropriate) by noon, Monday, 7 February. I will provide them to
25X1 [redacted] office and will obtain and circulate all members' comments for
your individual review and comment prior to developing an Intelligence
Community position.



Attachment:
Japanese Computer Specifications
(20 Charts)

UNCLASSIFIED

SUBJECT: Supercomputers.

Distribution: (DCI/ICS 83-4224)

- 1 - each addressee w/att
- 1 - ER w/att
- 1 - A-D/ICS w/o att
- 1 - ICS Registry w/att
- 25X1 1 - ICS/Info Handling Committee Staff ¹¹⁵⁷ w/att
- 1 - ICS/PPS Subject (Supercomputers) w/att
- 1 - ICS/PPS Chrono w/o att

25X1 DCI/ICS/PP: (26 Jan 83)

JAPANESE GOALS

JAPANESE GOVERNMENT (MITI) AND COMPUTER
INDUSTRY WANT TO BE LEADERS IN SUPER
COMPUTING

THREE NATIONAL PROJECTS

- COMPONENTS
- HIGH-SPEED COMPUTER
- FIFTH GENERATION COMPUTER

NUMEROUS INDIVIDUAL COMPANY PROJECTS

COMPUTING

Los Alamos

**JAPANESE NATIONAL
SUPER-SPEED COMPUTER PROJECT**

DURATION: 1982-89

FUNDING: \$200M

**OBJECTIVES: 10 GIGAFLOPS
1 GIGABYTE OF MEMORY WITH
1.5 GIGABYTE BANDWIDTH
100 MEGAFLOPS IN DISTRIBUTED
PROCESSING**

PARTICIPANTS:

- ETL**
- FUJITSU**
- HITACHI**
- NEC**
- MITSUBISHI**
- OKI**
- TOSHIBA**

COMPUTING

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FIFTH GENERATION COMPUTER

STARTS APRIL 1982

OBJECTIVE: A LARGE, INTELLIGENT COMPUTER SYSTEM
FOR

- LANGUAGE PROCESSING
- SPEECH AND IMAGE PROCESSING
- EXPERT SYSTEMS

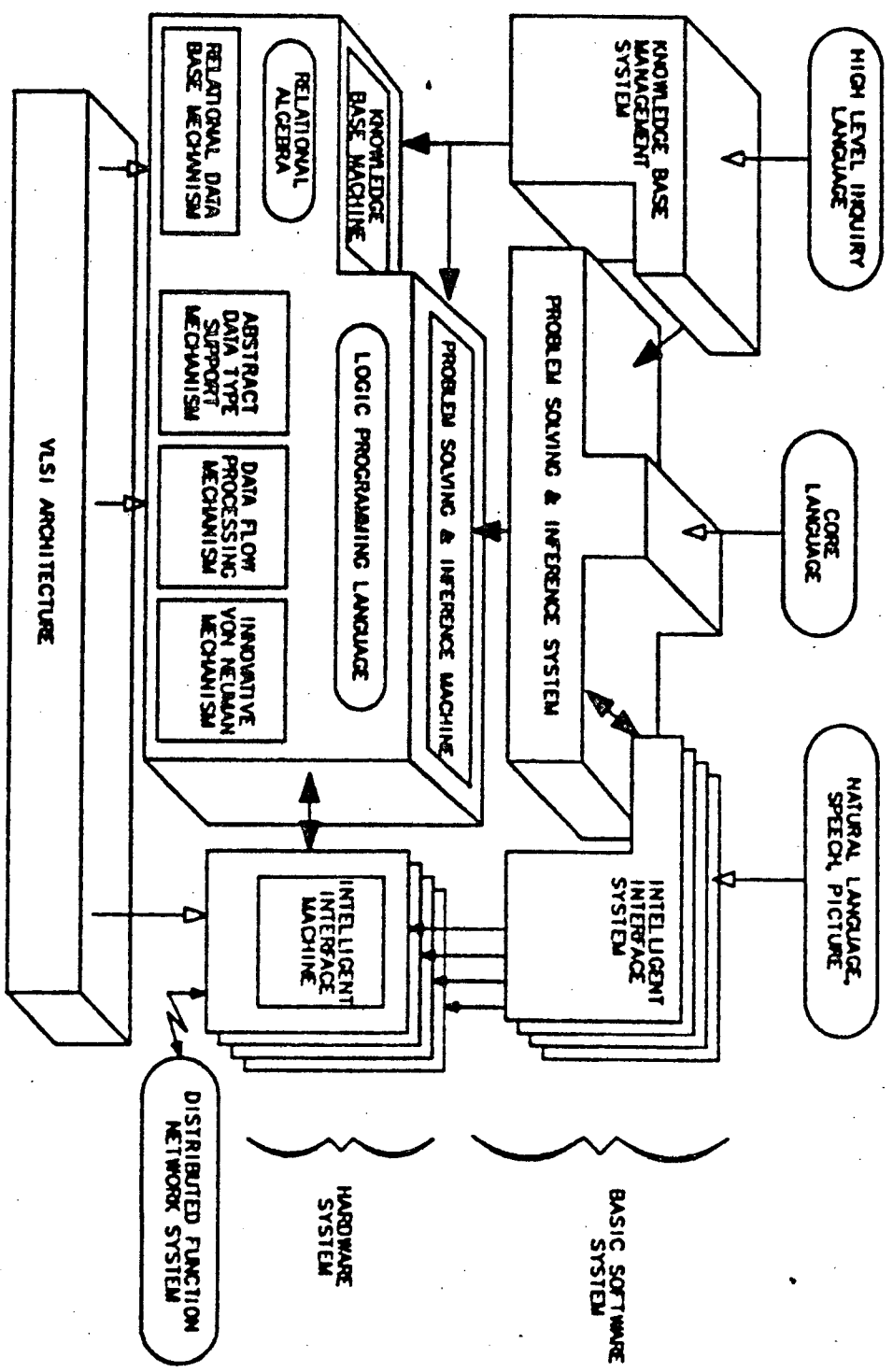
THREE PHASES

- 1ST - 3 YEARS - FUNCTIONAL MODULES
- 2ND - 4 YEARS - BUILD A PROTOTYPE
- 3RD - 3 YEARS - COMPLETE THE SYSTEM
AND SOFTWARE

\$45M OF GOVERNMENT FUNDS FOR FIRST PHASE

COMPUTING

Los Alamos



BASIC CONFIGURATION IMAGE OF THE FIFTH GENERATION COMPUTER SYSTEM (JAPANESE)

COMPUTING

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5TH GENERATION COMPUTER: SPECIFICATIONS

- HIGHER PERFORMANCE LEVEL AT A LOWER COST
- "TRIPARTITE BRAIN"
 - 1) INTELLIGENT INTERFACE SYSTEM
 - ACCESS THROUGH NATURAL LANGUAGE AND PICTURES
 - 2) PROBLEM-SOLVING AND INFERENCE SYSTEM
 - HANDLE MANY MORE GENERAL PROBLEM-SOLVING TASKS THAN TODAY'S MACHINES
 - BE ABLE TO LEARN, ASSOCIATE, AND INFER
 - 3) KNOWLEDGE-BASED MANAGEMENT SYSTEM
 - BE ABLE TO UNDERSTAND AND USE STORED INFORMATION
 - "KNOWLEDGE BASES" RATHER THAN "DATABASES"
- EACH OF THE THREE SYSTEMS HAS OWN SPECIALIZED MACHINE WITH VLSI ARCHITECTURE
- COMPUTER SIZES TO RANGE FROM MICRO'S TO MAINFRAMES

SOURCE: TOM MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: EXAMPLE: PROJECTS AND SPECIFICATIONS

- PERSONAL WORK STATION
 - PERFORM 2 MIPS
 - HAVE .5 TO 5 MEGABYTES OF MEMORY
 - HAVE 100 MEGABYTES OF DISK STORAGE, WITH AN AVERAGE ACCESS OF 1 MILLISECOND
- "SUPER HIGH-SPEED PROCESSOR"
 - PERFORM 1 TO 100 BILLION FLOATING POINT OPERATIONS PER SECOND (FLOPS)
 - HAVE 8 TO 160 MEGABYTES OF MEMORY
- PROBLEM — SOLVING AND INFERENCE FUNCTION
 - PERFORM 100 MILLION TO 1 BILLION LOGICAL-INFERENCE OPERATIONS PER SECOND

(1 LOGICAL INFERENCE = 100 TO 1000 INSTRUCTIONS)
- NATURAL LANGUAGE PROCESSING SYSTEM
- KNOWLEDGE-BASED MANAGEMENT FUNCTION
 - RETRIEVE 1 UNIT OF KNOWLEDGE IN SEVERAL SECONDS FROM A BASE OF 100 TO 1000 GIGABYTES

SOURCE: MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: EXAMPLE: PROJECTS AND SPECIFICATIONS

- VERY-LARGE-SCALE INTEGRATION TECHNOLOGY
- AT FIRST, HAVE 1 MILLION TRANSISTORS PER CHIP
- EVENTUALLY HAVE 10 MILLION TRANSISTORS PER CHIP

SOURCE: MANUEL, BYTE, 5/82

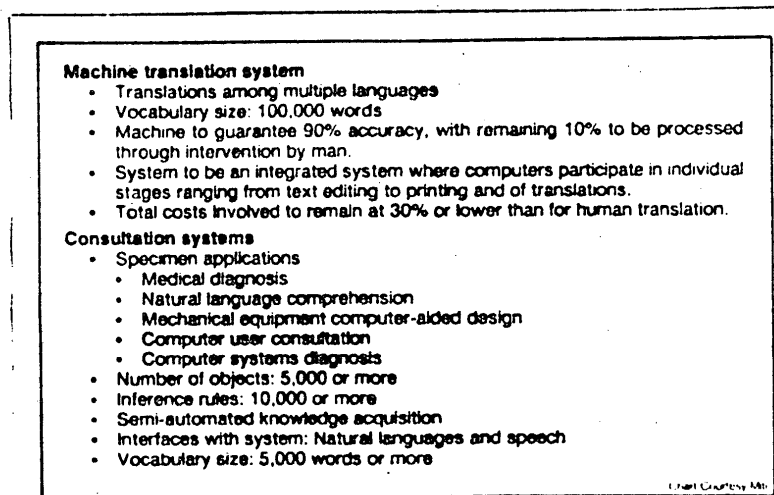


Figure 1. Subjects and 10-Year Targets for Basic Applications Systems

SOURCE: REX MALIK, COMPUTERWORLD/EXTRA
11/17/82, P. 25

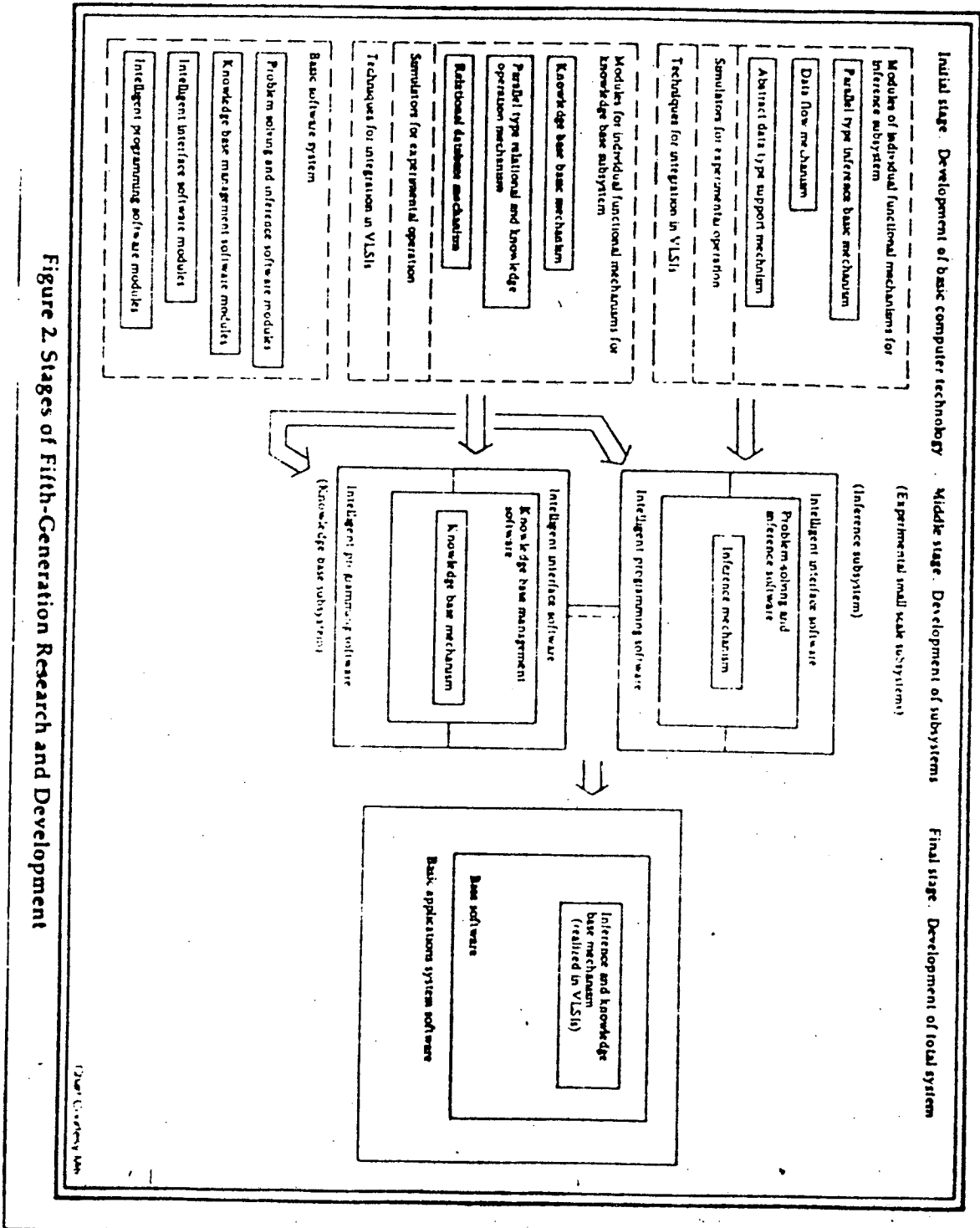


Figure 2. Stages of Fifth-Generation Research and Development

SOURCE: REX MALIK, COMPUTERWORLD/EXTRA 11/17/82, P. 25

5TH GENERATION COMPUTER: NEW TECHNOLOGIES

- NEW TECHNIQUES TO BE USED
 - NEW ARCHITECTURES LIKE DATA-FLOW MACHINES
 - ARTIFICIAL-INTELLIGENCE CONCEPTS
 - LANGUAGES SUCH AS LISP AND PROLOG WITH MACHINES OPTIMIZED FOR THEM
- TECHNOLOGIES CURRENTLY EXCLUDED FROM PROGRAM
 - EXAMPLES
 - GALLIUM ARSENIDE
 - JOSEPHSON JUNCTIONS
 - RESEARCHERS FELT THESE TECHNOLOGIES WOULD NOT BE SUFFICIENTLY DEVELOPED FOR GENERAL USE BY 1990
 - THEY WILL BE INCLUDED AT SOME INTERMEDIATE STAGE IF OUTSIDE RESEARCH GAINS OCCUR

SOURCE: MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: DESIGN AUTOMATION SYSTEM (page 4)

- CONSISTS OF THREE PARTS
 - 1) SOFTWARE FOR AUTOMATED DESIGN OF VLSI
 - PLAN TO INITIALLY IMPLEMENT HSL (HIERARCHICAL SPECIFICATION LANGUAGE)
 - HSL CONTAINS SEVERAL MODULES INTEGRATED INTO A TOTAL DESIGN SYSTEM
 - CURRENTLY BEING USED AT THE MUSASHINO ELECTRICAL COMMUNICATION LABORATORY OF NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION
 - 2) SYSTEM 5G - THE COMPUTER SYSTEM TO RUN IT
 - PLAN TO USE CONVENTIONAL 40 MIPS GENERAL-PURPOSE COMPUTER UNTIL FIRST 5TH GENERATION COMPUTERS ARE AVAILABLE

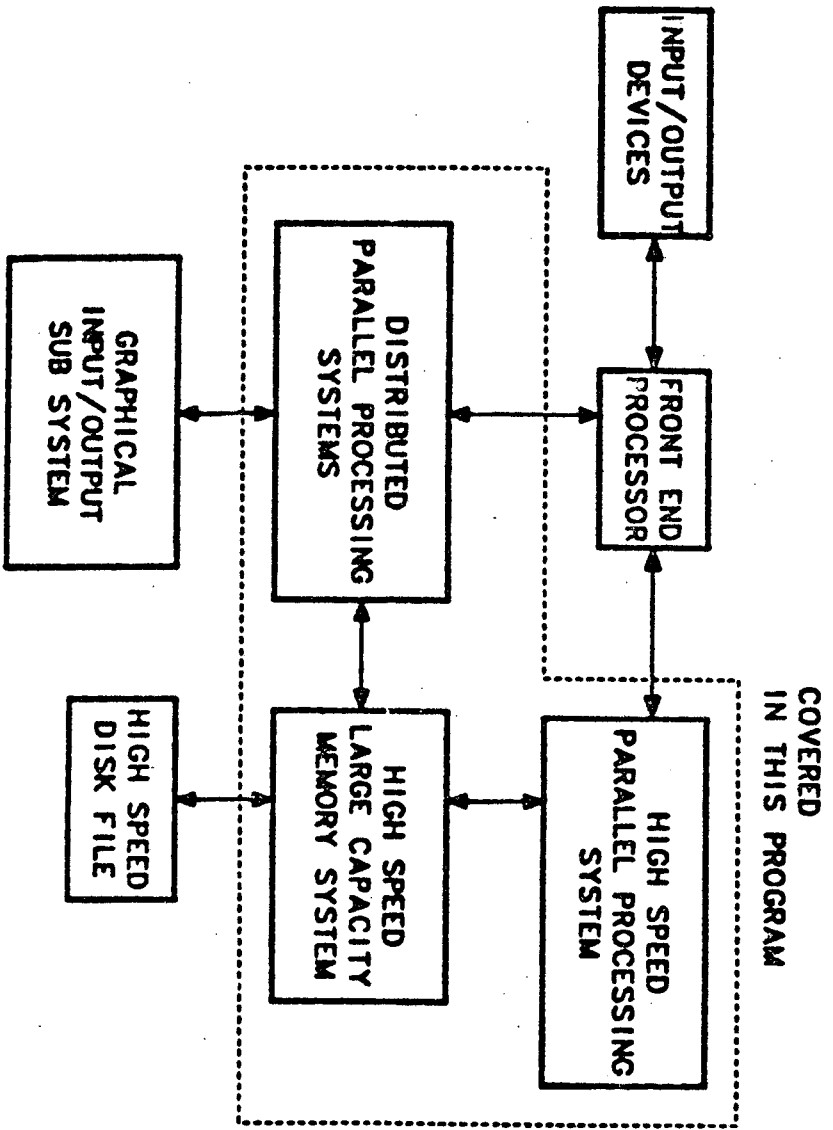
SOURCE: MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: DESIGN AUTOMATION SYSTEM (PAGE 2)

- 3) 5G PERSONAL COMPUTER - LOGIC-PROGRAMMING WORK STATION FOR DESIGNERS
- REQUIRES HIGH-SPEED PROCESSING OF VOICE, GRAPHIC, AND DIGITIZED IMAGE INPUT AS WELL AS PERFORMANCE AS A PERSONAL-INTERFACE MACHINE
 - NO EXISTING PERSONAL COMPUTER MEETS THESE SPECIFICATIONS

SOURCE: MANUEL, BYTE, 5/82

JAPANESE ULTRA-HIGH-SPEED COMPUTING FACILITY



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**ADVANCES ARE REQUIRED
IN**

COMPONENTS

ARCHITECTURE

ALGORITHMS AND LANGUAGES

COMPUTING

Los Alamos

COMPONENT OBJECTIVES

LOGIC: 3k GATES. 10 ps DELAY (JJHEMT)
3k GATES. 30 ps DELAY (GAs)

MEMORY: 16k bits. 10 ns ACCESS

COMPUTING

Los Alamos

SUMMARY

JAPAN HAS LAUNCHED A NATIONAL PROGRAM TO BECOME A WORLD LEADER IN SUPERCOMPUTERS.

ALL SIX MAJOR JAPANESE VENDORS ARE PARTICIPATING.

THE PROJECT IS LIKELY TO PRODUCE A COMPUTER AND EVEN PARTIAL SUCCESS COULD HAVE FAR REACHING CONSEQUENCES.

COMPUTING

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5TH GENERATION COMPUTER: SOME JAPANESE EXPECTATIONS

- BENEFITS TO BE GAINED
 - RAISING PRODUCTIVITY IN LOW-PRODUCTIVITY FIELDS
 - PRESERVATION OF INTERNATIONAL COMPETITIVE CAPABILITY BY DEVELOPMENT OF NEW TECHNOLOGY
 - CONSERVATION OF ENERGY AND RESOURCES
 - PROMOTE UTILIZATION OF CAPACITY OF AGING CITIZENS
 - INFORMATIONALIZATION OF SOCIETY

SOURCES:

SID FERNBACH, BRIEF ON THE
JAPANESE COMPUTER INDUSTRY, MAY, 1981

ZEN YAMADA, MEMORANDUM ON RECENT
PUBLISHED INFORMATION, MAY 13, 1981

5TH GENERATION COMPUTER: SOME JAPANESE EXPECTATIONS

- FEATURES OF 5TH GENERATION COMPUTER
 - CONSIDERABLE DIVERSITY
 - EMPHASIS ON SPECIALIZATION
 - NON-VON NEUMANN ARCHITECTURE
 - COMPOSITE MICRO-ARCHITECTURE
 - INPUT/OUTPUT OF DAILY LANGUAGES, CHARACTERS, GRAPHS WITH NO MODIFICATION
 - SELF-RECOVERING FUNCTION (AUTOMATIC RECOVERY)
 - SELF-PROGRAMMABLE WITH SIMPLE INSTRUCTIONS (NO REQUIREMENT FOR HUGE PROGRAMS)
 - FUTURE PROBLEM SOLVING BASED ON RECORDED DATA

SOURCES: SID FERNBACH, BRIEF ON THE JAPANESE COMPUTER INDUSTRY, MAY, 1981

ZEN YAMADA, MEMORANDUM ON RECENT PUBLISHED INFORMATION, MAY 13, 1981

5TH GENERATION COMPUTER: SOME JAPANESE EXPECTATIONS

- MAJOR R&D THEMES

- DEVICE TECHNOLOGY
- ARCHITECTURE AND HIGH PERFORMANCE PROCESSES
- DISTRIBUTED FUNCTIONAL SYSTEMS
- SOFTWARE ENGINEERING
- INTELLIGENT ROBOTS
- HIGH RELIABILITY, SECRECY PROTECTION FUNCTION

SOURCES: SID FERNBACH, BRIEF ON THE
JAPANESE COMPUTER INDUSTRY, MAY, 1981
ZEN YAMADA, MEMORANDUM ON RECENT
PUBLISHED INFORMATION, MAY 13, 1981

JAPANESE COMPUTER RESEARCH: SOFTWARE DEVELOPMENT

- "THE ELECTRONIC COMPUTER BASIC TECHNOLOGY DEVELOPMENT ASSOCIATION"
 - COOPERATIVE ASSOCIATION TO DEVELOP SOFTWARE
 - MEMBERS
 - HITACHI
 - TOSHIBA
 - FUJITSU
 - NEC
 - MITSUBISHI
 - OKI
 - MATSUSHITA
 - SHARP
 - NEC - TOSHIBA INFORMATION SYSTEMS
 - COMPUTER DEVELOPMENT LABORATORY
- WILL SPEND \$56 M (1981-1986)
 - MITI WILL PROVIDE HALF THE FUNDS

SOURCE: SID FERNBACH, BRIEF REPORT
ON THE JAPANESE COMPUTER
INDUSTRY, MAY, 1981